Lab Assignment 4

Name: Manobal Singh Bagady

SID: 21104129 **Semester:** 8

Branch: Electrical Engineering

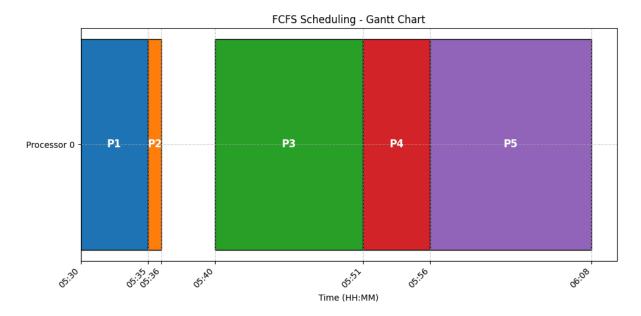
Due Date: Mar 5, 2025

The arrival time for four processes to a system are as below:

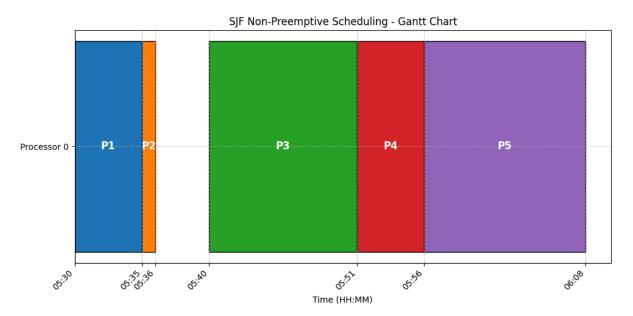
Process ID	Arrival Time	Estimated Processing Time
P1	5:30 PM	5 unit time
P2	5:33 PM	1 unit time
Р3	5:40 PM	11 unit time
P4	5:42 PM	5 unit time
P5	5:45 PM	12 unit time

Different Timing Diagrams for these processes:

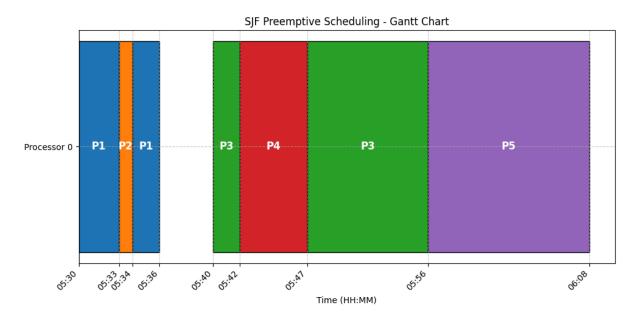
1. Multiprogramming System (FCFS)



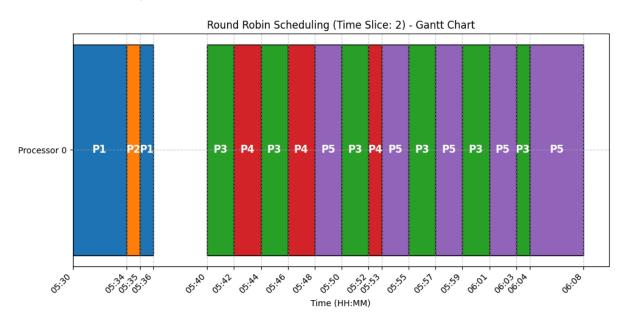
2. Multiprogramming with priority for shortest job first in non-preemptive mode (SJF)



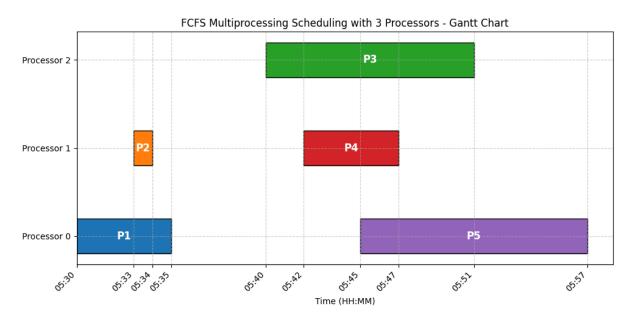
3. Multiprogramming with priority for shortest job first in pre-emptive mode (SRTF)



4. Time sharing system (RR) with time slice of 2-unit time



5. Multiprocessing system (FCFS) with 3 processors



6. Multiprocessing time sharing system (RR) with two processors and time slice of 2 unit time

