



Solutions



1.1 Personal computer: Computer that emphasizes delivery of good performance to a single user at low cost and usually executes third-party software.

Server: Computer used for large workloads and usually accessed via a network.

Embedded computer: Computer designed to run one application or one set of related applications and integrated into a single system.

1.2

- Performance via Pipelining
- Dependability via Redundancy
- Performance via Prediction
- Make the Common Case Fast
- Hierarchy of Memories
- Performance via Parallelism
- Use Abstraction to Simplify Design

1.3 The program is compiled into an assembly language program, which is itself assembled into a machine language program.

1.4

- $1280 \times 1024 \text{ pixels} = 1,310,720 \text{ pixels} \Rightarrow 1,310,720 \times 3 = 3,932,160 \text{ bytes/frame.}$
- $3,932,160 \text{ bytes} \times (8 \text{ bits/byte}) / 100\text{E6 bits/second} = 0.31 \text{ seconds}$

1.5

Desktop Processor	Year	Tech	Max. Clock Speed (GHz)	Integer IPC/core	Cores	Max. DRAM Bandwidth (GB/s)	SP Floating Point (Gflop/s)	MiB
Westmere i7-620	2010	32	3.33	4	2	17.1	107	4
Ivy Bridge i7-3770K	2013	22	3.90	6	4	25.6	250	8
Broadwell i7-6700K	2015	14	4.20	8	4	34.1	269	8
Kaby Lake i7-7700K	2017	14	4.50	8	4	38.4	288	8
Coffee Lake i7-9700K	2019	14	4.90	8	8	42.7	627	12
Imp./year		20%	4%	7%	15%	10%	19%	12%
Doubles every		4 years	18 years	10 years	5 years	7 years	4 years	6 years



1.6

- a. performance of P1 (instructions/sec) = $3 \times 10^9 / 1.5 = 2 \times 10^9$
 performance of P2 (instructions/sec) = $2.5 \times 10^9 / 1.0 = 2.5 \times 10^9$
 performance of P3 (instructions/sec) = $4 \times 10^9 / 2.2 = 1.8 \times 10^9$
- b. cycles(P1) = $10 \times 3 \times 10^9 = 30 \times 10^9$ s
 cycles(P2) = $10 \times 2.5 \times 10^9 = 25 \times 10^9$ s
 cycles(P3) = $10 \times 4 \times 10^9 = 40 \times 10^9$ s
- c. No. instructions(P1) = $30 \times 10^9 / 1.5 = 20 \times 10^9$
 No. instructions(P2) = $25 \times 10^9 / 1 = 25 \times 10^9$
 No. instructions(P3) = $40 \times 10^9 / 2.2 = 18.18 \times 10^9$
 $CPI_{\text{new}} = CPI_{\text{old}} \times 1.2$, then $CPI(P1) = 1.8$, $CPI(P2) = 1.2$, $CPI(P3) = 2.6$
 $f = \text{No. instr.} \times CPI / \text{time}$, then
 $f(P1) = 20 \times 10^9 \times 1.8 / 7 = 5.14 \text{ GHz}$
 $f(P2) = 25 \times 10^9 \times 1.2 / 7 = 4.28 \text{ GHz}$
 $f(P3) = 18.18 \times 10^9 \times 2.6 / 7 = 6.75 \text{ GHz}$

1.7

- a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.
 Time = No. instr. \times CPI/clock rate
 Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3) / (2.5 \times 10^9)$
 $= 10.4 \times 10^{-4}$ s
 Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2) / (3 \times 10^9)$
 $= 6.66 \times 10^{-4}$ s
 $CPI(P1) = 10.4 \times 10^{-4} \times 2.5 \times 10^9 / 10^6 = 2.6$
 $CPI(P2) = 6.66 \times 10^{-4} \times 3 \times 10^9 / 10^6 = 2.0$
- b. clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$
 clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

1.8

- a. $CPI = T_{\text{exec}} \times f / \text{No. instr.}$
 Compiler A $CPI = 1.1$
 Compiler B $CPI = 1.25$





$$\text{b. } f_B/f_A = (\text{No. instr.}(B) \times \text{CPI}(B))/(\text{No. instr.}(A) \times \text{CPI}(A)) = 1.37$$

$$\text{c. } T_A/T_{\text{new}} = 1.67$$

$$T_B/T_{\text{new}} = 2.27$$

1.9

$$\text{1.9.1 } C = 2 \times DP/(V^2 \times F)$$

$$\text{Pentium 4: } C = 3.2\text{E-}8F$$

$$\text{Core i5 Ivy Bridge: } C = 2.9\text{E-}8F$$

$$\text{1.9.2 Pentium 4: } 10/100 = 10\%$$

$$\text{Core i5 Ivy Bridge: } 30/70 = 42.9\%$$

$$\text{1.9.3 } (S_{\text{new}} + D_{\text{new}})/(S_{\text{old}} + D_{\text{old}}) = 0.90$$

$$D_{\text{new}} = C \times V_{\text{new}}^2 \times F$$

$$S_{\text{old}} = V_{\text{old}} \times I$$

$$S_{\text{new}} = V_{\text{new}} \times I$$

Therefore:

$$V_{\text{new}} = [D_{\text{new}}/(C \times F)]^{1/2}$$

$$D_{\text{new}} = 0.90 \times (S_{\text{old}} + D_{\text{old}}) - S_{\text{new}}$$

$$S_{\text{new}} = V_{\text{new}} \times (S_{\text{old}}/V_{\text{old}})$$

Pentium 4:

$$S_{\text{new}} = V_{\text{new}} \times (10/1.25) = V_{\text{new}} \times 8$$

$$D_{\text{new}} = 0.90 \times 100 - V_{\text{new}} \times 8 = 90 - V_{\text{new}} \times 8$$

$$V_{\text{new}} = [(90 - V_{\text{new}} \times 8)/(3.2\text{E}8 \times 3.6\text{E}9)]^{1/2}$$

$$V_{\text{new}} = 0.85 \text{ V}$$

Core i5:

$$S_{\text{new}} = V_{\text{new}} \times (30/0.9) = V_{\text{new}} \times 33.3$$

$$D_{\text{new}} = 0.90 \times 70 - V_{\text{new}} \times 33.3 = 63 - V_{\text{new}} \times 33.3$$

$$V_{\text{new}} = [(63 - V_{\text{new}} \times 33.3)/(2.9\text{E}8 \times 3.4\text{E}9)]^{1/2}$$

$$V_{\text{new}} = 0.64 \text{ V}$$





1.10

1.10.1

p	# arith inst.	# L/S inst.	# branch inst.	cycles	ex. time	speedup
1	2.56E9	1.28E9	2.56E8	1.92E10	9.60	1.00
2	1.83E9	9.14E8	2.56E8	1.41E10	7.04	1.36
4	9.14E8	4.57E8	2.56E8	7.68E9	3.84	2.50
8	4.57E8	2.29E8	2.56E8	4.48E9	2.24	4.29

1.10.2

p	ex. time
1	41.0
2	29.3
4	14.6
8	7.33

1.10.3 3

1.11

1.11.1 die area_{15cm} = wafer area/dies per wafer = $\pi \times 7.5^2 / 84 = 2.10 \text{ cm}^2$

$$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \times 2.10/2))^2 = 0.9593$$

die area_{20cm} = wafer area/dies per wafer = $\pi \times 10^2/100 = 3.14 \text{ cm}^2$

$$\text{yield}_{20\text{cm}} = 1/(1 + (0.031 \times 3.14/2))^2 = 0.9093$$

1.11.2 cost/die_{15cm} = $12/(84 \times 0.9593) = 0.1489$

$$\text{cost/die}_{20\text{cm}} = 15/(100 \times 0.9093) = 0.1650$$

1.11.3 die area_{15cm} = wafer area/dies per wafer = $\pi \times 7.5^2/(84 \times 1.1) = 1.91 \text{ cm}^2$

$$\text{yield}_{15\text{cm}} = 1/(1 + (0.020 \times 1.15 \times 1.91/2))^2 = 0.9575$$

die area_{20cm} = wafer area/dies per wafer = $\pi \times 10^2/(100 \times 1.1) = 2.86 \text{ cm}^2$

$$\text{yield}_{20\text{cm}} = 1/(1 + (0.03 \times 1.15 \times 2.86/2))^2 = 0.9082$$

1.11.4 defects per area_{0.92} = $(1-y^{-.5})/(y^{-.5} \times \text{die_area}/2) = (1 - 0.92^{-.5})/(0.92^{-.5} \times 2/2) = 0.043 \text{ defects/cm}^2$

$$\text{defects per area}_{0.95} = (1-y^{-.5})/(y^{-.5} \times \text{die_area}/2) = (1 - 0.95^{-.5})/(0.95^{-.5} \times 2/2) = 0.026 \text{ defects/cm}^2$$

1.12

1.12.1 CPI = clock rate \times CPU time/instr. count

$$\text{clock rate} = 1/\text{cycle time} = 3 \text{ GHz}$$

$$\text{CPI}(\text{bzip2}) = 3 \times 10^9 \times 750/(2389 \times 10^9) = 0.94$$



1.12.2 SPEC ratio = ref. time/execution time

$$\text{SPEC ratio(bzip2)} = 9650/750 = 12.86$$

1.12.3 CPU time = No. instr. \times CPI/clock rate

If CPI and clock rate do not change, the CPU time increase is equal to the increase in the number of instructions, that is 10%.

1.12.4 CPU time(before) = No. instr. \times CPI/clock rate

$$\text{CPU time(after)} = 1.1 \times \text{No. instr.} \times 1.05 \times \text{CPI/clock rate}$$

$\text{CPU time(after)}/\text{CPU time(before)} = 1.1 \times 1.05 = 1.155$. Thus, CPU time is increased by 15.5%.

1.12.5 SPECratio = reference time/CPU time

$$\text{SPECratio(after)}/\text{SPECratio(before)} = \text{CPU time(before)}/\text{CPU time(after)} = 1/1.155 = 0.86. \text{ The SPECratio is decreased by 14\%.}$$

1.12.6 CPI = (CPU time \times clock rate)/No. instr.

$$\text{CPI} = 700 \times 4 \times 10^9 / (0.85 \times 2389 \times 10^9) = 1.37$$

1.12.7 Clock rate ratio = 4 GHz/3 GHz = 1.33

$$\text{CPI @ 4 GHz} = 1.37, \text{ CPI @ 3 GHz} = 0.94, \text{ ratio} = 1.45$$

They are different because, although the number of instructions has been reduced by 15%, the CPU time has been reduced by a lower percentage.

1.12.8 $700/750 = 0.933$. CPU time reduction: 6.7%

1.12.9 No. instr. = CPU time \times clock rate/CPI

$$\text{No. instr.} = 960 \times 0.9 \times 4 \times 10^9 / 1.61 = 2146 \times 10^9$$

1.12.10 Clock rate = No. instr. \times CPI/CPU time.

$$\text{Clock rate}_{\text{new}} = \text{No. instr.} \times \text{CPI} / 0.9 \times \text{CPU time} = 1/0.9 \text{ clock rate}_{\text{old}} = 4.44 \text{ GHz}$$

1.12.11 Clock rate = No. instr. \times CPI/CPU time.

$$\text{Clock rate}_{\text{new}} = \text{No. instr.} \times 0.85 \times \text{CPI} / 0.80 \text{ CPU time} = 0.85/0.80, \text{ clock rate}_{\text{old}} = 3.18 \text{ GHz}$$

1.13

1.13.1 $T(P1) = 5 \times 10^9 \times 0.9 / (4 \times 10^9) = 1.125 \text{ s}$

$$T(P2) = 10^9 \times 0.75 / (3 \times 10^9) = 0.25 \text{ s}$$

clock rate (P1) > clock rate(P2), performance(P1) < performance(P2)



1.13.2 $T(P1) = \text{No. instr.} \times \text{CPI/clock rate}$

$$T(P1) = 2.25 \times 10^{21} \text{ s}$$

$$T(P2) = 5 \times 10^9 \times 0.75 / (3 \times 10^9), \text{ then } N = 9 \times 10^8$$

1.13.3 $\text{MIPS} = \text{Clock rate} \times 10^{-6} / \text{CPI}$

$$\text{MIPS}(P1) = 4 \times 10^9 \times 10^{-6} / 0.9 = 4.44 \times 10^3$$

$$\text{MIPS}(P2) = 3 \times 10^9 \times 10^{-6} / 0.75 = 4.0 \times 10^3$$

$$\text{MIPS}(P1) > \text{MIPS}(P2), \text{ performance}(P1) < \text{performance}(P2) \text{ (from 11a)}$$

1.13.4 $\text{MFLOPS} = \text{No. FP operations} \times 10^{-6} / T$

$$\text{MFLOPS}(P1) = .4 \times 5 \times 10^9 \times 10^{-6} / 1.125 = 1.78 \text{E}3$$

$$\text{MFLOPS}(P2) = .4 \times 1 \times 10^9 \times 10^{-6} / .25 = 1.60 \text{E}3$$

$$\text{MFLOPS}(P1) > \text{MFLOPS}(P2), \text{ performance}(P1) < \text{performance}(P2) \text{ (from 11a)}$$

1.14

1.14.1 $T_{fp} = 70 \times 0.8 = 56 \text{ s}$, $T_{new} = 56 + 85 + 55 + 40 = 236 \text{ s}$. Reduction: 5.6%

1.14.2 $T_{new} = 250 \times 0.8 = 200 \text{ s}$, $T_{fp} + T_{l/s} + T_{branch} = 165 \text{ s}$, $T_{int} = 35 \text{ s}$. Reduction time INT: 58.8%

1.14.3 $T_{new} = 250 \times 0.8 = 200 \text{ s}$, $T_{fp} + T_{int} + T_{l/s} = 210 \text{ s}$. NO

1.15

1.15.1 $\text{Clock cycles} = \text{CPI}_{fp} \times \text{No. FP instr.} + \text{CPI}_{int} \times \text{No. INT instr.} + \text{CPI}_{l/s} \times \text{No. L/S instr.} + \text{CPI}_{branch} \times \text{No. branch instr.}$

$$T_{CPU} = \text{clock cycles} / \text{clock rate} = \text{clock cycles} / 2 \times 10^9$$

$$\text{clock cycles} = 512 \times 10^6; T_{CPU} = 0.256 \text{ s}$$

To have the number of clock cycles by improving the CPI of FP instructions:

$$\text{CPI}_{improved fp} \times \text{No. FP instr.} + \text{CPI}_{int} \times \text{No. INT instr.} + \text{CPI}_{l/s} \times \text{No. L/S instr.} + \text{CPI}_{branch} \times \text{No. branch instr.} = \text{clock cycles} / 2$$

$$\text{CPI}_{improved fp} = (\text{clock cycles} / 2 - (\text{CPI}_{int} \times \text{No. INT instr.} + \text{CPI}_{l/s} \times \text{No. L/S instr.} + \text{CPI}_{branch} \times \text{No. branch instr.})) / \text{No. FP instr.}$$

$$\text{CPI}_{improved fp} = (256 - 462) / 50 < 0 \Rightarrow \text{not possible}$$

1.15.2 Using the clock cycle data from a.

To have the number of clock cycles improving the CPI of L/S instructions:

$$\text{CPI}_{fp} \times \text{No. FP instr.} + \text{CPI}_{int} \times \text{No. INT instr.} + \text{CPI}_{improved l/s} \times \text{No. L/S instr.} + \text{CPI}_{branch} \times \text{No. branch instr.} = \text{clock cycles} / 2$$



$$CPI_{\text{improved l/s}} = (\text{clock cycles}/2 - (CPI_{\text{fp}} \times \text{No. FP instr.} + CPI_{\text{int}} \times \text{No. INT instr.} + CPI_{\text{branch}} \times \text{No. branch instr.})) / \text{No. L/S instr.}$$

$$CPI_{\text{improved l/s}} = (256 - 198)/80 = 0.725$$

1.15.3 Clock cycles = $CPI_{\text{fp}} \times \text{No. FP instr.} + CPI_{\text{int}} \times \text{No. INT instr.} + CPI_{\text{l/s}} \times \text{No. L/S instr.} + CPI_{\text{branch}} \times \text{No. branch instr.}$

$$T_{\text{CPU}} = \text{clock cycles}/\text{clock rate} = \text{clock cycles}/2 \times 10^9$$

$$CPI_{\text{int}} = 0.6 \times 1 = 0.6; CPI_{\text{fp}} = 0.6 \times 1 = 0.6; CPI_{\text{l/s}} = 0.7 \times 4 = 2.8; CPI_{\text{branch}} = 0.7 \times 2 = 1.4$$

$$T_{\text{CPU}} (\text{before improv.}) = 0.256 \text{ s}; T_{\text{CPU}} (\text{after improv.}) = 0.171 \text{ s}$$

1.16

processors	exec. time/ processor	time w/overhead	speedup	actual speedup/ideal speedup
1	100			
2	50	54	$100/54 = 1.85$	$1.85/2 = .93$
4	25	29	$100/29 = 3.44$	$3.44/4 = 0.86$
8	12.5	16.5	$100/16.5 = 6.06$	$6.06/8 = 0.75$
16	6.25	10.25	$100/10.25 = 9.76$	$9.76/16 = 0.61$