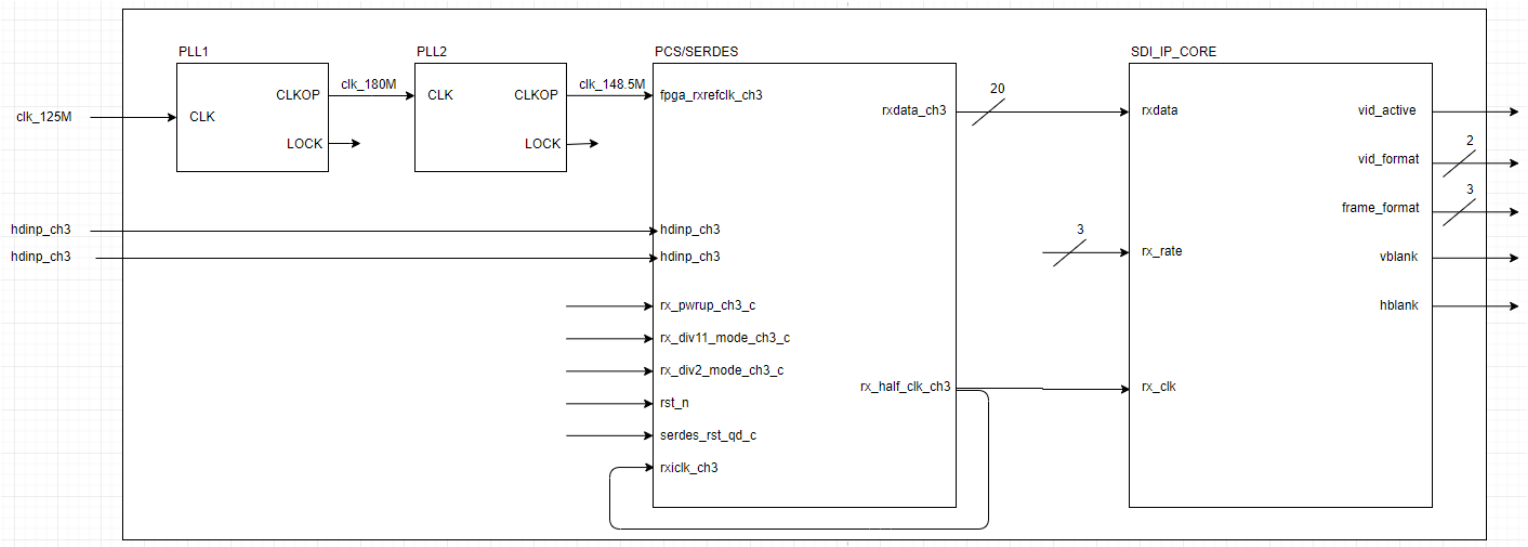
Diagramme de block partie analyse flux
Protocole SDI

Voici le diagramme de block qui explique les ports d'entrés et de sorties de notre système, ainsi que les connections entre les sous-blocks :



Les trames qu'on a choisies sont les suivantes :

Octet	Nom	Valeur	Description
1	Nb_Octets	0x9	Nombre d'octet de la trame
2	ID_Sys	0x3	Système dont la commande est sollicitée
3	ID_Cmd	0x1	SDI_INFO
4	Vid_format	2 bits	Se compose de 2 bits, il permet d'afficher la résolution (voir tableau ci-dessous)
6	Frame_format	3 bits	Se compose de 3 bits, il permet d'afficher le frame format (voir tableau ci-dessous)
7	Vid_active	1 bit	Une info d'un bit qui indique qu'une ligne du frame est transmise.
8	vblank	1 bit	Une info d'un bit, si égal 1 en reçoit un flux sinon on ne reçoit rien
9	hblank	1 bit	Un signal d'un bit est transmis après le transfert de la frame entière

Les ports les plus importants à récupérer pour les envoyer à l'IHM avec une description :

Port	Bits	I/O	Description
vid_active	1	O	Video active signal. This output signal is high if the receiver is locked to a valid video stream at the receiver input.
vid_format	2	O	Video format output. The format is identified as follows: 01 – 1280 x 720 11 – 1920 x 1080 For 3G-b outputs, the video format corresponds to stream 1 video
frame_format	3	O	Frame format output. This output identifies the number of fields and whether the video is interlaced or progressive as follows: 000 – Unknown or custom 001 – 24p or 23.98p or 23.98psF 010 – 25p, 25psF 011 – 30p or 29.97p or 29.97psF 100 – 50i 101 – 60i or 59.94i 110 – 50p 111 – 60p or 59.94p For 3G-b outputs, the frame format corresponds to stream 1 video
vblank	1	O	Vertical blanking signal. The value at this output changes state when the XYZ word appears at the output. For 3G-b video, the vblank output corresponds to stream 1 video and it changes state when the y-channel XYZ word appears at the output.
hblank	1	O	Horizontal blanking signal. The value at this output changes state when the XYZ word appears at the output. For 3G-b video, the hblank output corresponds to stream 1 video and it changes state when the y-channel XYZ word appears at the output.

Port	Bits	I/O	Description
Clk_125	1	I	FPGA internal clock.
hdinp_ch3	1	I	High-speed CML input, positive, channel 3
hdinn_ch3	1	I	High-speed CML input, negative, channel 3
rx_rate	3	I/signal interne (pas encore confirmé)	This input command controls the rates scanned by the receiver. Each bit enables the scanning of one of the rates, as shown below: rx_rate [2]: 0 - disable 3G scan, 1 - enable 3G scan rx_rate [1]: 0 - disable HD scan, 1 - enable HD scan rx_rate [0]: 0 - disable SD scan, 1 - enable SD scan This is an asynchronous control input. The receiver scans only for the rates that are enabled. However, if the scan for one of the rates is disabled when that rate is being received, the reception is not affected.