

1. Description

1.1. Project

Project Name	PDM_INITIAL_WITHOUT_USER_L
	ABELS
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	12/09/2023

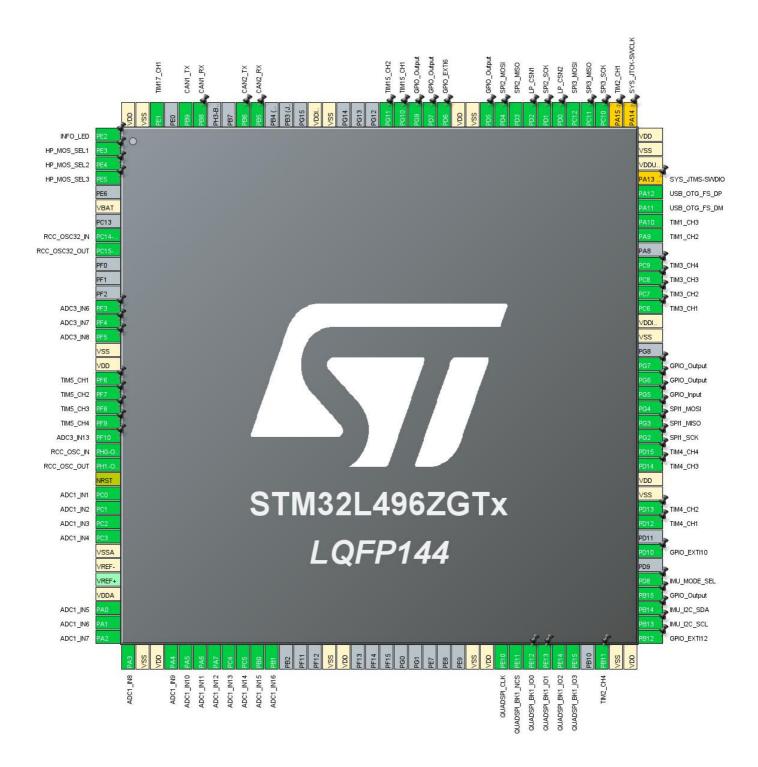
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

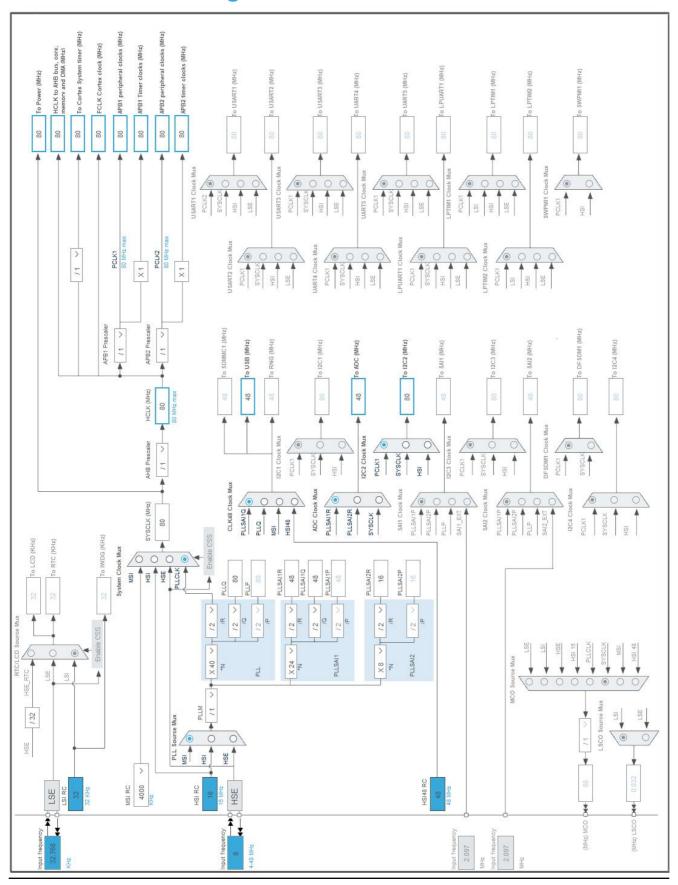
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
1	PE2 *	I/O	GPIO_Output	INFO_LED
2	PE3 *	I/O	GPIO_Output	HP_MOS_SEL1
3	PE4 *	I/O	GPIO_Output	HP_MOS_SEL2
4	PE5 *	I/O	GPIO_Output	HP_MOS_SEL3
6	VBAT	Power		
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
13	PF3	I/O	ADC3_IN6	
14	PF4	I/O	ADC3_IN7	
15	PF5	I/O	ADC3_IN8	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	TIM5_CH1	
19	PF7	I/O	TIM5_CH2	
20	PF8	I/O	TIM5_CH3	
21	PF9	I/O	TIM5_CH4	
22	PF10	I/O	ADC3_IN13	
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN1	
27	PC1	I/O	ADC1_IN2	
28	PC2	I/O	ADC1_IN3	
29	PC3	I/O	ADC1_IN4	
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
34	PA0	I/O	ADC1_IN5	
35	PA1	I/O	ADC1_IN6	
36	PA2	I/O	ADC1_IN7	
37	PA3	I/O	ADC1_IN8	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN9	
41	PA5	I/O	ADC1_IN10	
42	PA6	I/O	ADC1_IN11	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
43	PA7	I/O	ADC1_IN12	
44	PC4	I/O	ADC1_IN13	
45	PC5	I/O	ADC1_IN14	
46	PB0	I/O	ADC1_IN15	
47	PB1	I/O	ADC1_IN16	
51	VSS	Power	/12 0 1 <u>_</u> 0	
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	QUADSPI_CLK	
64	PE11	I/O	QUADSPI_BK1_NCS	
65	PE12	I/O	QUADSPI_BK1_IO0	
66	PE13	I/O	QUADSPI_BK1_IO1	
67	PE14	I/O	QUADSPI_BK1_IO2	
68	PE15	I/O	QUADSPI_BK1_IO3	
70	PB11	I/O	TIM2_CH4	
71	VSS	Power	_	
72	VDD	Power		
73	PB12	I/O	GPIO_EXTI12	
74	PB13	I/O	I2C2_SCL	IMU_I2C_SCL
75	PB14	I/O	I2C2_SDA	IMU_I2C_SDA
76	PB15 *	I/O	GPIO_Output	
77	PD8 *	I/O	GPIO_Output	IMU_MODE_SEL
79	PD10	I/O	GPIO_EXTI10	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	TIM4_CH3	
86	PD15	I/O	TIM4_CH4	
87	PG2	I/O	SPI1_SCK	
88	PG3	I/O	SPI1_MISO	
89	PG4	I/O	SPI1_MOSI	
90	PG5 *	I/O	GPIO_Input	
91	PG6 *	I/O	GPIO_Output	
92	PG7 *	I/O	GPIO_Output	
94	VSS	Power		
95	VDDIO2	Power		
96	PC6	I/O	TIM3_CH1	

Pin Number LQFP144	Pin Name	Pin Type	Alternate	Label
LQFF144	(function after reset)		Function(s)	
97	PC7	I/O	TIM3_CH2	
98	PC8	I/O	TIM3_CH3	
99	PC9	I/O	TIM3_CH4	
101	PA9	I/O	TIM1_CH2	
102	PA10	I/O	TIM1_CH3	
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13 (JTMS/SWDIO) **	I/O	SYS_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK) **	I/O	SYS_JTCK-SWCLK	
110	PA15 (JTDI) **	I/O	TIM2_CH1	
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	SPI3_MISO	
113	PC12	I/O	SPI3_MOSI	
114	PD0 *	I/O	GPIO_Output	LP_CSN2
115	PD1	I/O	SPI2_SCK	
116	PD2 *	I/O	GPIO_Output	LP_CSN1
117	PD3	I/O	SPI2_MISO	
118	PD4	I/O	SPI2_MOSI	
119	PD5 *	I/O	GPIO_Output	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	GPIO_EXTI6	
123	PD7 *	I/O	GPIO_Output	
124	PG9 *	I/O	GPIO_Output	
125	PG10	I/O	TIM15_CH1	
126	PG11	I/O	TIM15_CH2	
130	VSS	Power		
131	VDDIO2	Power		
135	PB5	I/O	CAN2_RX	
136	PB6	I/O	CAN2_TX	
139	PB8	I/O	CAN1_RX	
140	PB9	I/O	CAN1_TX	
142	PE1	I/O	TIM17_CH1	
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function ** The pin is affected with a peripheral function but no peripheral mode is activated		

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	PDM_INITIAL_WITHOUT_USER_LABELS
Project Folder	C:\Users\Karol\Documents\GitHub\PDM\CODE\PDM_INITIAL_WITHOUT_USER
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_ADC3_Init	ADC3
6	MX_CAN1_Init	CAN1
7	MX_CAN2_Init	CAN2
8	MX_QUADSPI_Init	QUADSPI
9	MX_SPI1_Init	SPI1
10	MX_SPI3_Init	SPI3
11	MX_TIM4_Init	TIM4

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Rank	Function Name	Peripheral Instance Name
12	MX_TIM3_Init	TIM3
13	MX_TIM2_Init	TIM2
14	MX_I2C2_Init	I2C2
15	MX_TIM1_Init	TIM1
16	MX_TIM5_Init	TIM5
17	MX_TIM15_Init	TIM15
18	MX_TIM17_Init	TIM17
19	MX_SPI2_Init	SPI2
20	MX_USB_DEVICE_Init	USB_DEVICE

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496ZGTx
Datasheet	DS11585_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

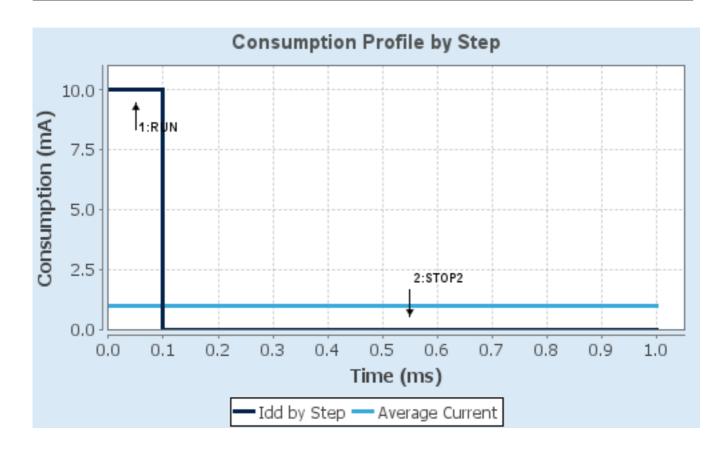
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10 mA	2.69 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	104.04	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1 mA
Battery Life	4 months, 19	Average DMIPS	100.0 DMIPS
	days, 3 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN8: IN8 Single-ended IN9: IN9 Single-ended

IN10: IN10 Single-ended

IN11: IN11 Single-ended IN12: IN12 Single-ended

IN13: IN13 Single-ended

IN14: IN14 Single-ended

IN15: IN15 Single-ended mode: IN16 Single-ended

mode: Temperature Sensor Channel

mode: Vbat Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

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Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 1
Sampling Time 2.5 Cycles
Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

7.2. ADC3

IN6: IN6 Differential IN8: IN8 Single-ended

mode: IN13

7.2.1. Parameter Settings:

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution
Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular ConversionsEnableEnable Regular OversamplingDisableNumber Of Conversion1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 6
Sampling Time 2.5 Cycles
Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

7.3. CAN1

mode: Activated

7.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum 200.0 *

Time Quanta in Bit Segment 1 6 Times *

Time Quanta in Bit Segment 2 1 Time
Time for one Bit 1600 *

Time for one Bit 1600 *

Baud Rate 625000 *

Basic Parameters:

ReSynchronization Jump Width

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

1 Time

7.4. CAN2

mode: Activated

7.4.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum

200.0 *

Time Quanta in Bit Segment 1

8 Times *

Time Quanta in Bit Segment 2

1 Time

Time for one Bit

2000 *

500000 *

ReSynchronization Jump Width 1 Time

Basic Parameters:

Baud Rate

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Disable

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

7.5. I2C2 I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

Custom Timing Disabled
I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Timing 0x10909CEC *

Slave Features:

Analog Filter

Clock No Stretch Mode Disabled
General Call Address Detection Disabled

Enabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

7.6. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.6.1. Parameter Settings:

General Parameters:

Clock Prescaler 255
Fifo Threshold 1

Sample Shifting No Sample Shifting

 Flash Size
 1

 Chip Select High Time
 1 Cycle

 Clock Mode
 Low

 Flash ID
 Flash ID 1

 Dual Flash
 Disabled

7.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value 64

MSI Calibration Value 0

MSI Auto Calibration Enabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

LSE Drive Capability

LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.8. SPI1

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 4 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate)

Baud Rate 40.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

7.9. SPI2

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 4 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 40.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

7.10. SPI3

Mode: Full-Duplex Master 7.10.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 4 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 40.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

7.11. SYS

Timebase Source: SysTick

7.12. TIM1

Channel2: PWM Generation CH2 Channel3: PWM Generation CH3

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

Clear Input:

Clear Input Source Disable

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

7.13. TIM2

Channel4: PWM Generation CH4

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 4294967295
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (32 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

7.14. TIM3

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

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Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.15. TIM4

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.16. TIM5

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 4294967295
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.17. TIM15

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable BRK Polarity High

BRK Sources Configuration

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

7.18. TIM17

mode: Activated

Channel1: PWM Generation CH1

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

Output

No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High

BRK Sources Configuration

Digital Input
 COMP1
 Disable
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.19. USB_OTG_FS

Mode: Device_Only

7.19.1. Parameter Settings:

Speed Full Speed 12MBit/s

Low powerDisabledBattery chargingDisabledLink Power ManagementDisabledUse dedicated end point 1 interruptDisabledVBUS sensingDisabledSignal start of frameDisabled

7.20. USB DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.20.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)

1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)

1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)

512
USBD_SELF_POWERED (Enabled self power)

Enabled

USBD_DEBUG_LEVEL (USBD Debug Level) 0: No debug message

USBD_LPM_ENABLED (Link Power Management) 1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size 2048
USB CDC Tx Buffer Size 2048

7.20.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier) 1155

LANGID_STRING (Language Identifier) English(United States)

MANUFACTURER_STRING (Manufacturer Identifier) STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier) 22336

PRODUCT_STRING (Product Identifier) STM32 Virtual ComPort

CONFIGURATION_STRING (Configuration Identifier)

CDC Config

INTERFACE_STRING (Interface Identifier)

CDC Interface

PDM_	INITIAL_	_WITHOUT_	_USER_	_LABELS	Project
			Con	figuration	Report

* User modified value		

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
ADC1	PC0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN16	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF3	ADC3_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PF4	ADC3_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PF5	ADC3_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PF10	ADC3_IN13	Analog mode	No pull-up and no pull-down	n/a	
CAN1	PB8	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB9	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
CAN2	PB5	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
12C2	PB13	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	IMU_I2C_SCL
	PB14	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	IMU_I2C_SDA
QUADSPI	PE10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	QUADSPI_BK1_	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		NCS			*	
	PE12	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	QUADSPI_BK1_I O3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PG2	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PD1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD3	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
TIM1	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PF6	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM15	PG10	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM17	PE1	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
Single Mapped Signals	PA13 (JTMS/SWDI O)	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC LK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PA15 (JTDI)	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	INFO_LED
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HP_MOS_SEL1
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HP_MOS_SEL2
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HP_MOS_SEL3
	PB12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_MODE_SEL
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LP_CSN2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LP_CSN1
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD6	GPIO_EXTI6	External Interrupt Mode with	No pull-up and no pull-down	n/a	
			Rising edge trigger detection			
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC3	DMA2_Channel5	Peripheral To Memory	Low
TIM3_CH4/UP	DMA1_Channel3	Peripheral To Memory	Low
SPI1_RX	DMA1_Channel2	Peripheral To Memory	Low
SPI1_TX	DMA2_Channel4	Memory To Peripheral	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

ADC3: DMA2_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

TIM3_CH4/UP: DMA1_Channel3 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

SPI1_RX: DMA1_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte

Memory Data Width: Byte

SPI1_TX: DMA2_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *

Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA1 channel1 global interrupt	true	0	0	
DMA1 channel2 global interrupt	true	0	0	
DMA1 channel3 global interrupt	true	0	0	
DMA2 channel4 global interrupt	true	0	0	
DMA2 channel5 global interrupt	true	0	0	
USB OTG FS global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38		unused		
Flash global interrupt		unused		
RCC global interrupt		unused		
ADC1 and ADC2 interrupts		unused		
CAN1 TX interrupt		unused		
CAN1 RX0 interrupt		unused		
CAN1 RX1 interrupt		unused		
CAN1 SCE interrupt		unused		
EXTI line[9:5] interrupts		unused		
TIM1 break interrupt and TIM15 global interrupt		unused		
TIM1 update interrupt and TIM16 global interrupt		unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt		unused		
TIM1 capture compare interrupt		unused		
TIM2 global interrupt		unused		
TIM3 global interrupt		unused		
TIM4 global interrupt		unused		
I2C2 event interrupt	unused			
I2C2 error interrupt	unused			
SPI1 global interrupt	unused			
SPI2 global interrupt		unused		
EXTI line[15:10] interrupts		unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
ADC3 global interrupt		unused	
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
QUADSPI global interrupt	unused		
FPU global interrupt	unused		
CAN2 TX interrupt	unused		
CAN2 RX0 interrupt		unused	
CAN2 RX1 interrupt		unused	
CAN2 SCE interrupt	unused		

8.3.2. NVIC Code generation

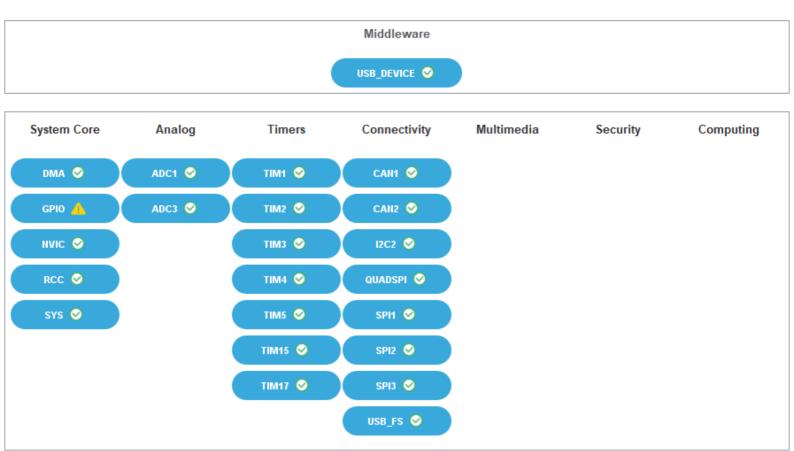
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA2 channel4 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true
USB OTG FS global interrupt	false	true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32l4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32l4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4_svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_stm8_functi

onal-safety-packages.pdf

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pres.pdf

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stm8_software_development_tools.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32-family-overview.pdf

Brochures https://www.st.com/resource/en/brochure/brstm32ulp.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32l4.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf

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Certifications certificate_stm32l4.pdf

Application Notes https://www.st.com/resource/en/application_note/an1181-electrostatic-

discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

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recommendations-and-package-information-for-leadfree-ecopack-mcus-

and-mpus-stmicroelectronics.pdf

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design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf

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waveform-generation-using-the-dac-in-stm32-products-

stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3154-can-protocol-

used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application note/an3155-usart-protocol-

used-in-the-stm32-bootloader-stmicroelectronics.pdf

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protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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number-of-touchkeys-for-touch-sensing-applications-on-mcus-

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- Application Notes https://www.st.com/resource/en/application_note/an4555-getting-started-with-stm32l4-series-and-stm32l4-series-hardware-development-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4612-migrating-from-stm32l1-series-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4616-migrating-from-stm32f401-and-stm32f411-lines-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
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