**Investigation into MTL Signals reaching values up to 10kV above the set limit.**

Bradley Elvy, ICRH  
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Abstract – A problem causing the values on MTLA1 to reach up to 10kV above the limit level has been identified. The control system has been analysed to work out what could be causing an issue. Undocumented hardware has been found, analysed and recorded for future uses. This hardware has been tested to prove its functionality. The main problem has not persisted but less severe cases of the MTL values reaching up to 3kV above the limit level have been seen. This could be due to response delays and should be further investigated.

1. Problem

“please find below an example of the ALM misbehaviour:

The Vmax limits are set to 30kV, however the A1 MTL Vmax (green trace, top figure) is clearly not limited reaching dangerously high voltages; at the same time B1 Vmax is limited at 30kV (green trace, bottom figure), i.e. the A vs B Vmax OR-ing logic clearly doesn’t work.” – 26/09/19 Igor Monakhov

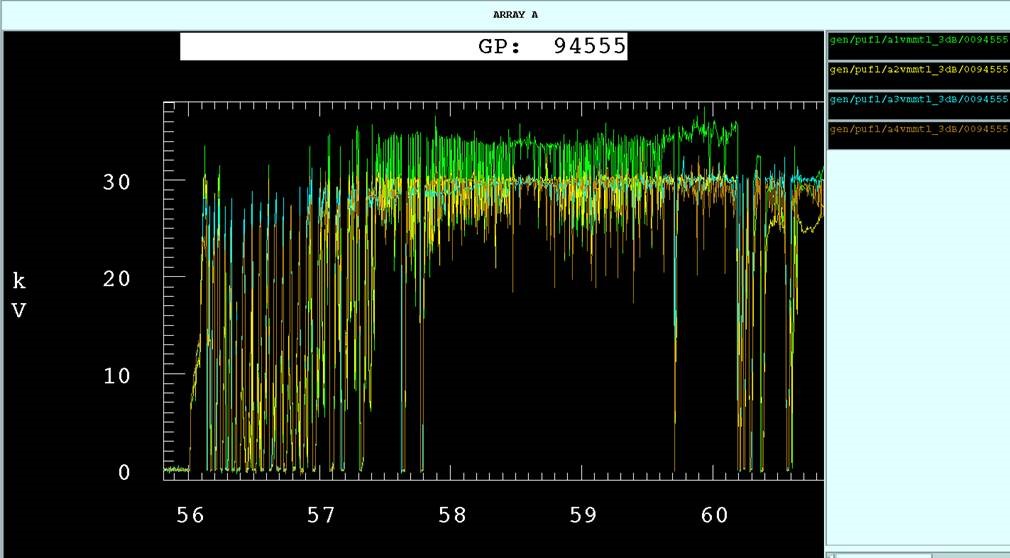


Figure 1 Voltage versus time (s) during a pulse, showing the A1 MTL signal much higher than the limit value.

1. ALM Pre-Existing ORinf Circuit

The ALM was physically removed during a non-operations period, where an undocumented PCB was found attached to the ALM. The circuit was analysed and thought to be an ORing circuit which should stop the problem shown in figure 1.

The PCB’s were traced back to Trevor?? Blackman, and the design was found. These are shown in figure 2 along with and image of the PCB on the ALM in figure 3.

The ORing circuit design was analysed and found to take 4 MTL signals. VFMTL and VRMTL for A1 and B1. The forward and reflected signals of each MTL are averaged and then OR’d together so that the highest signal passes through to the LIM\_MOD card (MOD3).

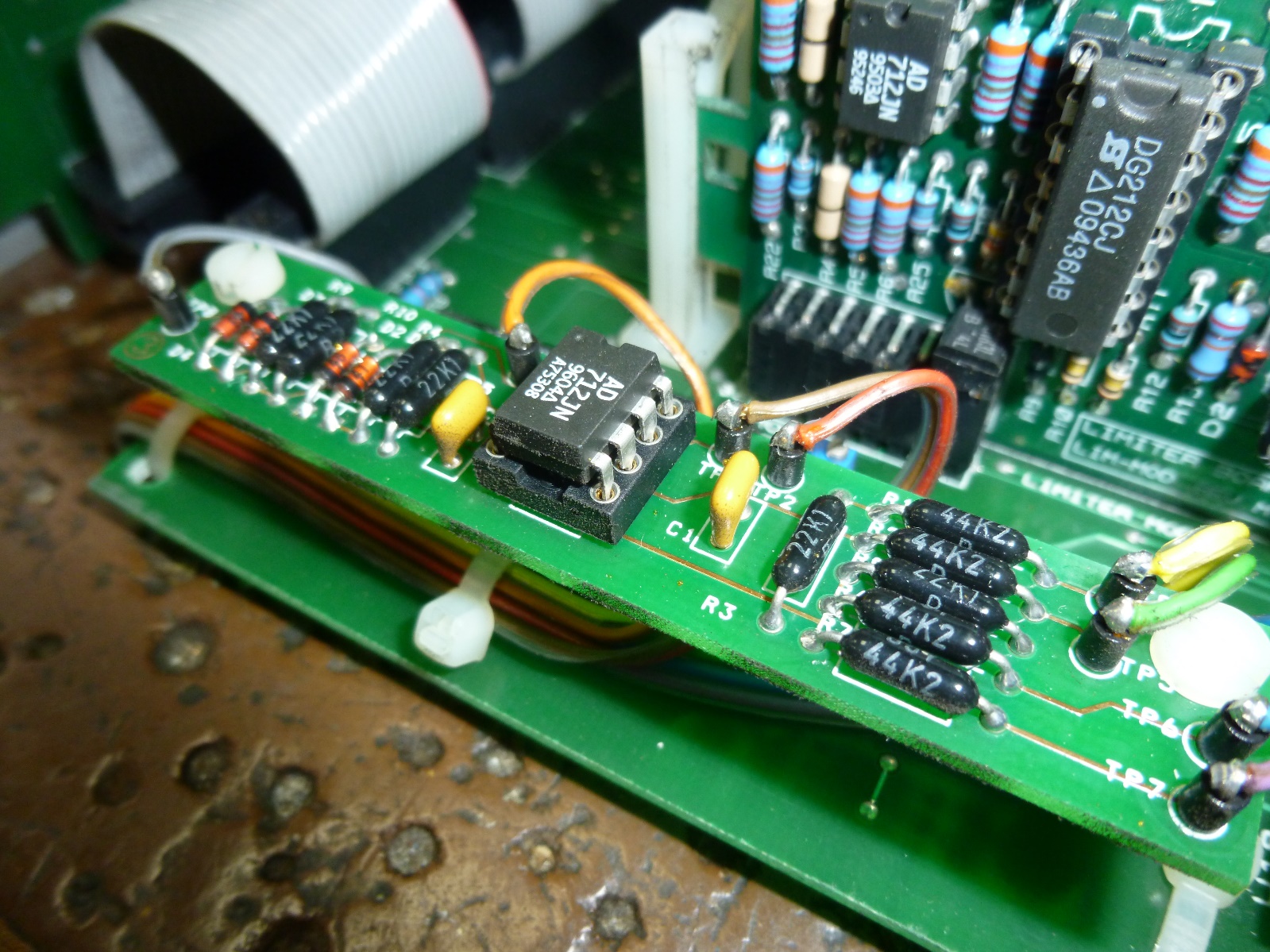


Figure 3 ALM ORing PCB

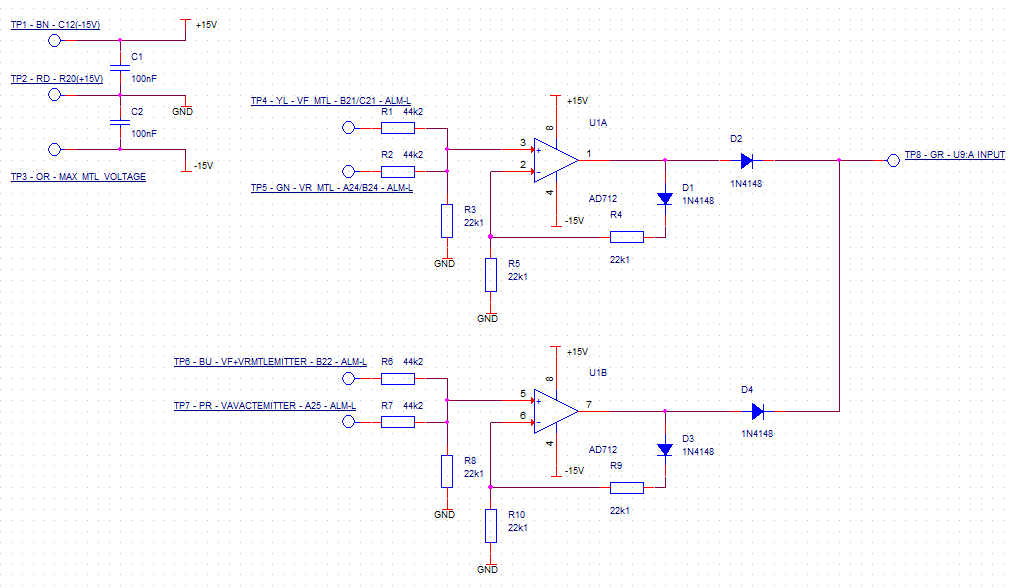


Figure 2 ALM ORing circuit diagram.

The PCB slots into the ALM using the previously designed SUMing circuit as a buffer, shown in the figures below.

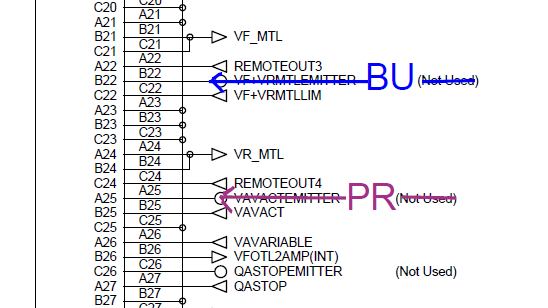
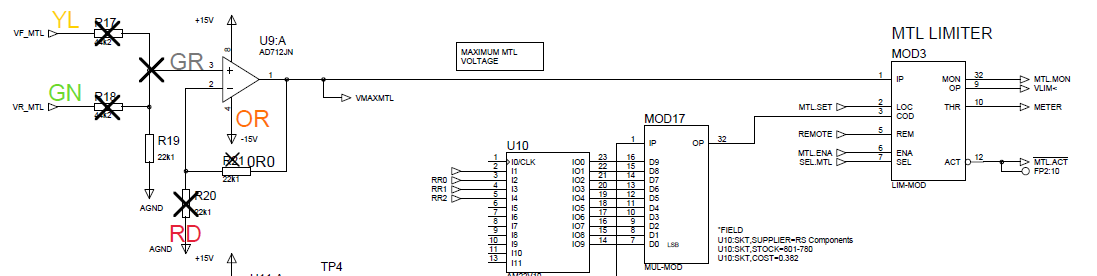
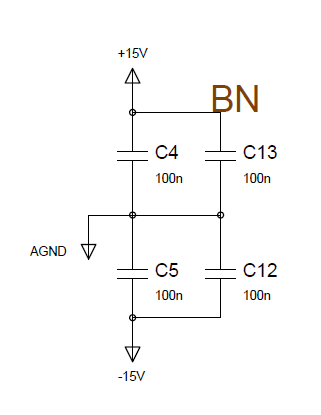
INSERT PDF OF SUMING CIRCUIT AND WHERE THE CONNECTIONS TO THE PCB ARE.

Figure 6 Original Schematic showing where +15V is supplied to the additional board (page 3/7).

Figure 5 Original ALM schematic ALM-L Connector with added connections (page 6/7).

Figure 4 Original ALM Schematic marked with the additional board’s modifications (page 3/7).

1. Quick Fix

Some joints were found to be poor and could have caused the circuit to malfunction. These joints were resoldered and the issue has not occurred since. It is not certain whether this is because of the new soldering or whether the conditions have not been appropriate for the issue to occur.

1. Testing the board and system

Although the error has not been seen on the same scale, smaller peaks around 3kV above the limit have been observed. This leads to an investigation on whether each ALM is functioning correctly and why they could be performing this way.

The initial test is to confirm that each ALM correctly OR’s the summation of the forward and reflected signal from the corresponding A and B MTL. This is done with the following setup.

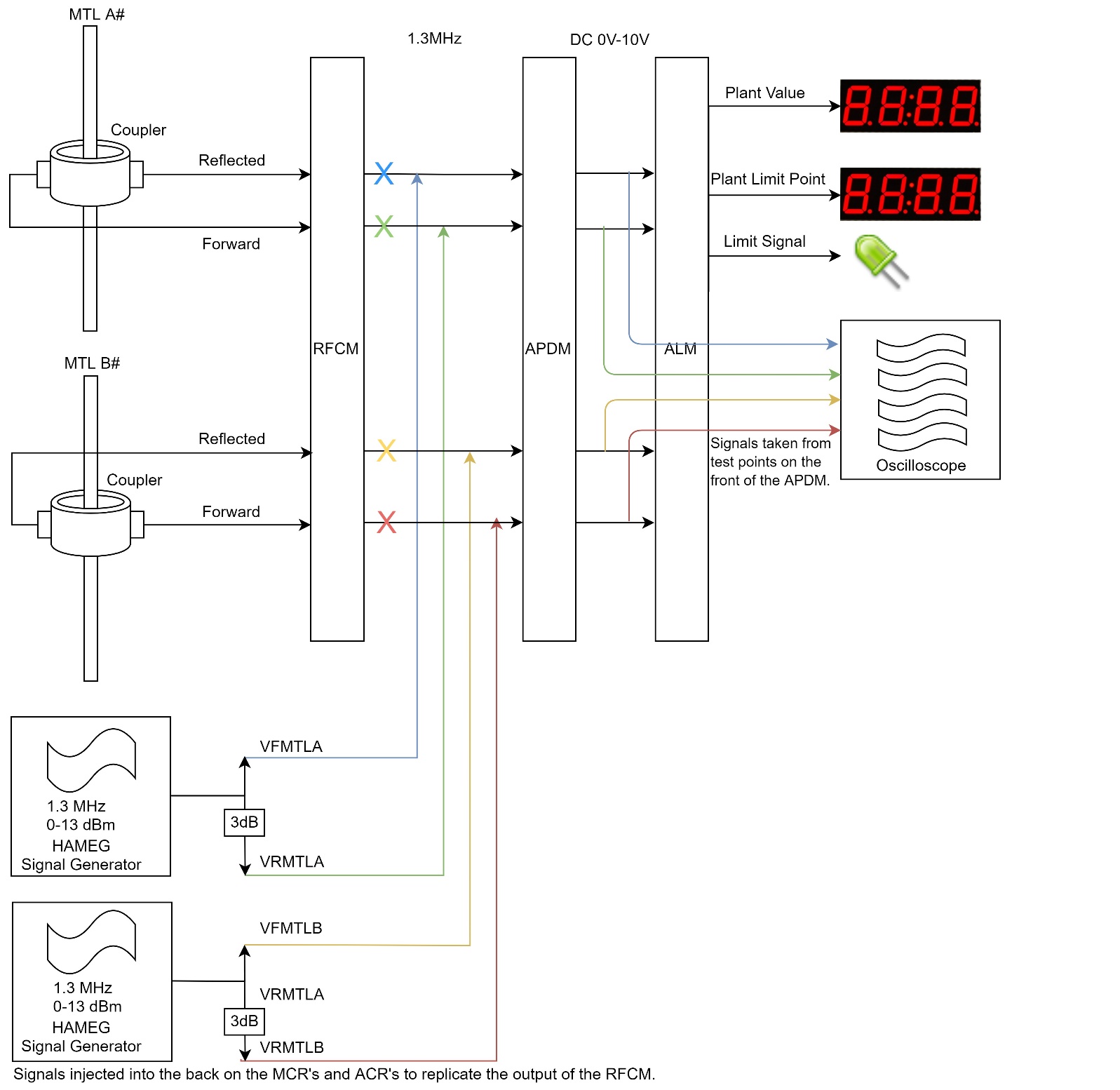


Figure 4 ALM ORing circuit test setup.

Each ALM has been tested with 2dBm intervals, from 2dBm to 8dBm (approx. 0.28V – 0.56V). The points at which the signals are limited were then tested for each MTL whilst the corresponding MTL maintained a reduced signal level to not interfere.

1. Results

Each ALM performed similarly. Each ALM triggered limiting at around 11.1-11.3 dBm or 0.8V. The ALM limit when MTLA rises does not seem to depend on the value on MTLB and vice versa. This all suggests that the ALM’s are functioning correctly.

It is worth noting that, although the function is correct, it is not precise and the signals in this test were unstable. The limit values were difficult to examine as the output signals fluctuated, leaving the limit signal turning on and off.

1. What’s next?

The potential cause thought to be most likely for the MTL values rising roughly 3kV above the limit level is the control systems response delay. An investigation could be conducted to measure the time delay on the system and therefore suggest whether the errors are linked to fast changing MTL values caused by rapidly fluctuating plasmas.

1. Appendix
   1. Glossary
   2. Test Results