Total No. of Questions—8]   [Total No. of Printed Pages—3

Seat
No.

[4757]-1083

S.E. (I.T.) (First Semester) EXAMINATION, 2015

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours   Maximum Marks : 50

N.B. :— (*i*)   Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**
              and Q. No. **5** *or* Q. No. **6** and Q. No. **7** *or* Q. No. **8**.

       (*ii*)   Neat diagrams must be drawn wherever necessary.

       (*iii*) Figures to the right indicate full marks.

       (*iv*)   Assume suitable data, if necessary.

1.   (*a*)   Represent the following decimal numbers in single precision
             floating point format :   [6]

             (*i*)   255.5

             (*ii*) 110.65

     (*b*)   What do you mean by open collector output ? Explain
             with suitable circuit diagram. What is the advantage of this
             output ?   [6]

                                                                   P.T.O.

2. (*a*)   Perform 2's complement arithmetics of :   [6]

(*i*) $(7)_{10} - (11)_{10}$

(*ii*) $(-7)_{10} - (11)_{10}$

(*iii*) $(-7)_{10} + (11)_{10}$

(*b*)   Draw suitable circuit diagram and explain the drawback of WIRED_OR TTL GATE ?   [6]

3. (*a*)   What is race around condition ? Explain with the help of timing diagram. How is it removed in basic flip-flop circuit ? [6]

(*b*)   Design a sequence generator using shift register and decoder circuit to generate the sequence ......1101011...... .   [7]

Or

4. (*a*)   How will you convert the basic SR-flip-flop (SR-FF) into JK-flip-flop ?   [6]

(*b*)   Design a MOD-11 counter using IC7490. Show states with the help of timing diagram.   [7]

5. (*a*)   Draw the basic structure FPGA. Explain its feature in brief. [6]

(*b*)   Implement the following function using programmable logic device :   [6]

(*i*)   F1 $= \Sigma m$ (0, 3, 4, 7)

(*ii*) F2 $= \Sigma m$ (1, 2, 5, 7)

6. (*a*) Draw the basic structure of CPLD. Explain its features in brief. [6]

(*b*) Design a BCD to Excess-3 code convertor using suitable programmable logic device. [6]

7. (*a*) State and explain different data types supported by VHDL. [6]

(*b*) Write features of VHDL. Explain entity architecture declaration for 2 bit NOR and AND gate. [7]

Or

8. (*a*) State and discuss different types of operators used in VHDL. Give precedence of these operators. [6]

(*b*) Describe different modelling styles of VHDL with suitable example. [7]