同济大学计算机系

数字逻辑课程实验报告

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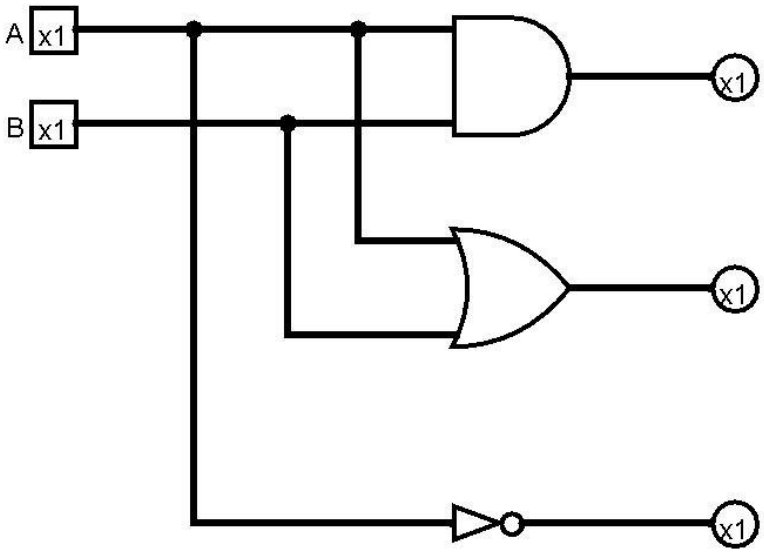
一、实验内容

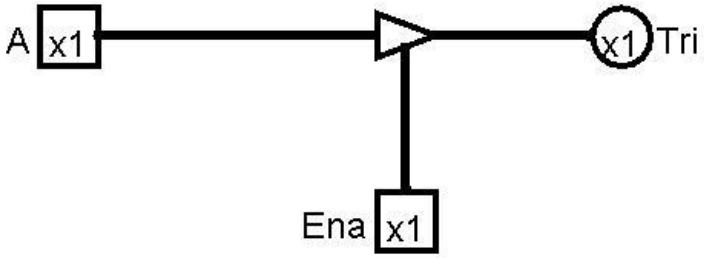
练习使用 Verlog HDL 语言，采用三种不同的描述方式设计基本门电路，并实现数据扩展。

二、硬件逻辑图

1. 与门，或门，非门电路图：



2. 三态门电路图：



三、模块建模

1. 与门，或门，非门

（1） 结构型描述

```
module logic_gates_1(iA,iB,oAnd,oOr,oNot);
    input iA, iB;
    output oAnd,oOr,oNot;
    and and_inst(oAnd, iA,iB);
    or or_inst(oOr, iA,iB);
    not not_inst(oNot, iA);
endmodule
```

（2） 数据流型描述

```
module logic_gates_2(iA,iB,oAnd,oOr,oNot);
    input iA, iB;
    output oAnd,oOr,oNot;
    assign oAnd = iA & iB;
    assign oOr = iA | iB;
    assign oNot = ~iA;
endmodule
```

（3） 行为描述

```
module logic_gates_3(iA,iB,oAnd,oOr,oNot);
    input iA, iB;
    output oAnd,oOr,oNot;
    reg oAnd, oOr, oNot;
    always @ (*)
    begin
        oAnd=iA & iB;
        oOr=iA| iB;
        oNot=~iA;
    end
endmodule
```

2. 三态门

```
module three_state_gates(iA,iEna,oTri);
    input iA;
    input iEna;
    output oTri;
assign oTri = (iEna==1)? iA:'bz;
endmodule
```

3. 数字扩展

```
module extend #(parameter WIDTH = 16)(
    input [WIDTH-1:0] a,
    input sext,
    output [31:0] b
);
    assign b=sext? {{(32-WIDTH){a[WIDTH-1]}},a} :
{{(32-WIDTH){1'b0}},a};
endmodule
```

四、测试模块建模

（要求列写各建模模块的 test bench 模块代码）

1. 与门，或门，非门

（1） Logic_gates_1_tb

```
`timescale 1ns / 1ps

module logic_gates_tb;
    reg iA;
    reg iB;
    wire oAnd;
    wire oNot;
    wire oOr;

    initial
    begin
        iA=0;
        #40 iA=1;
        #40 iA=0;
        #40 iA=1;
        #40 iA=0;
    end

    initial
    begin
        iB=0;
        #40 iB=0;
        #40 iB=1;
        #40 iB=1;
        #40 iB=0;
    end

    logic_gates_1
    logic_gates_inst(
        .iA(iA),
        .iB(iB),
        .oAnd(oAnd),
        .oOr(oOr),
        .oNot(oNot)
        );
endmodule
```

（2） Logic_gates_2_tb

```
`timescale 1ns / 1ps
```

```
module logic_gates_tb;
    reg iA;
    reg iB;
    wire oAnd;
    wire oNot;
    wire oOr;

    initial
    begin
        iA=0;
        #40 iA=1;
        #40 iA=0;
        #40 iA=1;
        #40 iA=0;
    end

    initial
    begin
        iB=0;
        #40 iB=0;
        #40 iB=1;
        #40 iB=1;
        #40 iB=0;
    end

    logic_gates_2
    logic_gates_inst(
        .iA(iA),
        .iB(iB),
        .oAnd(oAnd),
        .oOr(oOr),
        .oNot(oNot)
        );
endmodule
```

（3） Logic_gates_3_tb

```
`timescale 1ns / 1ps

module logic_gates_tb;
    reg iA;
    reg iB;
    wire oAnd;
    wire oNot;
    wire oOr;
```

```
    initial
    begin
        iA=0;
        #40 iA=1;
        #40 iA=0;
        #40 iA=1;
        #40 iA=0;
    end

    initial
    begin
        iB=0;
        #40 iB=0;
        #40 iB=1;
        #40 iB=1;
        #40 iB=0;
    end

    logic_gates_1
    logic_gates_inst(
        .iA(iA),
        .iB(iB),
        .oAnd(oAnd),
        .oOr(oOr),
        .oNot(oNot)
        );
endmodule
```

2. 三态门 testbench

```
`timescale 1ns / 1ps

 module three_state_gates_tb;
    reg iA;
    reg iEna;
    wire oTriState;

    three_state_gates uut (
.iA(iA),
.iEna(iEna),
.oTri(oTriState)
);
initial
begin
iA = 0;
#40 iA = 1;
```

```
 #40 iA = 0;
 #40 iA = 1;
end
initial
begin
 iEna = 1;
 #20 iEna = 0;
 #40 iEna= 1;
 #20 iEna = 0;
end
endmodule
```

3. 数据扩展 testbench

```
`timescale 1ns / 1ps
module extend_tb;
    reg [15:0] a;
    reg sext;
    wire [31:0] b;
// Instantiate the Unit Under Test (UUT)
    extend uut (.a(a),.sext(sext),.b(b));
    initial
    begin
        // Initialize Inputs
        a = 0;
        sext = 0;
        // Wait 100 ns for global reset to finish
        #100;
        // Add stimulus here
        sext = 1;
        a = 16'h0000;
        #100;
        sext = 0;
        a = 16'h8000;
        #100;
        sext = 1;
        a = 16'h8000;
        #100;
        sext = 0;
        a = 16'hffff;
        #100;
        sext = 1;
        a = 16'hffff;
        #100;
    end
endmodule
```

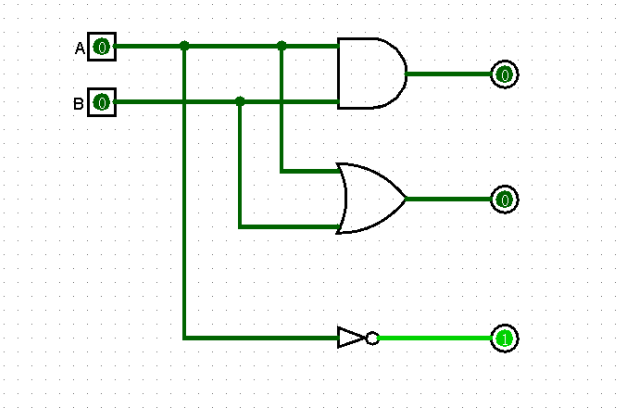
五、实验结果

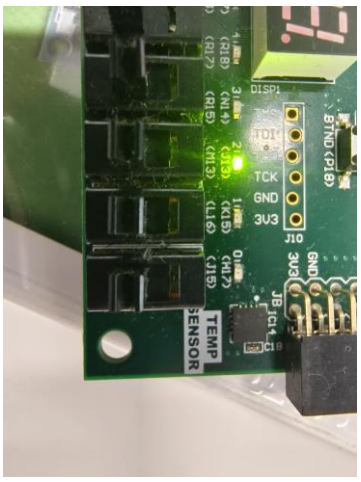
（该部分可截图说明，要求 logisim 逻辑验证图、modelsim 仿真波形图、以及下板后的实验结果贴图（实验步骤中没有下板要求的实验，不需要下板贴图））

1. 与门，或门，非门实验

[1] logisim 逻辑验证图与下板结果

（1）

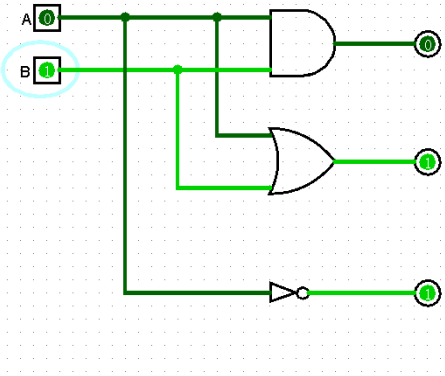


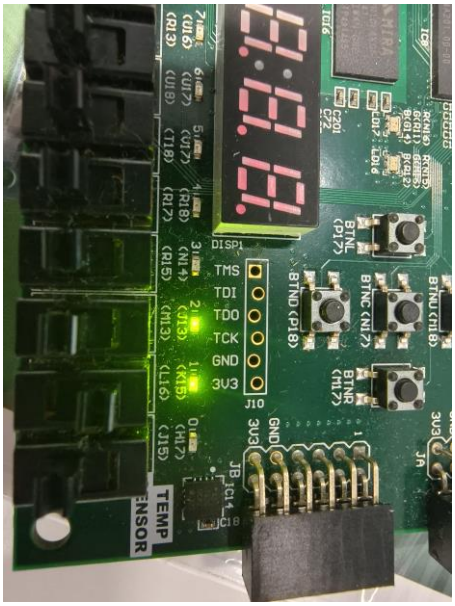


$A = 0, B = 0;$

$A + B = 0, A * B = 0, \overline{A} = 1$

（2）

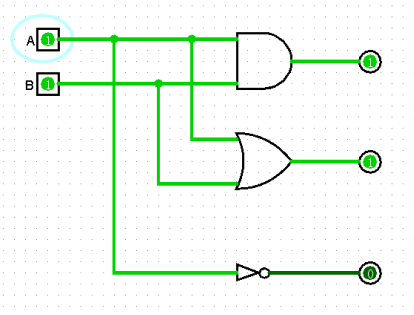


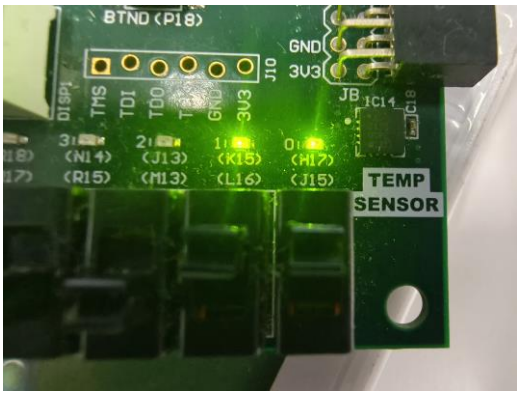


$A = 0, B = 1;$

$A + B = 1, A * B = 0, \overline{A} = 0$

（3）

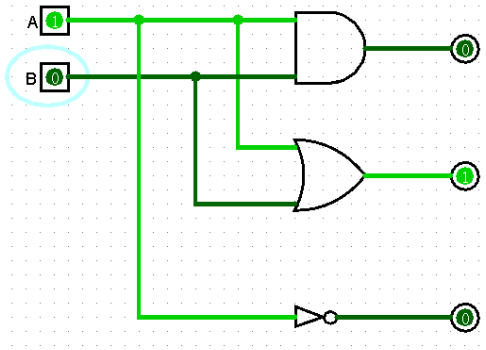


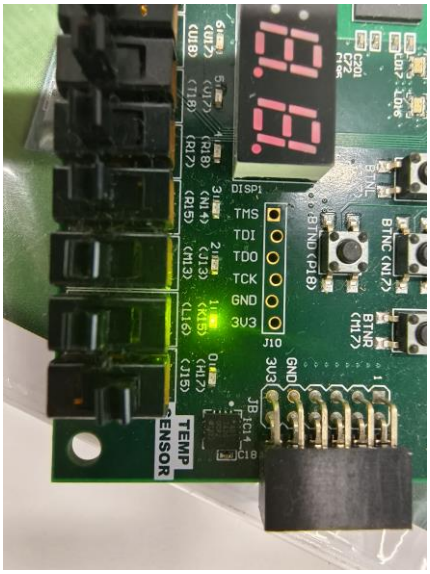


$A=1, B=1;$

$A+B=1, A*B=1, \bar{A}=0$

（4）

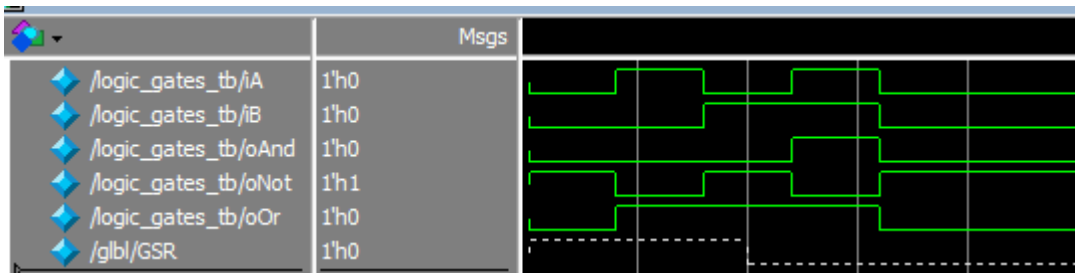




$A=1, B=0;$

$A+B=1, A*B=0, \bar{A}=0$

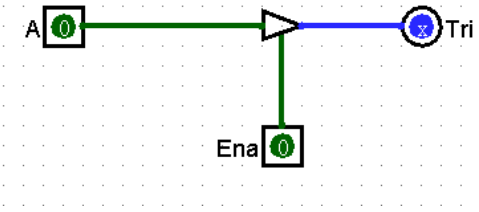
[2]modelsim 仿真波形图



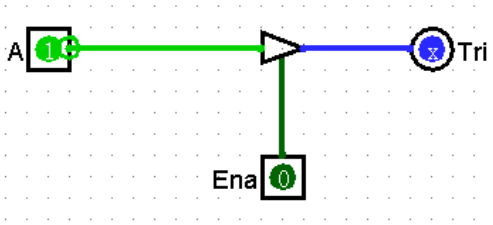
2. 三态门实验

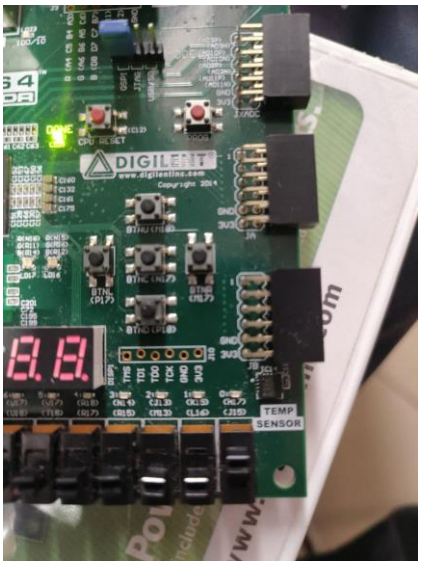
[1] logisim 逻辑验证图与下板结果

（1）

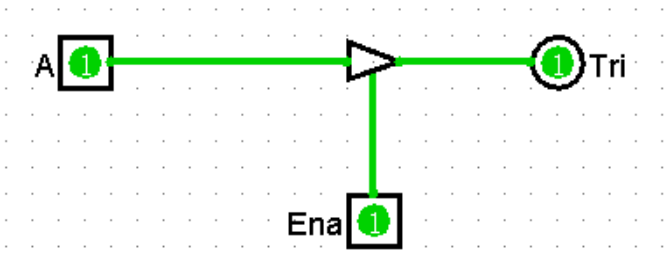


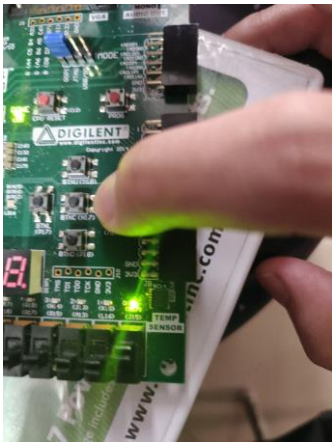
（2）



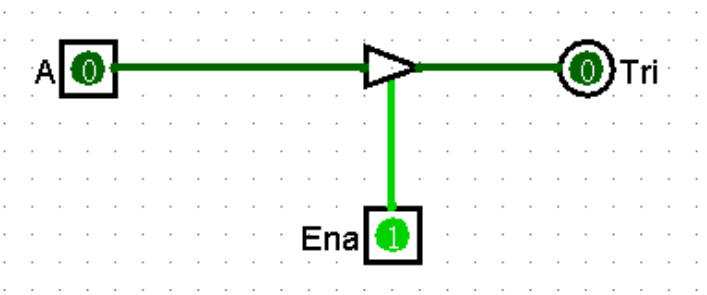


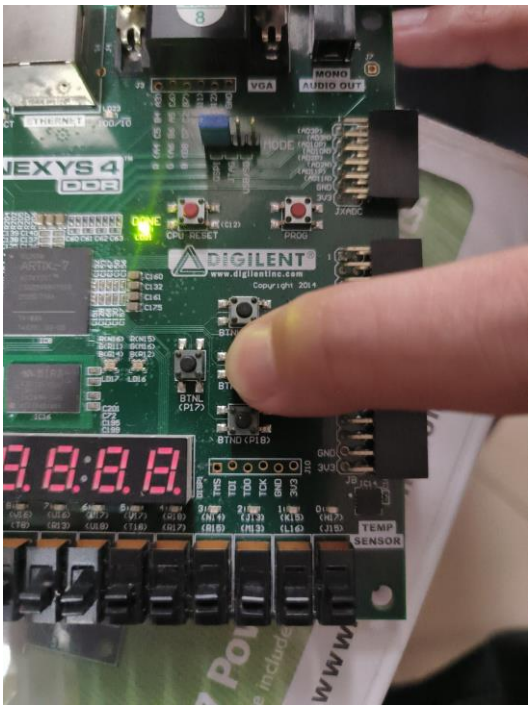
（3）





（4）





[2]仿真波形图

3. 数据扩展实验

[1]仿真波形图