同济大学计算机系

数字逻辑课程实验报告

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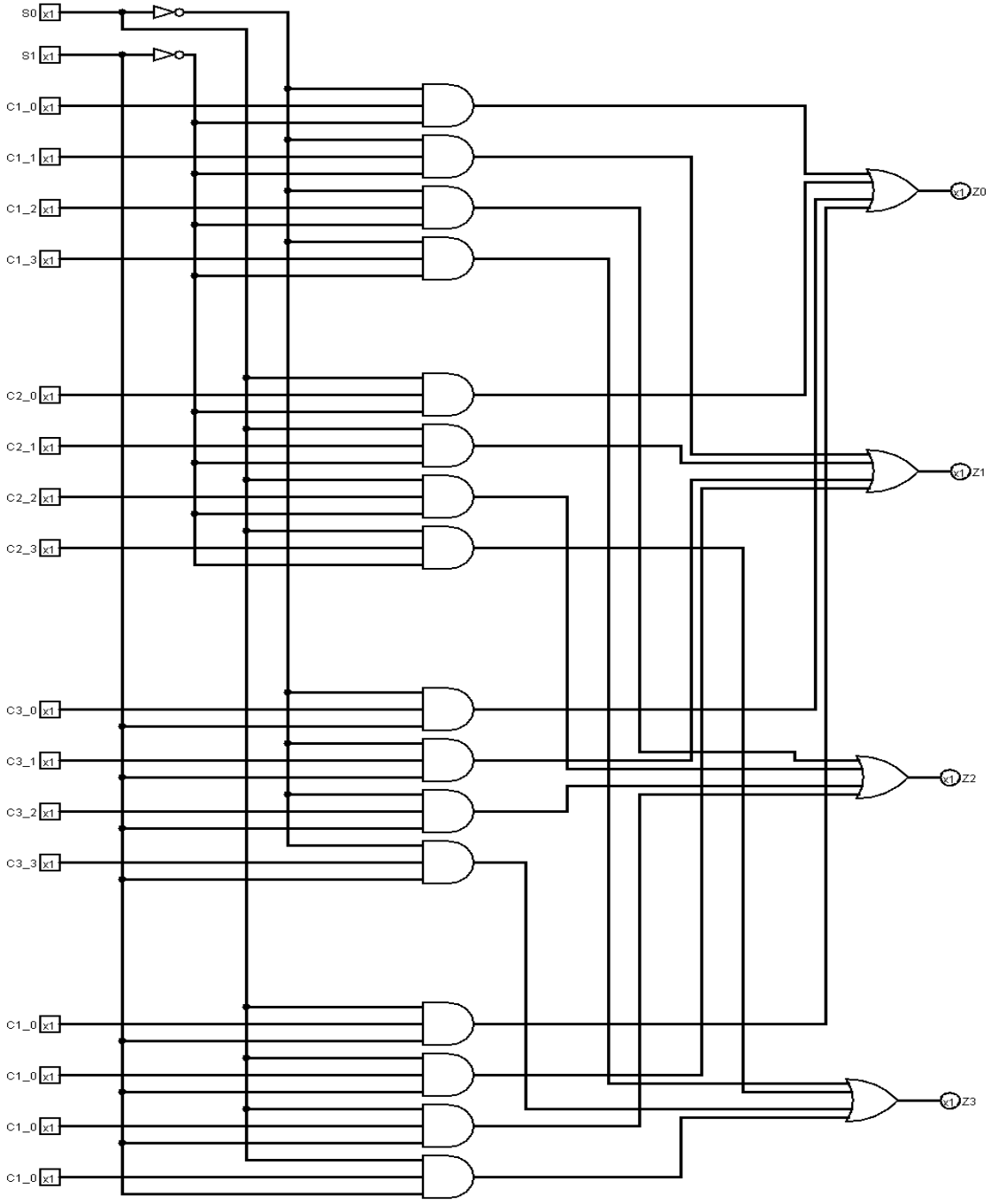
一、实验内容

本次实验将使用 Verilog HDL 语言实现数据选择器和数据分配器的设计和仿真。
实验包括三个部分：数据选择器，数据分配器，8路数据传输实验

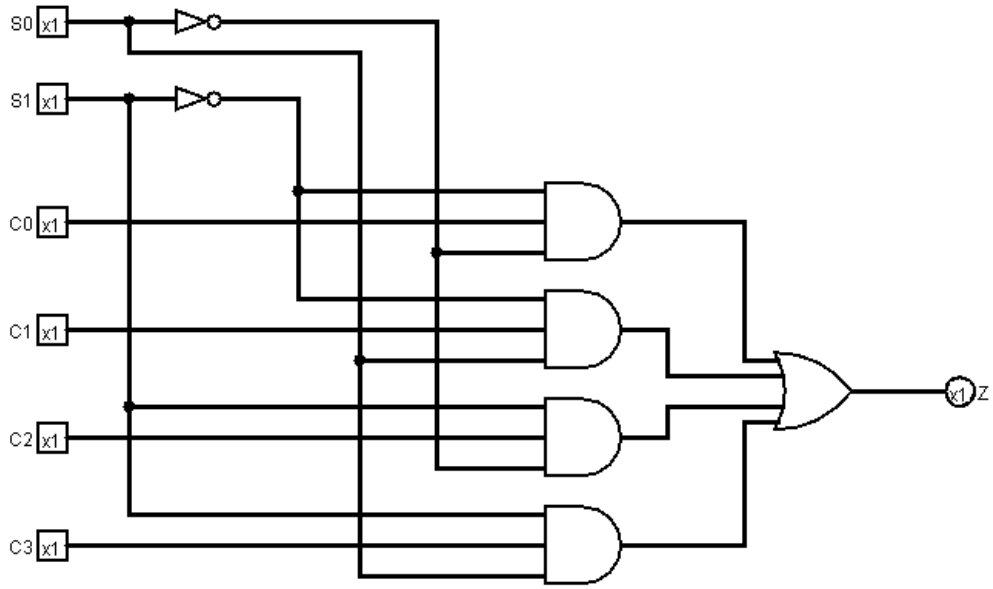
二、硬件逻辑图

（1） 数据选择器实验

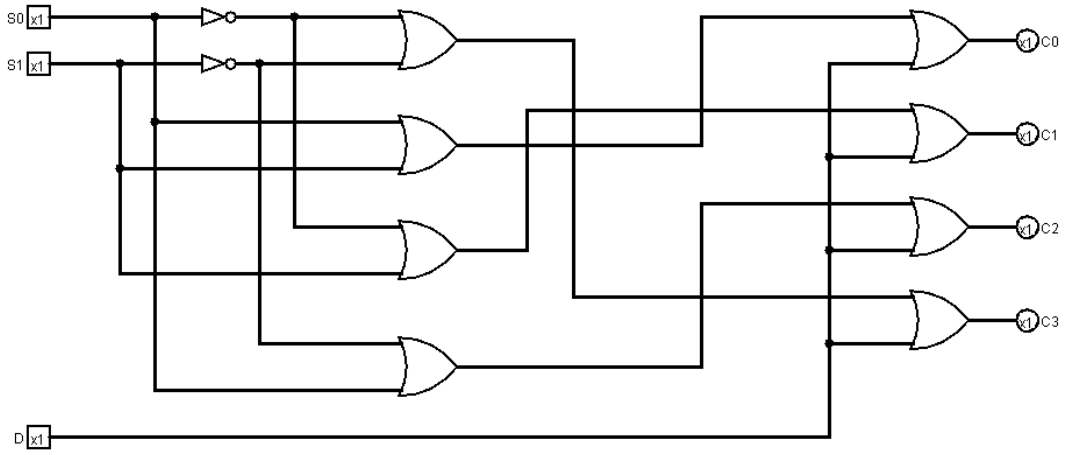
<1>4 个 4bit 数据的选择



<2>4 个 4bit 数据选择



（2） 数据分配器实验



三、模块建模

（1） 数据选择器实验

```
module selector41(
    input [3:0]iC0,
    input [3:0]iC1,
    input [3:0]iC2,
    input [3:0]iC3,
    input iS1,
    input iS0,
    output [3:0]oZ
    );

    assign oZ[0]=(~iS0&&~iS1)?iC0[0]:
                 (iS0&&~iS1)?iC1[0]:
```

```
                (~iS0&&iS1)?iC2[0]:iC3[0];

    assign oZ[1]=(~iS0&&~iS1)?iC0[1]:
                (iS0&&~iS1)?iC1[1]:
                (~iS0&&iS1)?iC2[1]:iC3[1];

    assign oZ[2]=(~iS0&&~iS1)?iC0[2]:
                (iS0&&~iS1)?iC1[2]:
                (~iS0&&iS1)?iC2[2]:iC3[2];

    assign oZ[3]=(~iS0&&~iS1)?iC0[3]:
                (iS0&&~iS1)?iC1[3]:
                (~iS0&&iS1)?iC2[3]:iC3[3];
endmodule
```

（2） 数据分配器实验

```
module de_selector14(
    input iC,
    input iS1,
    input iS0,
    output oZ0,
    output oZ1,
    output oZ2,
    output oZ3
    );
    or(oZ0,iS1,iS0,iC);
    or(oZ1,iS1,~iS0,iC);
    or(oZ2,~iS1,iS0,iC);
    or(oZ3,~iS1,~iS0,iC);
endmodule
```

（3） 8 路数据传输实验

```
module selector81(
    input iC0,
    input iC1,
    input iC2,
    input iC3,
    input iC4,
    input iC5,
    input iC6,
    input iC7,
    input A,
    input B,
    input C,
    output oZ
    );
```

```
    assign oZ = (~A && ~B && ~C)? iC0:
            (~A && ~B && C)? iC1:
            (~A && B && ~C)? iC2:
            (~A && B && C)? iC3:
            (A && ~B && ~C)? iC4:
            (A && ~B && C)? iC5:
            (A && A && ~C)? iC6:iC7;

endmodule

module de_selector18(
    input iC,
    input A,
    input B,
    input C,
    output oZ0,
    output oZ1,
    output oZ2,
    output oZ3,
    output oZ4,
    output oZ5,
    output oZ6,
    output oZ7
    );

    or(oZ0,A,B,C,iC);
    or(oZ1,A,B,~C,iC);
    or(oZ2,A,~B,C,iC);
    or(oZ3,A,~B,~C,iC);
    or(oZ4,~A,B,C,iC);
    or(oZ5,~A,B,~C,iC);
    or(oZ6,~A,~B,C,iC);
    or(oZ7,~A,~B,~C,iC);

endmodule

module transmission8(
    input[7:0]iData,
    input A,B,C,
    output [7:0] oData
    );
    wire oTmp;
```

```
    selector81
ins_sel(iData[0],iData[1],iData[2],iData[3],iData[3],iData[5],iData
[6],iData[7],A,B,C,oTmp);
    de_selector18
ins_de(oTmp,A,B,C,oData[0],oData[1],oData[2],oData[3],oData[4],oDat
a[5],oData[6],oData[7]);

endmodule
```

四、测试模块建模

（1） 数据选择器实验

```
module selector41_tb;
    reg [3:0] iC0;
    reg [3:0] iC1;
    reg [3:0] iC2;
    reg [3:0] iC3;
    reg iS1;
    reg iS0;
    wire [3:0]oZ;
    parameter size=4;

    selector41 selector(iC0,iC1,iC2,iC3,iS1,iS0,oZ);
    initial begin
        iS0 = 0;
        #120 iS0 = 1;
        #120 iS0 = 0;
        #120 iS0 = 1;
    end

    initial begin
        iS1 = 0;
        #120 iS1 = 0;
        #120 iS1 = 1;
        #120 iS1 = 1;
    end

    initial
    begin
        repeat(size)
        begin
            iC0 = 4'b0001;
            iC1 = 4'b0110;
            iC2 = 4'b0011;
```

```
            iC3 = 4'b1111;

            #40 iC0 = 4'b1001;
            iC1 = 4'b0111;
            iC2 = 4'b0011;
            iC3 = 4'b1101;

            #40 iC0 = 4'b1101;
            iC1 = 4'b0111;
            iC2 = 4'b1111;
            iC3 = 4'b1100;
        end
    end

endmodule
```

（2） 数据分配器实验

```
module de_selector14_tb;
    reg iC;
    reg iS1;
    reg iS0;
    wire oZ0,oZ1,oZ2,oZ3;
    parameter size=4;

    de_selector14 ins(iC,iS1,iS0,oZ0,oZ1,oZ2,oZ3);
    initial begin
        iS0 = 0;
        #120 iS0 = 1;
        #120 iS0 = 0;
        #120 iS0 = 1;
    end

    initial begin
        iS1 = 0;
        #120 iS1 = 0;
        #120 iS1 = 1;
        #120 iS1 = 1;
    end

    initial begin
        iC = 0;
        #60 iC = 1;
        #60 iC = 0;
        #60 iC = 1;
        #60 iC = 0;
```

```
        #60 iC = 1;
        #60 iC = 0;
        #60 iC = 1;
    end

endmodule
```

（3） 8 路数据传输实验

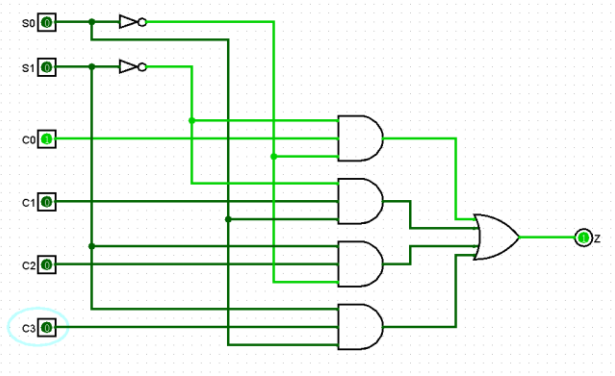
```
module transmission8_tb;
    reg [7:0]iData;
    wire [7:0]oData;
    reg A;
    reg B;
    reg C;

    transmission8 ins(iData,A,B,C,oData);

    initial begin
        A = 0;
        #40 A = 0;
        #40 A = 0;
        #40 A = 0;
        #40 A = 1;
        #40 A = 1;
        #40 A = 1;
        #40 A = 1;
    end

    initial begin
        B = 0;
        #40 B = 0;
        #40 B = 1;
        #40 B = 1;
        #40 B = 0;
        #40 B = 0;
        #40 B = 1;
        #40 B = 1;
    end

    initial begin
        C = 0;
        #40 C = 1;
        #40 C = 0;
        #40 C = 1;
        #40 C = 0;
```

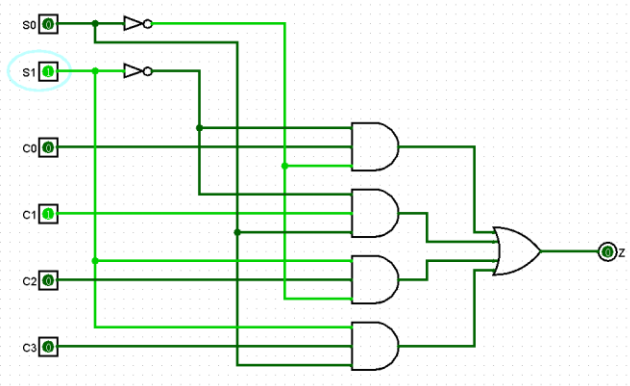
```
        #40 C = 1;
        #40 C = 0;
        #40 C = 1;
    end


    initial
    begin
        iData[0] = 0;
        iData[1] = 0;
        iData[2] = 0;
        iData[3] = 0;
        iData[4] = 0;
        iData[5] = 0;
        iData[6] = 0;
        iData[7] = 0;
    end

endmodule
```

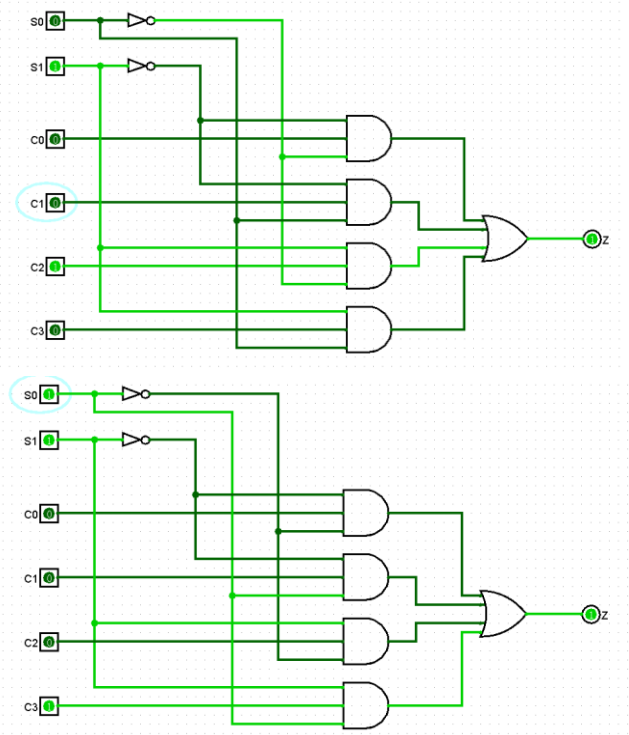
五、实验结果

（1） 数据选择器

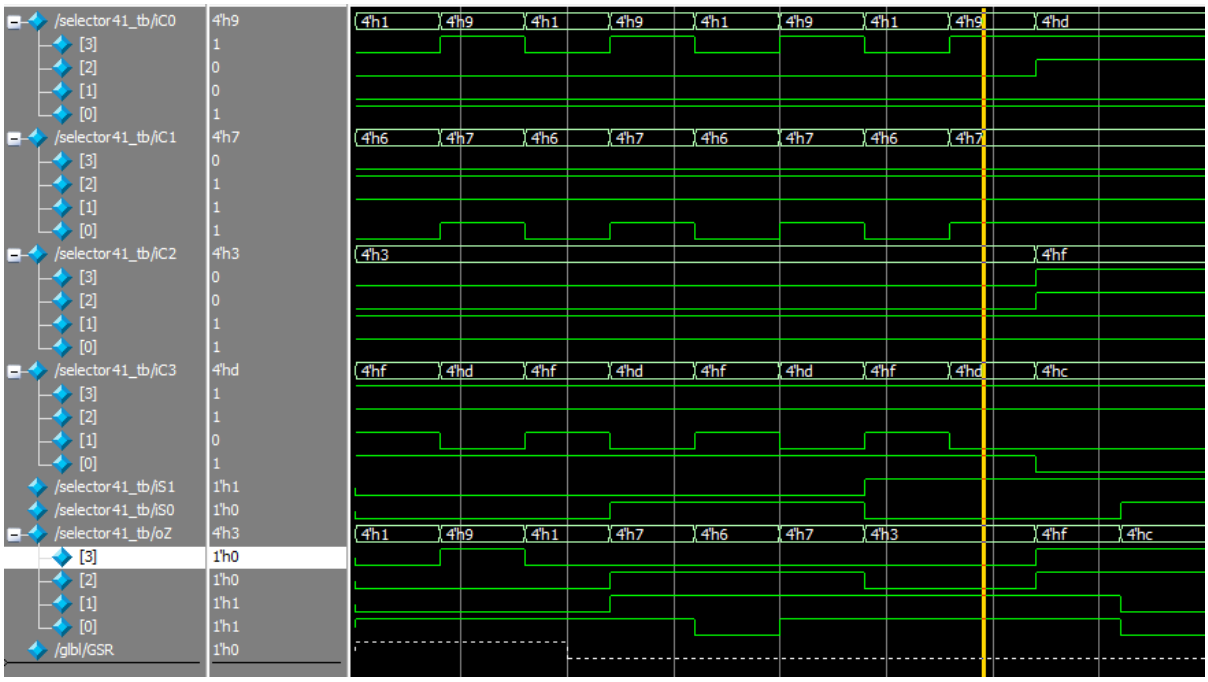
<1>logisim 逻辑验证图



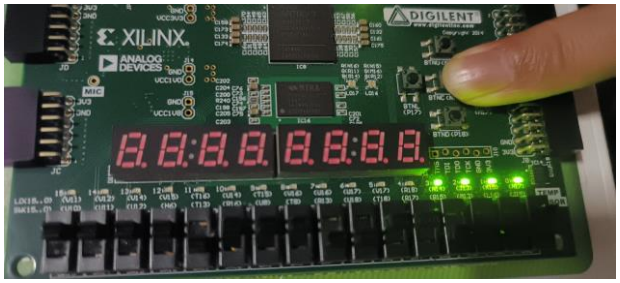




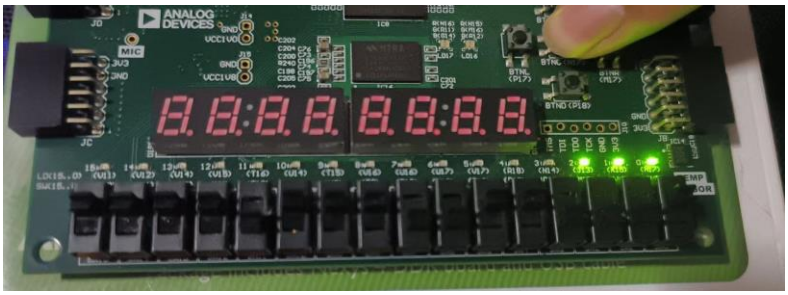
<2>modelsim 仿真图



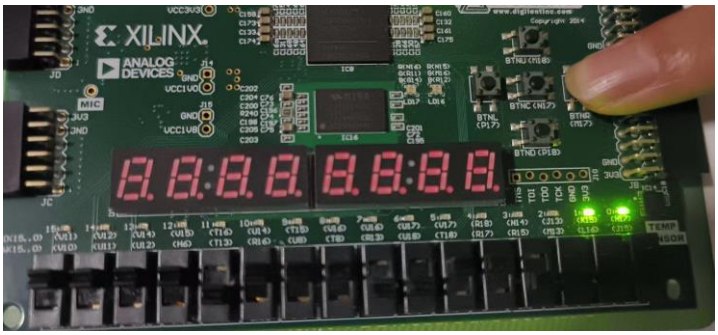
<3>下板结果图，预设每个 4bit 输入各不相同



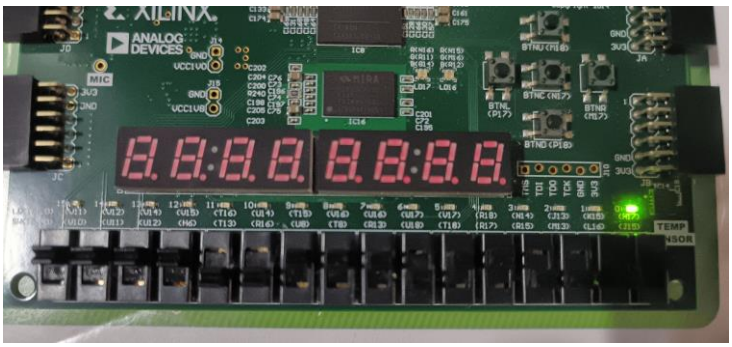
$S_0=1, S_1=1$，此时对应 C3 的输入值



$S_0=0, S_1=1$，此时对应 C2 的输入值



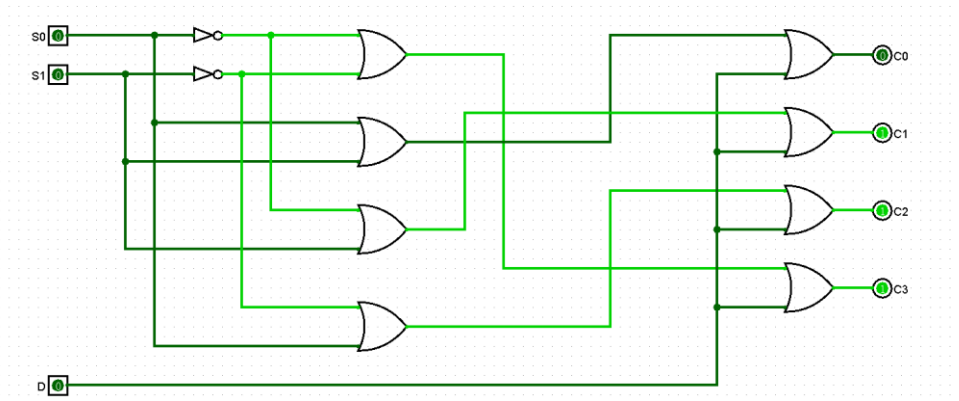
$S_0=1, S_1=0$，此时对应 C1 的输入值

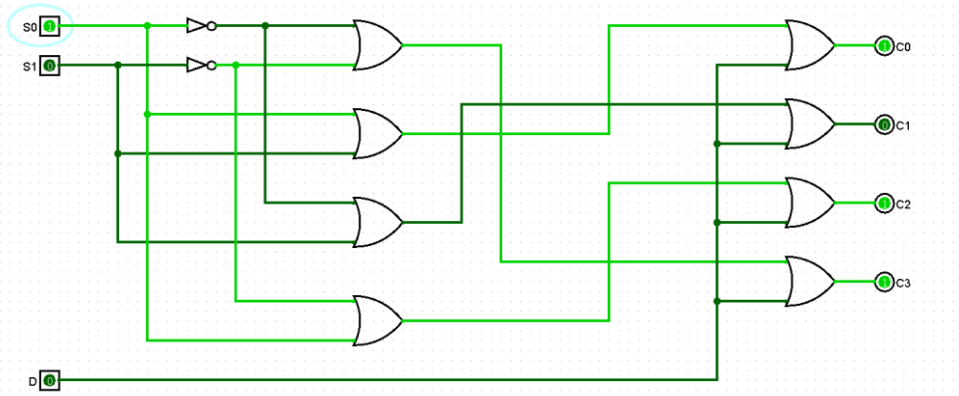


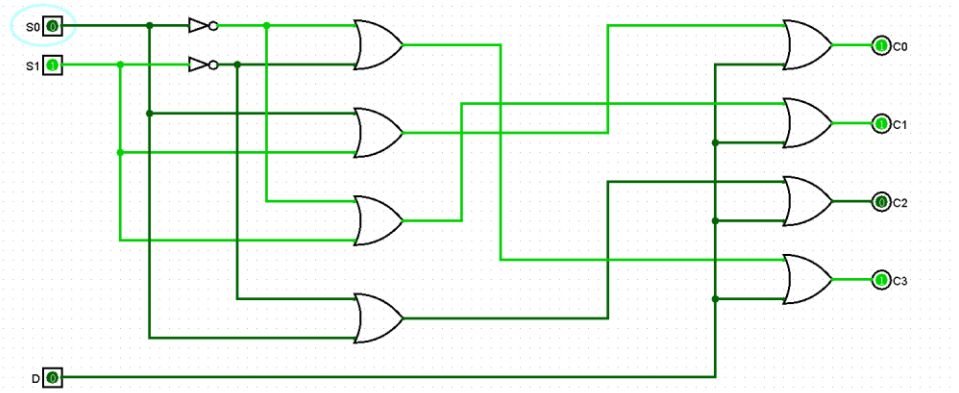
$S_0=0, S_1=0$，此时对应 C0 的输入值

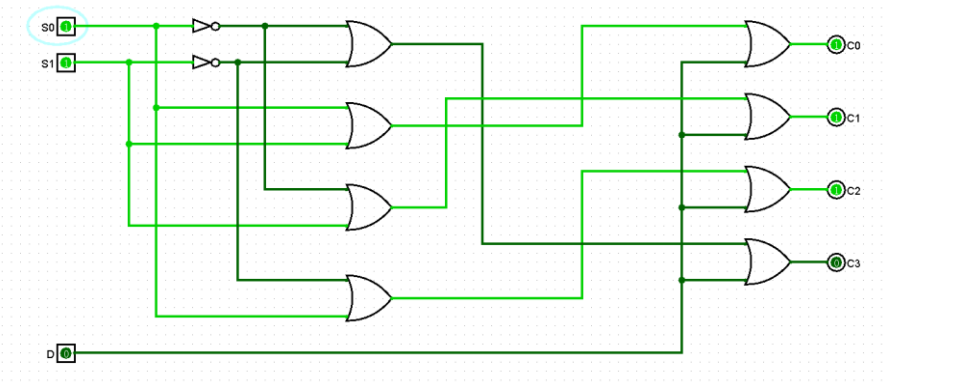
（2） 数据分配器

<1>logisim 逻辑验证图

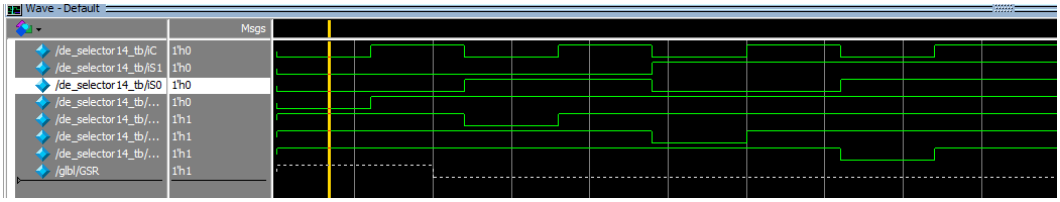




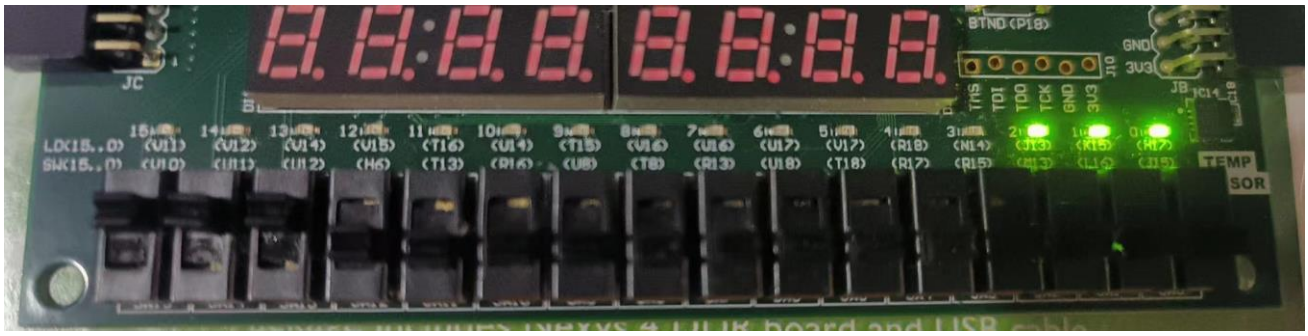




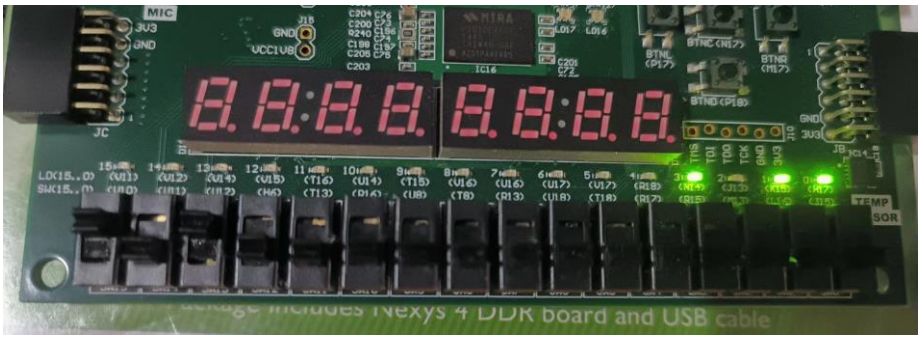
<2>modelsim 仿真图



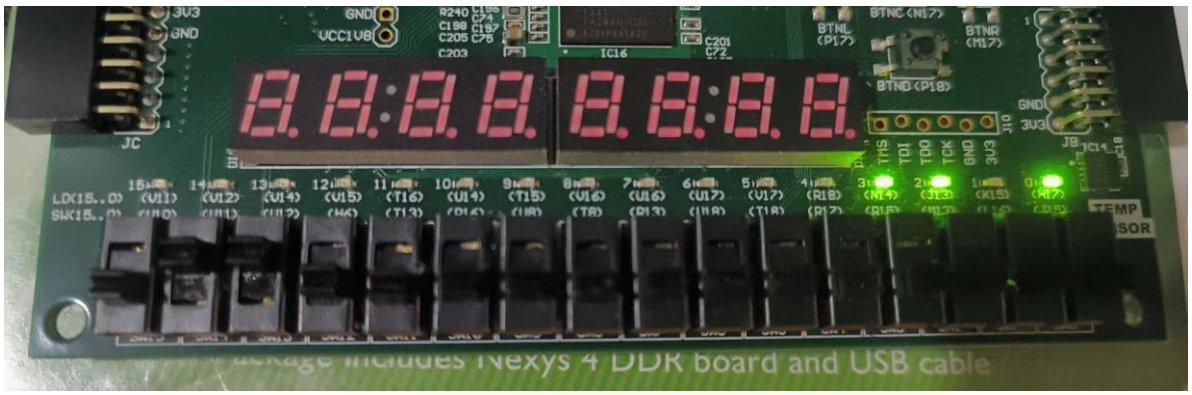
<3>下板结果图



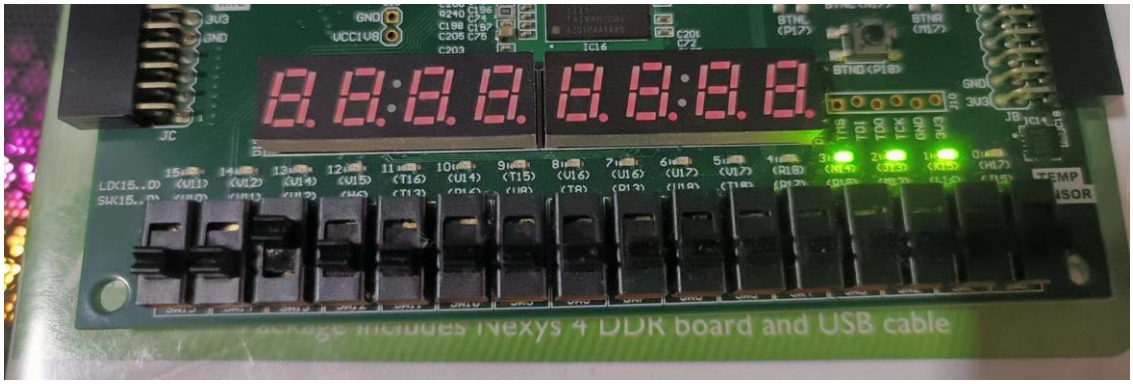
$S_1 = 1,\ S_0 = 1$



$S_1 = 1,\ S_0 = 0$



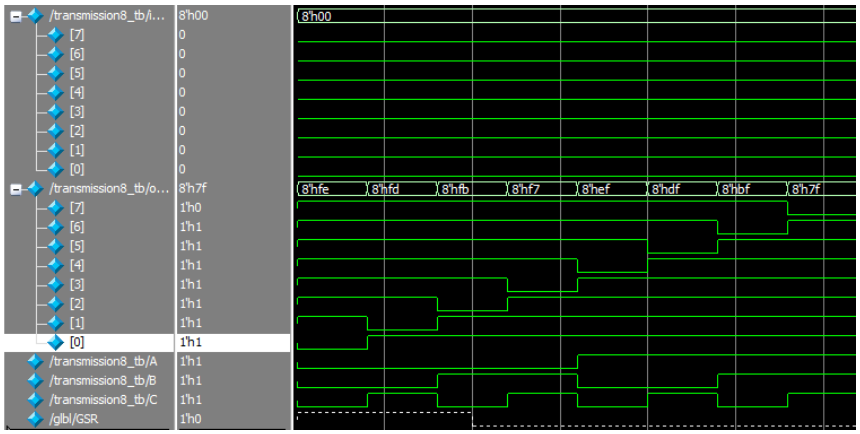
$S_1 = 0,\ S_0 = 1$



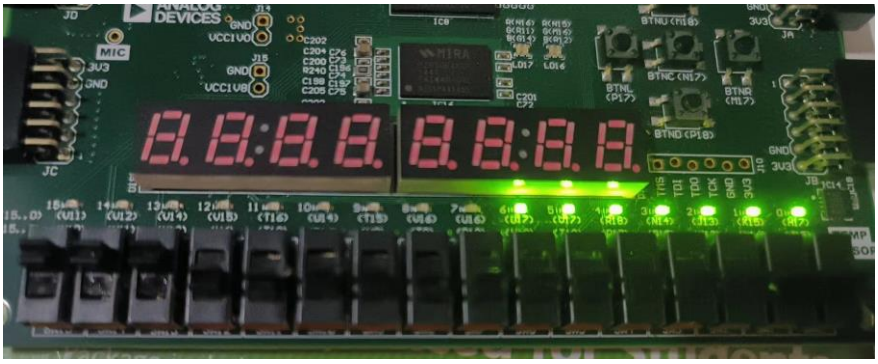
$$S_1 = 0,\ S_0 = 0$$

（3） 8 路数据传输实验

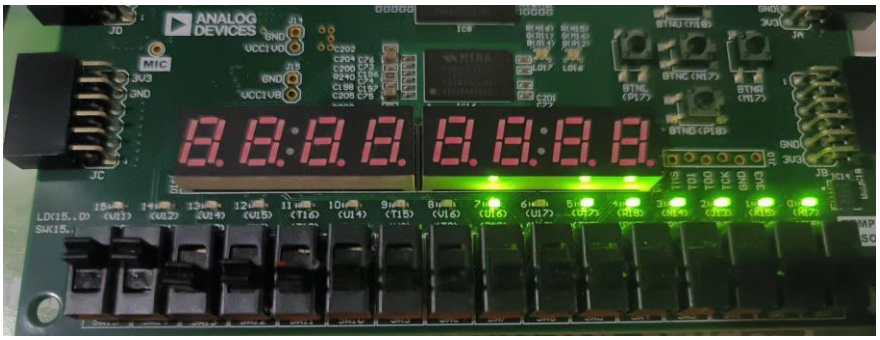
<1>modelsim 仿真图



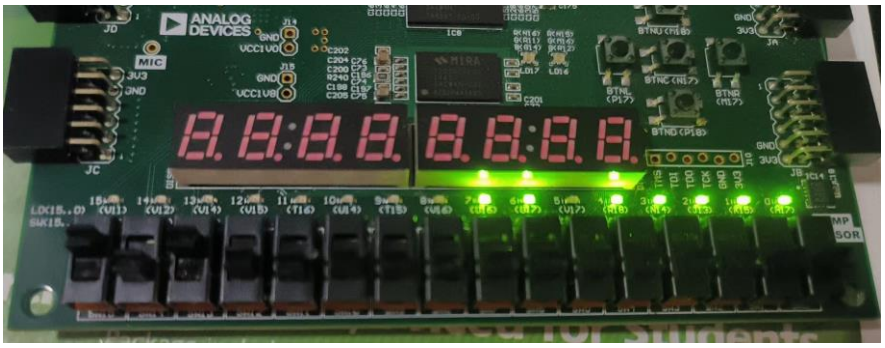
<2>下板结果图



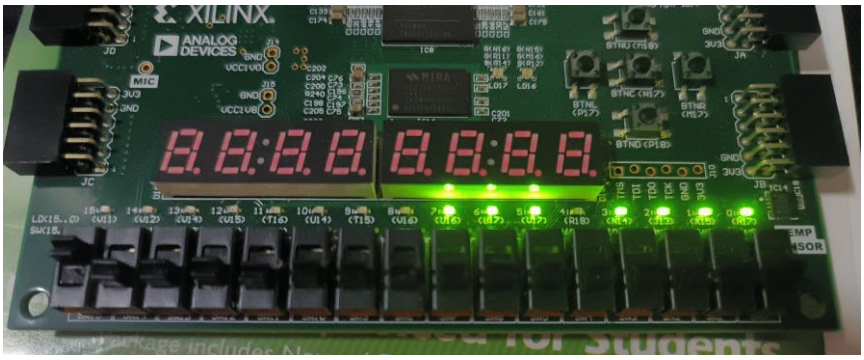
$$A = 1,\ B = 1,\ C = 1$$



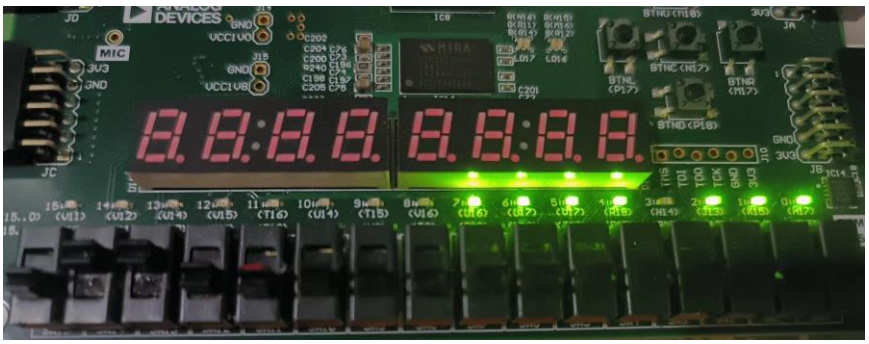
$A = 1,\ B = 1,\ C = 0$



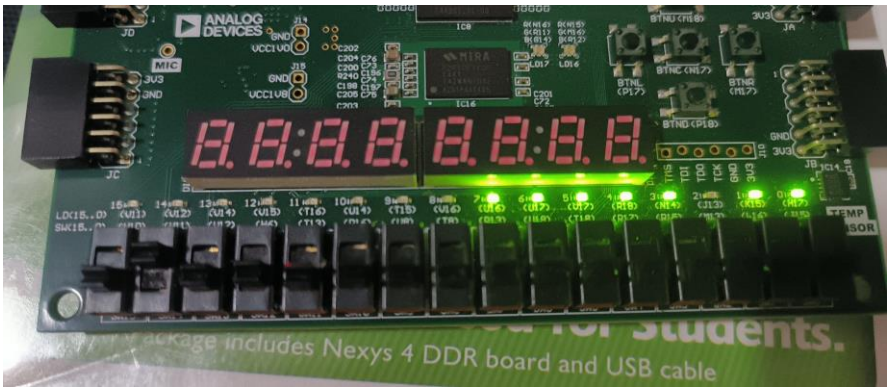
$A = 1,\ B = 0,\ C = 1$



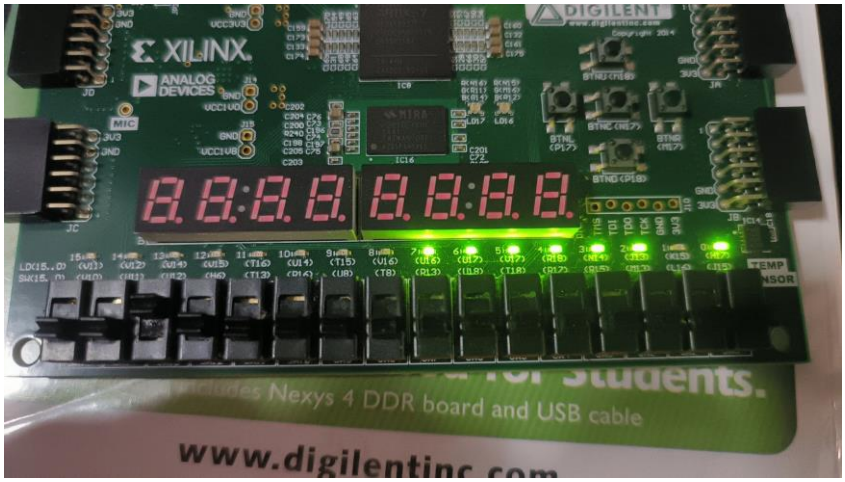
$A = 1,\ B = 0,\ C = 0$



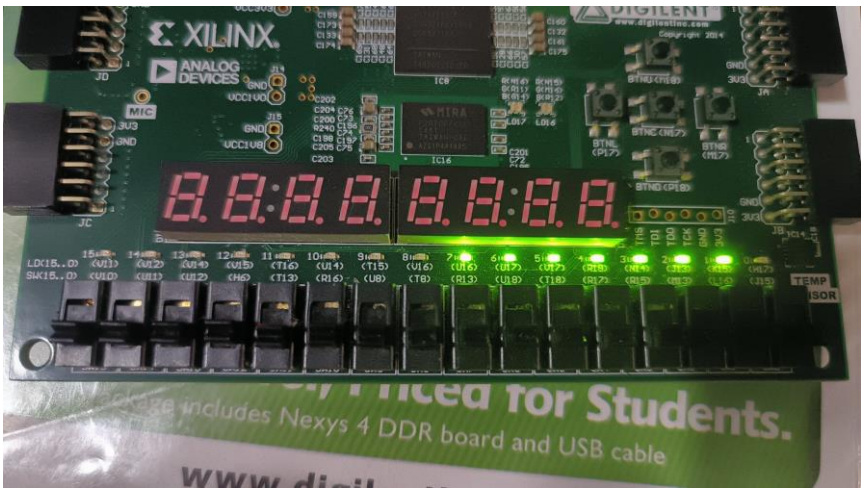
$A = 0,\ B = 1,\ C = 1$



$A = 0,\ B = 1,\ C = 0$



$A = 0,\ B = 0,\ C = 1$



$A = 0,\ B = 0,\ C = 0$