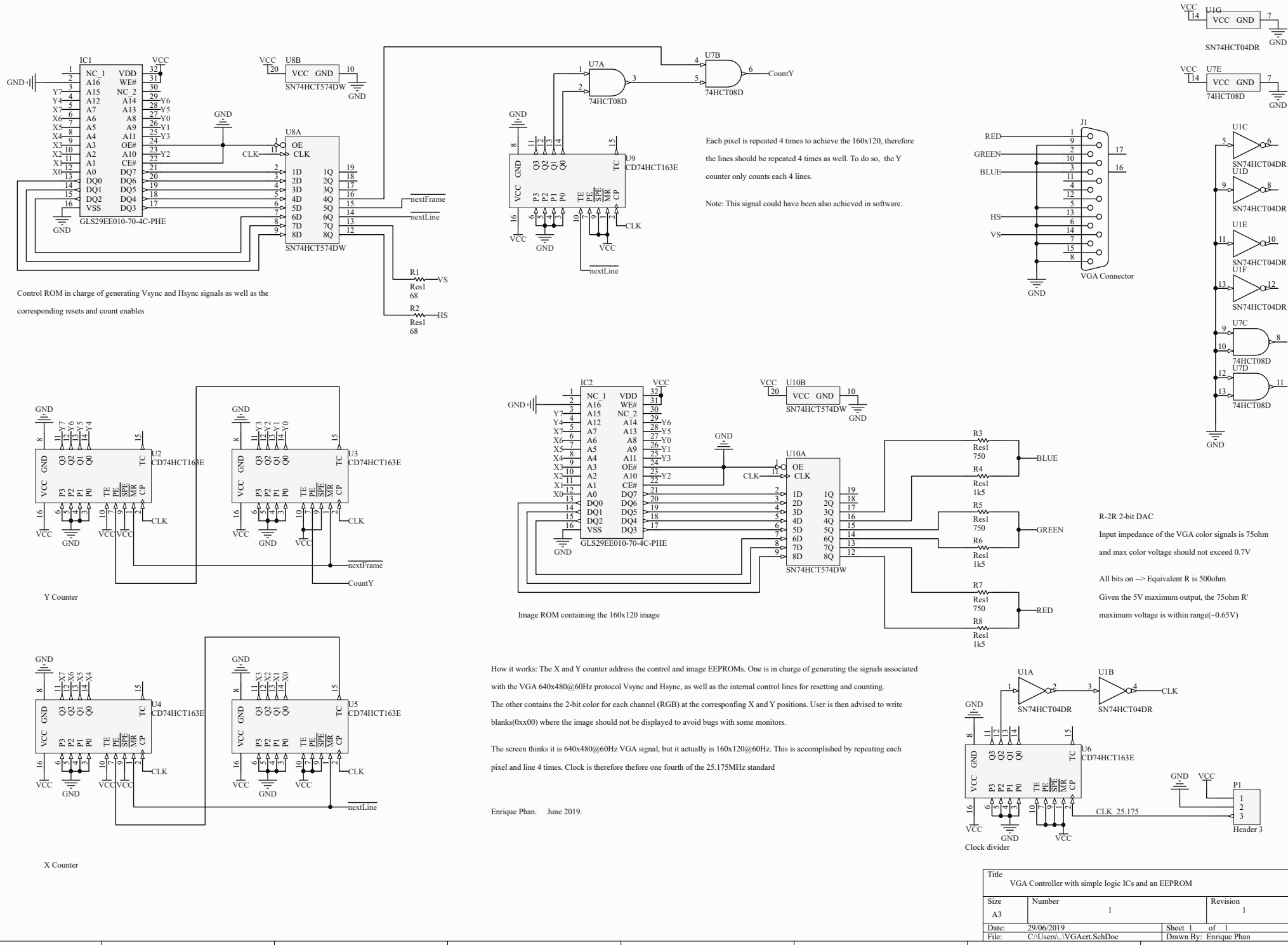
IC1
U8B
SN74HCT574DW
U8A
GLS29EE010-70-4C-PHE
SN74HCT574DW
nextFrame
nextLine
R1
Res1
68
VS
R2
Res1
68
HS
Control ROM in charge of generating Vsync and Hsync signals as well as the
corresponding resets and count enables
U7A
74HCT08D
U7B
74HCT08D
CountY
U9
CD74HCT163E
CLK
Each pixel is repeated 4 times to achieve the 160x120, therefore
the lines should be repeated 4 times as well. To do so, the Y
counter only counts each 4 lines.
Note: This signal could have been also achieved in software.
J1
VGA Connector
RED
GREEN
BLUE
HS
VS
U1G
SN74HCT04DR
U7E
74HCT08D
U1C
U1D
U1E
U1F
U7C
U7D
74HCT08D
U2
U3
CD74HCT163E
Y Counter
IC2
U10B
SN74HCT574DW
U10A
GLS29EE010-70-4C-PHE
SN74HCT574DW
Image ROM containing the 160x120 image
R3
R4
R5
R6
R7
R8
Res1
750
1k5
BLUE
GREEN
RED
R-2R 2-bit DAC
Input impedance of the VGA color signals is 75ohm
and max color voltage should not exceed 0.7V
All bits on --> Equivalent R is 500ohm
Given the 5V maximum output, the 75ohm R'
maximum voltage is within range(~0.65V)
U4
U5
CD74HCT163E
X Counter
How it works: The X and Y counter address the control and image EEPROMs. One is in charge of generating the signals associated
with the VGA 640x480@60Hz protocol Vsync and Hsync, as well as the internal control lines for resetting and counting.
The other contains the 2-bit color for each channel (RGB) at the corresponfing X and Y positions. User is then advised to write
blanks(0xx00) where the image should not be displayed to avoid bugs with some monitors.
The screen thinks it is 640x480@60Hz VGA signal, but it actually is 160x120@60Hz. This is accomplished by repeating each
pixel and line 4 times. Clock is therefore thefore one fourth of the 25.175MHz standard
Enrique Phan. June 2019.
U1A
U1B
SN74HCT04DR
U6
CD74HCT163E
CLK 25.175
P1
Header 3
Clock divider
Title
VGA Controller with simple logic ICs and an EEPROM
Size
A3
Number
1
Revision
1
Date: 29/06/2019
Sheet 1 of 1
File: C:\Users\..\VGAcrt.SchDoc
Drawn By: Enrique Phan