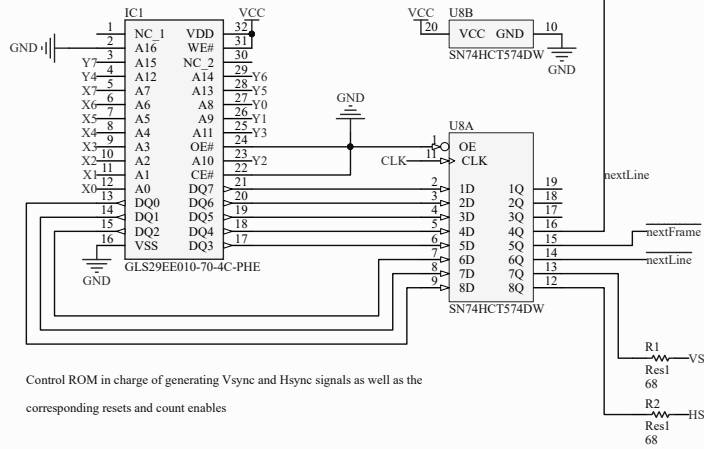
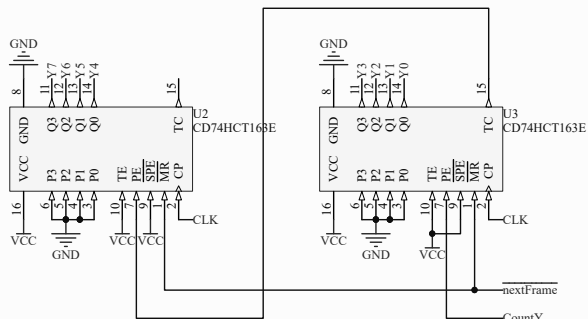


A



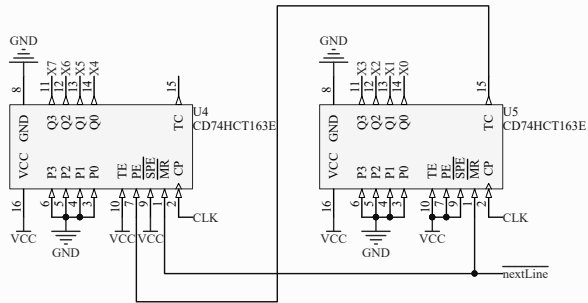
Control ROM in charge of generating Vsync and Hsync signals as well as the corresponding resets and count enables

B



Y Counter

C



X Counter

D

Each pixel is repeated 4 times to achieve the 160x120, therefore the lines should be repeated 4 times as well. To do so, the Y counter only counts each 4 lines.

Note: This signal could have been also achieved in software.

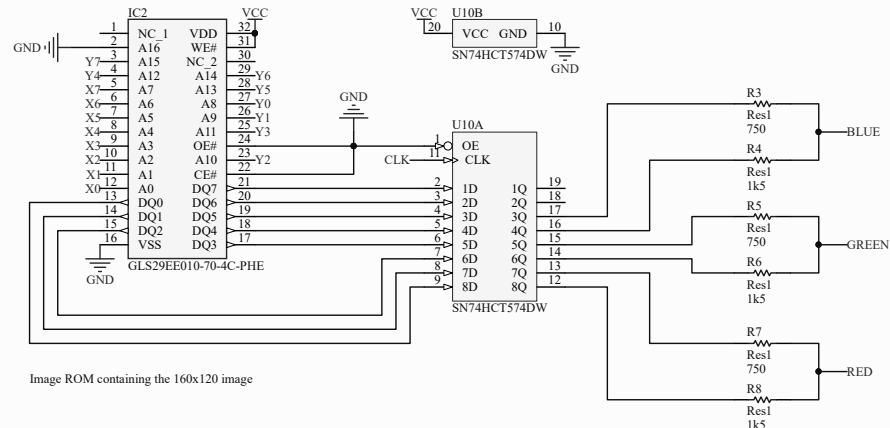


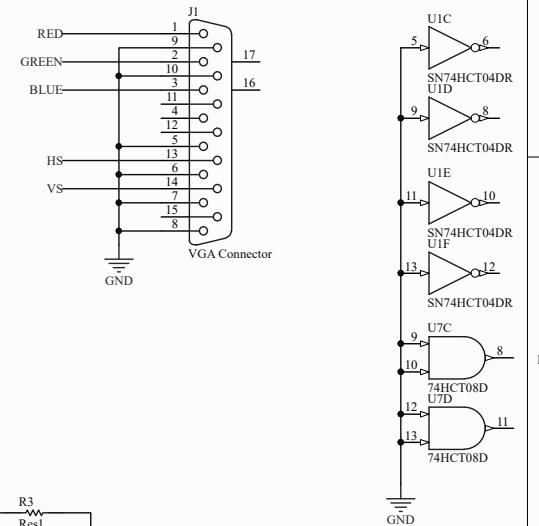
Image ROM containing the 160x120 image

How it works: The X and Y counter address the control and image EEPROMs. One is in charge of generating the signals associated with the VGA 640x480@60Hz protocol Vsync and Hsync, as well as the internal control lines for resetting and counting.

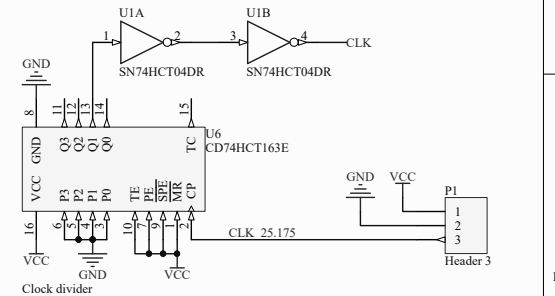
The other contains the 2-bit color for each channel (RGB) at the corresponding X and Y positions. User is then advised to write blanks(0xx00) where the image should not be displayed to avoid bugs with some monitors.

The screen thinks it is 640x480@60Hz VGA signal, but it actually is 160x120@60Hz. This is accomplished by repeating each pixel and line 4 times. Clock is therefore one fourth of the 25.175MHz standard

Enrique Phan. June 2019.



R-2R 2-bit DAC
Input impedance of the VGA color signals is 75ohm and max color voltage should not exceed 0.7V
All bits on --> Equivalent R is 500ohm
Given the 5V maximum output, the 75ohm R' maximum voltage is within range(-0.65V)



Clock divider

Title		
VGA Controller with simple logic ICs and an EEPROM		
Size	Number	Revision
A3	1	1
Date:	07/07/2019	Sheet 1 of 1
File:	C:\Users\...\VGAert.SchDoc	Drawn By: Enrique Phan