PHoEnix Association presents

VERILOG WORKSHOP

SUMMARY

1. **UNIT OF STUDY**: Verilog
2. **OBJECTIVE**: Teach the basic concepts of Verilog HDL to prepare students for 2nd year courses and enable them to make a project based on it.
3. **INSTRUCTOR**: Vishwas Baya, Sathvik Swaminathan, Dhruv Makwana
4. **TIME**: 5 live interactive sessions

WHAT IS VERILOG?

Verilog is a hardware description language (HDL) used to model electronic systems. Applied to electronic design, Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis (testability analysis and fault grading) and for logic synthesis.

WHAT CAN YOU DO WITH VERILOG?

It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using a HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

COURSE PLAN

Topic No.	Topics to be covered	Learning Objectives	Day
1	Overview of digital design	• Combinational Circuits • Doubts and discussion on DD	**DAY 1**
2	Introduction to Verilog and Abstraction	• Introduction to verilog and the software used. • Introduction to different levels of modeling and abstraction • Data Types and Operators	**DAY 2**
3	Testbench and Structure Modelling	• Testbench. • 2 to 1 Multiplexer. • 2 to 4 Decoder. • 3-Bit Adder.	**DAY 3-5**
4	Behavioural Modeling (sequential statements)	• Sequential Statements (if-else, case). • Multiplexers. • Decoders. • Comparator using sequential statements.	
5	Project	Application of Verilog into a project (optional)	

MATERIAL AND RESOURCES

Resources corresponding to the topics covered in each class would be provided as the course goes on for better understanding and further reading.

ASSESSMENT

Final project needs to be completed to be eligible for the certificate.