Combinational circuits and k-maps from day 1 was completed.
Verilog was started after that.
Slides used in all 3 sections
https://docs.google.com/presentation/d/1tIYgitft6ctL3BZuuMhFqYhTXRGaSiuLqlUbDq-S1j8/edit?usp=sharing
Iverilog commands : https://iverilog.fandom.com/wiki/Getting_Started

a good comprehensive book that explains all of what we covered in detail:
https://faculty.kfupm.edu.sa/COE/aimane/coe405/FPGA%20Prototyping%20with%20Verilog%20examples.pdf

Test bench template:

(any variables you assign under the initial block should be declared as reg. so basically all the inputs should be declared as **reg.** change the wire and reg variable names accordingly for your circuit)

```
// The `timescale directive specifies that
// the simulation time unit is 1 ns  and
// the simulation timestep is 10 ps
`timescale 1 ns/10 ps

module eq2_testbench;
    // signal declaration
    reg  [1:0] test_in0, test_in1;
    wire  test_out;

    // instantiate the circuit under test
    eq2 uut
        (.a(test_in0), .b(test_in1), .aeqb(test_out));

    //  test vector generator
    initial
    begin
        // test vector 1
        test_in0 = 2'b00;
        test_in1 = 2'b00;
        # 200;
        // test vector 2
        test_in0 = 2'b01;
        test_in1 = 2'b00;
```

```
25          # 200;
            // test vector 3
            test_in0 = 2'b01;
            test_in1 = 2'b11;
            # 200;
30          // test vector 4
            test_in0 = 2'b10;
            test_in1 = 2'b10;
            # 200;
            // test vector 5
35          test_in0 = 2'b10;
            test_in1 = 2'b00;
            # 200;
            // test vector 6
            test_in0 = 2'b11;
40          test_in1 = 2'b11;
            # 200;
            // test vector 7
            test_in0 = 2'b11;
            test_in1 = 2'b01;
45          # 200;
            // stop simulation
            $stop;
        end

50  endmodule
```