POKAI HUANG

Design Verification Engineer

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https://github.com/PKhuang-TW

PROFESSIONAL SUMMARY

Experienced engineer with 1 year in design verification and 3.5 years in firmware development. Skilled in collaborating with clients to define test plans and design test vectors, and experienced in working closely with in-house designers for efficient debugging. Familiar with FPV and using SVA to verify submodule behaviors. Highly self-motivated, dedicating personal time to mastering UVM library internals and building UVM VIPs to strengthen practical and theoretical understanding.

EXPERIENCE

Design Verification Engineer | Phison Electronic 06/2024 - Present

- UFS underlying IP (**Unipro**) design verification
- Develop UVM environment for DUT
- Formal Property Verification (**FPV**)
- Design test plans and testvectors
- Discuss and modify test plans with international clients
- Verifying in-house DUTs and collaborating with designers on debugging

Firmware Engineer | Silicon Motion 01/2021 – 05/2024

- Develop Security features according to TCG specification
- Design Security features Test Plan & verify
- Customize requirements & Firmware debug
- Modularize features into Libraries for easier project management
- Develop automation scripts to improve working efficiency

EDUCATION

National Chiao Tung University - Hsinchu 09/2018 – 11/2020
Master - Institute of Computer Science And Engineering

National Central University - Taoyuan 09/2013 – 06/2017
Bachelor – Department of Communication Engineering