

### Brief Description

The ZSPM4521 is a DC/DC synchronous switching lithium-ion (Li-Ion) battery charger with fully integrated power switches, internal compensation, and full fault protection. It uses a temperature-independent photovoltaic maximum power point tracking (MPPT) function to optimize power output from the source during Full-Charge Constant-Current (CC) Mode. Its switching frequency of 1MHz enables the use of small filter components, resulting in smaller board space and reduced bill-of material costs.

During Full-Charge Constant-Current Mode, the duty cycle is controlled by the MPPT regulator. Once the battery's termination voltage is reached, the regulator operates in Constant Voltage Mode. In this mode, the ZSPM4521 modulates the charging current until the battery reaches full charge. When the regulator is disabled (the EN pin is low), the device draws 10µA (typical) quiescent current (Disabled Mode).

The ZSPM4521 includes supervisory reporting through the NFLT (inverted fault) open-drain output to interface other components in the system. Device programming is achieved by an I<sup>2</sup>C™\* interface through the SCL and SDA pins.

### Benefits

- Up to 1.5A of continuous output current in Full-Charge Constant Current (CC) Mode
- High efficiency – up to 92% with typical loads

### Available Support

- Evaluation Kit
- Documentation

### Features

- Temperature-independent photovoltaic maximum power tracking (MPPT) regulator
- VBAT reverse-current blocking
- Programmable temperature-compensated termination voltage: 3.94V to 4.18V ± 1%
- User programmable maximum charge current: 50mA to 1500mA
- Supervisor for V<sub>BAT</sub> reported at the NFLT pin
- Input supply under-voltage lockout
- Full protection for VBAT over-current, over-temperature, VBAT over-voltage, and charging timeout
- Charge status indication
- I<sup>2</sup>C™ program interface with EEPROM registers

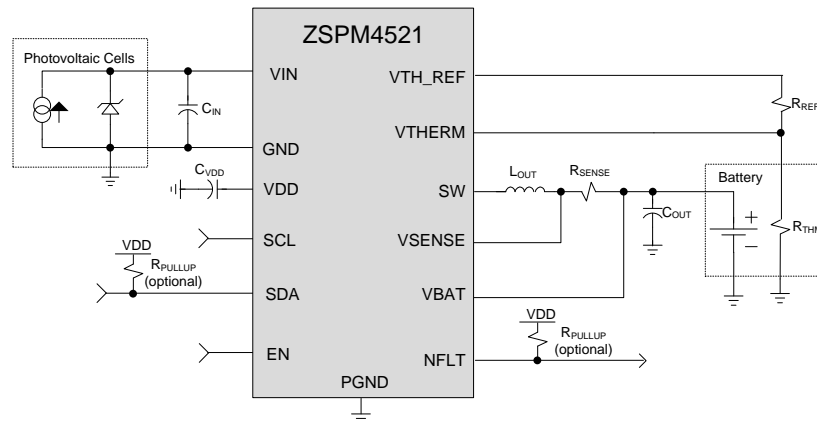
### Related IDT Smart Power Products

- ZSPM4523 DC/DC Synchronous Switching Super Capacitor Charger With MPPT Regulator
- ZSPM4551 High-Efficiency Li-Ion Battery Charger
- ZSPM4121 Ultra-low Power Under-Voltage Switch
- ZSPM4141 Ultra-Low-Power Linear Regulator

### Physical Characteristics

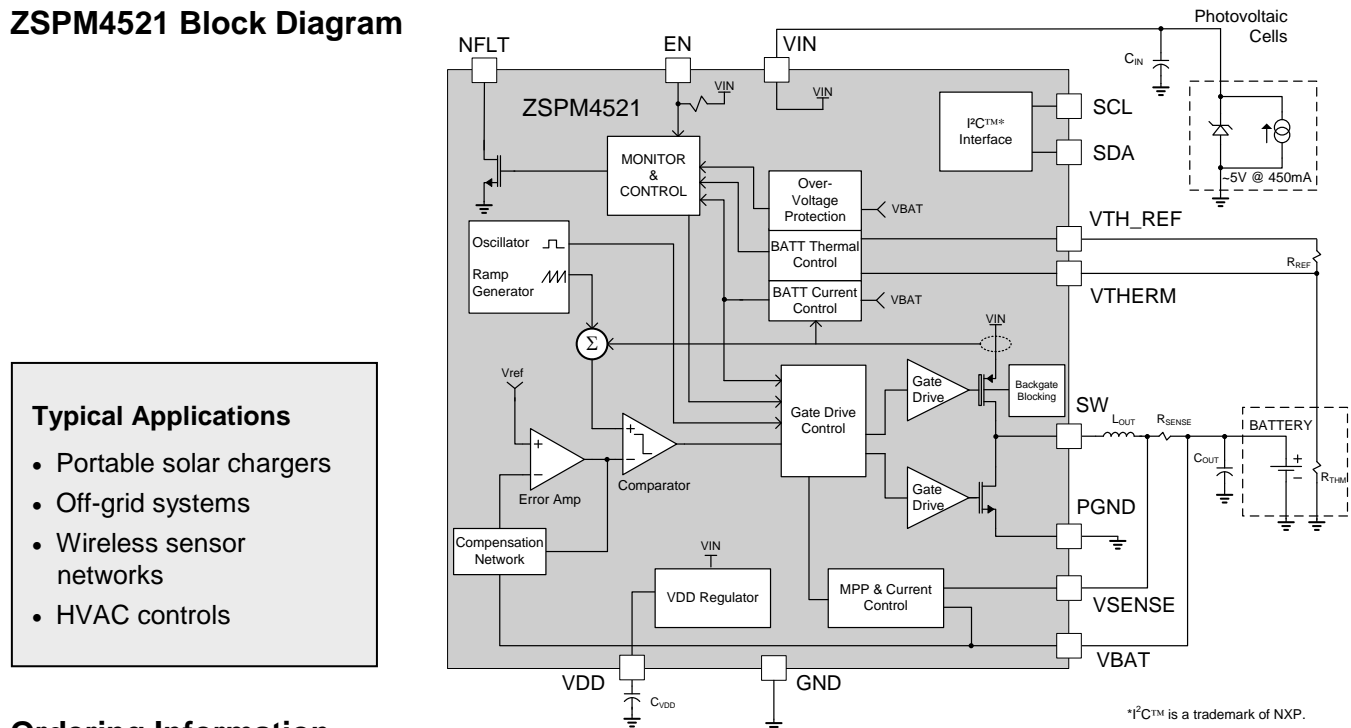
- Wide input voltage range: 4.0V to 7.2V
- Junction operating temperature: -40°C to 125°C
- Package: 16-pin PQFN (4mm x 4mm)

### ZSPM4521 Application Circuit



\* I<sup>2</sup>C™ is a trademark of NXP.

### ZSPM4521 Block Diagram



### Ordering Information

| Ordering Code | Description                                                              | Package                             |
|---------------|--------------------------------------------------------------------------|-------------------------------------|
| ZSPM4521AA1W  | ZSPM4521 High Efficiency Li-Ion Battery Charger for Photovoltaic Sources | 16-pin PQFN / 7" Reel (1000 parts)  |
| ZSPM4521AA1R  | ZSPM4521 High Efficiency Li-Ion Battery Charger for Photovoltaic Sources | 16-pin PQFN / 13" Reel (3300 parts) |
| ZSPM4521KIT   | ZSPM4521 Evaluation Kit                                                  | Kit                                 |

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# 1 ZSPM4521 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## 1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted.

**Table 1.1 Absolute Maximum Ratings**

| Parameter                                                                                                                                                                  | Value <sup>1)</sup> | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|
| VIN, EN, NFLT, SCL, SDA, VTHERM, VTH_REF, VBAT, VSENSE                                                                                                                     | -0.3 to 8           | V    |
| SW                                                                                                                                                                         | -1 to 8.8           | V    |
| VDD                                                                                                                                                                        | -0.3 to 3.6         | V    |
| Operating Junction Temperature Range, T <sub>J</sub>                                                                                                                       | -40 to 125          | °C   |
| Storage Temperature Range, T <sub>STOR</sub>                                                                                                                               | -65 to 150          | °C   |
| Electrostatic Discharge – Human Body Model <sup>2)</sup>                                                                                                                   | ±2k                 | V    |
| Electrostatic Discharge – Machine Model <sup>2)</sup>                                                                                                                      | +/-200              | V    |
| Lead Temperature (soldering, 10 seconds)                                                                                                                                   | 260                 | °C   |
| <sup>1)</sup> All voltage values are with respect to network ground terminal.<br><sup>2)</sup> ESD testing is performed according to the respective JESD22 JEDEC standard. |                     |      |

## 1.2. Thermal Characteristics

**Table 1.2 Thermal Characteristics**

| Parameter                                                                                                    | Symbol        | Value <sup>1)</sup> | Unit |
|--------------------------------------------------------------------------------------------------------------|---------------|---------------------|------|
| Thermal Resistance Junction to Air <sup>1)</sup>                                                             | $\theta_{JA}$ | 50                  | °C/W |
| <sup>1)</sup> Assumes a 4x4mm QFN-16 in 1 in <sup>2</sup> area of 2 oz. copper and 25°C ambient temperature. |               |                     |      |

### 1.3. Recommended Operating Conditions

**Table 1.3 Recommended Operating Conditions**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                        | Symbol               | Min | Typ | Max | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|-----|-----|------|
| Photovoltaic Input Operating Voltage at VIN Pin                                                                                                                                                                                                                                                                                                                                                                                  | V <sub>IN</sub>      | 4.0 | 5.3 | 7.2 | V    |
| Sense Resistor                                                                                                                                                                                                                                                                                                                                                                                                                   | R <sub>SENSE</sub>   |     | 50  |     | mΩ   |
| Output Filter Inductor Typical Value <sup>1)</sup>                                                                                                                                                                                                                                                                                                                                                                               | L <sub>OUT</sub>     |     | 4.7 |     | μH   |
| Output Filter Capacitor Typical Value <sup>2)</sup>                                                                                                                                                                                                                                                                                                                                                                              | C <sub>OUT</sub>     |     | 4.7 |     | μF   |
| Output Filter Capacitor ESR                                                                                                                                                                                                                                                                                                                                                                                                      | C <sub>OUT-ESR</sub> |     |     | 100 | mΩ   |
| Input Supply Bypass Capacitor Value <sup>3)</sup>                                                                                                                                                                                                                                                                                                                                                                                | C <sub>IN</sub>      | 3.3 | 10  |     | μF   |
| VDD Supply Bypass Capacitor Value <sup>2)</sup>                                                                                                                                                                                                                                                                                                                                                                                  | C <sub>VDD</sub>     | 70  | 100 | 130 | nF   |
| Operating Free Air Temperature                                                                                                                                                                                                                                                                                                                                                                                                   | T <sub>A</sub>       | -40 |     | 85  | °C   |
| Operating Junction Temperature                                                                                                                                                                                                                                                                                                                                                                                                   | T <sub>J</sub>       | -40 |     | 125 | °C   |
| <p>1) For best performance, use an inductor with a saturation current rating higher than the maximum V<sub>BAT</sub> load requirement plus the inductor current ripple.</p> <p>2) For best performance, use a low ESR ceramic capacitor.</p> <p>3) For best performance, use a low ESR ceramic capacitor. If C<sub>IN</sub> is not a low ESR ceramic capacitor, add a 0.1μF ceramic capacitor in parallel to C<sub>IN</sub>.</p> |                      |     |     |     |      |

### 1.4. Electrical Characteristics

Electrical characteristics T<sub>J</sub> = -40°C to 125°C, V<sub>IN</sub> = 5.3V, (unless otherwise noted)

**Table 1.4 Electrical Characteristics**

| Parameter                          | Symbol                  | Condition                                                                                | Min | Typ | Max | Unit |
|------------------------------------|-------------------------|------------------------------------------------------------------------------------------|-----|-----|-----|------|
| <b>VIN Supply Voltage</b>          |                         |                                                                                          |     |     |     |      |
| Photovoltaic Voltage Input         | V <sub>IN</sub>         |                                                                                          | 4   | 5.3 | 7.2 | V    |
| Quiescent Current<br>Normal Mode   | I <sub>CC-NORM</sub>    | I <sub>LOAD</sub> = 0A, no switching<br>EN ≥ 2.2V (HIGH)                                 |     | 3   |     | mA   |
| Quiescent Current<br>Disabled Mode | I <sub>CC-DISABLE</sub> | EN = 0V                                                                                  |     | 10  | 50  | μA   |
| <b>VBAT Leakage</b>                |                         |                                                                                          |     |     |     |      |
| Leakage Current From<br>Battery    | I <sub>BAT-LEAK</sub>   | EN = 0V, V <sub>VBAT</sub> = 4.1V                                                        |     |     | 10  | μA   |
| Reverse Current                    | I <sub>BAT-BACK</sub>   | V <sub>VBAT</sub> > V <sub>IN</sub> , V <sub>VBAT</sub> = 4.1V,<br>T <sub>J</sub> < 85°C |     |     | 10  | μA   |

| Parameter                                       | Symbol            | Condition           | Min | Typ  | Max | Unit        |
|-------------------------------------------------|-------------------|---------------------|-----|------|-----|-------------|
| <b>VIN Under-Voltage Lockout</b>                |                   |                     |     |      |     |             |
| Input Supply Under-Voltage Threshold            | $V_{IN-UV}$       | $V_{IN}$ increasing |     | 3.15 |     | V           |
| Input Supply Under-Voltage Threshold Hysteresis | $V_{IN-UV\_HYST}$ |                     | 100 | 200  |     | mV          |
| <b>OSC</b>                                      |                   |                     |     |      |     |             |
| Oscillator Frequency                            | $f_{OSC}$         |                     | 0.9 | 1    | 1.1 | MHz         |
| <b>NFLT Open Drain Output</b>                   |                   |                     |     |      |     |             |
| High-Level Output Leakage                       | $I_{OH-NFLT}$     | $V_{NFLT} = 5.3V$   |     | 0.1  |     | $\mu A$     |
| Low-Level Output Voltage                        | $V_{OL-NFLT}$     | $I_{NFLT} = -1mA$   |     |      | 0.4 | V           |
| <b>EN/SCL/SDA Input Voltage Thresholds</b>      |                   |                     |     |      |     |             |
| High Level Input Voltage                        | $V_{IH}$          |                     | 2.2 |      |     | V           |
| Low Level Input Voltage                         | $V_{IL}$          |                     |     |      | 0.8 | V           |
| Input Hysteresis– EN, SCL, SDA Pins             | $V_{HYST}$        |                     |     | 200  |     | mV          |
| Input Leakage – EN Pin                          | $I_{IN-EN}$       | $V_{EN}=VIN$        |     | 0.1  |     | $\mu A$     |
|                                                 |                   | $V_{EN}=0V$         |     | -2.0 |     | $\mu A$     |
| Input Leakage – SCL Pin                         | $I_{IN-SCL}$      | $V_{SCL}=VIN$       |     | 55   |     | $\mu A$     |
|                                                 |                   | $V_{SCL}=0V$        |     | -0.1 |     | $\mu A$     |
| Input Leakage – SDA Pin                         | $I_{IN-SDA}$      | $V_{SDA}=VIN$       |     | 0.1  |     | $\mu A$     |
|                                                 |                   | $V_{SDA}=0V$        |     | -0.1 |     | $\mu A$     |
| Low-Level Output Voltage                        | $V_{OL-SDA}$      | $I_{SDA} = -1mA$    |     |      | 0.4 | V           |
| <b>Thermal Shutdown</b>                         |                   |                     |     |      |     |             |
| Thermal Shutdown Junction Temperature           | $T_{SD}$          |                     | 150 | 170  |     | $^{\circ}C$ |
| TSD Hysteresis                                  | $T_{SD-HYST}$     |                     |     | 10   |     | $^{\circ}C$ |
| <b>Pre-Charge End</b>                           |                   |                     |     |      |     |             |
| Pre-charge Voltage Threshold                    | $V_{PRECHG}$      |                     | 2.9 | 3.0  | 3.1 | V           |
| Pre-charge Voltage Hysteresis                   | $V_{PC-HYST}$     |                     |     | 70   |     | mV          |
| <b>Charge Restart</b>                           |                   |                     |     |      |     |             |
| Voltage Below Termination for Charging Restart  | $V_{RESTART}$     |                     |     | 100  |     | mV          |

| Parameter                                                                                      | Symbol                | Condition                                                                                               | Min              | Typ            | Max              | Unit       |
|------------------------------------------------------------------------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------|------------------|----------------|------------------|------------|
| <b>Charging Regulator with <math>L_{OUT}=4.7\mu H</math> and <math>C_{OUT}=4.7\mu F</math></b> |                       |                                                                                                         |                  |                |                  |            |
| Output Current Limit Tolerance in Full-Charge Mode                                             | $I_{BAT-FC}$          | $I_{BAT}$ is user programmable; see Table 2.5.                                                          | $I_{BAT} - 10\%$ | $I_{BAT}$      | $I_{BAT} + 10\%$ | A          |
| Termination Voltage Tolerance in Top-Off Mode                                                  | $V_{BAT-TO}$          | $I_{CHG} = 0.1C$ , $0^{\circ}C < T_J < 85^{\circ}C$<br>$V_{BAT}$ is user programmable; see section 2.4. | $V_{BAT} - 1\%$  | $V_{BAT}$      | $V_{BAT} + 1\%$  | V          |
| Top-Off Mode Time Out                                                                          | $t_{TO}$              |                                                                                                         | 0                |                | 120              | Minutes    |
| Full-Charge Timer                                                                              | $t_{FC}$              |                                                                                                         | 200              |                | 1400             | Minutes    |
| Timer Accuracy                                                                                 | $t_{ACC}$             |                                                                                                         | -10%             |                | +10%             |            |
| High Side (HS) Switch On Resistance                                                            | $R_{DSON}$            | $I_{SW} = -1A$ , $T_J=25^{\circ}C$                                                                      |                  | 200            |                  | m $\Omega$ |
| Low Side (LS) Switch On Resistance                                                             |                       | $I_{SW} = 1A$ , $T_J=25^{\circ}C$                                                                       |                  | 250            |                  | m $\Omega$ |
| Maximum Output Current                                                                         | $I_{BAT}$             |                                                                                                         |                  | 1.5            |                  | A          |
| Over-Current Detection                                                                         | $I_{OCD}$             | HS switch current                                                                                       | 2.5              |                |                  | A          |
| $V_{BAT}$ Over-Voltage Threshold                                                               | $V_{BAT-OV}$          |                                                                                                         | 101% $V_{BAT}$   | 102% $V_{BAT}$ | 103% $V_{BAT}$   | V          |
| Maximum Duty Cycle                                                                             | $DUTY_{MAX}$          |                                                                                                         |                  | 98             |                  | %          |
| <b>Thermistor</b>                                                                              |                       |                                                                                                         |                  |                |                  |            |
| VTH_REF Output Voltage                                                                         | $V_{VTH\_REF}$        | $I_{VT\_REF} = 2\mu A$ to $100\mu A$                                                                    |                  | 1.8            |                  | V          |
| <b>Thermistor: 10k<math>\Omega</math> Temperature Thresholds – <math>\beta=3434K</math></b>    |                       |                                                                                                         |                  |                |                  |            |
| 0 $^{\circ}C$ VTHERM Threshold (0 $^{\circ}C$ )                                                | 0 $^{\circ}C$         | Decreasing Temperature                                                                                  |                  | 75.6           |                  | %VTH_REF   |
| 0 $^{\circ}C$ VTHERM Threshold with Hysteresis (10 $^{\circ}C$ )                               | 0 $^{\circ}C_{HYST}$  | Increasing Temperature                                                                                  |                  | 66.5           |                  | %VTH_REF   |
| 10 $^{\circ}C$ VTHERM Threshold (10 $^{\circ}C$ )                                              | 10 $^{\circ}C$        | Decreasing Temperature                                                                                  |                  | 66.2           |                  | %VTH_REF   |
| 10 $^{\circ}C$ VTHERM Threshold with Hysteresis (11 $^{\circ}C$ )                              | 10 $^{\circ}C_{HYST}$ | Increasing Temperature                                                                                  |                  | 65.4           |                  | %VTH_REF   |
| 45 $^{\circ}C$ VTHERM Threshold (45 $^{\circ}C$ )                                              | 45 $^{\circ}C$        | Increasing Temperature                                                                                  |                  | 34.5           |                  | %VTH_REF   |
| 45 $^{\circ}C$ VTHERM Threshold with Hysteresis (44 $^{\circ}C$ )                              | 45 $^{\circ}C_{HYST}$ | Decreasing Temperature                                                                                  |                  | 35.3           |                  | %VTH_REF   |
| 50 $^{\circ}C$ VTHERM Threshold (50 $^{\circ}C$ )                                              | 50 $^{\circ}C$        | Increasing Temperature                                                                                  |                  | 30.8           |                  | %VTH_REF   |
| 50 $^{\circ}C$ VTHERM Threshold with Hysteresis (49 $^{\circ}C$ )                              | 50 $^{\circ}C_{HYST}$ | Decreasing Temperature                                                                                  |                  | 31.5           |                  | %VTH_REF   |



| Parameter                                                | Symbol               | Condition              | Min | Typ  | Max | Unit     |
|----------------------------------------------------------|----------------------|------------------------|-----|------|-----|----------|
| 60°C VTHERM Threshold (60°C)                             | 60°C                 | Increasing Temperature |     | 24.9 |     | %VTH_REF |
| 60°C VTHERM Threshold with Hysteresis (50°C)             | 60°C <sub>HYST</sub> | Decreasing Temperature |     | 30.8 |     | %VTH_REF |
| Thermistor: 100KΩ Temperature Thresholds – $\beta=4311K$ |                      |                        |     |      |     |          |
| 0°C VTHERM Threshold (0°C)                               | 0°C                  | Decreasing Temperature |     | 80.5 |     | %VTH_REF |
| 0°C VTHERM Threshold with Hysteresis (10°C)              | 0°C <sub>HYST</sub>  | Increasing Temperature |     | 69.8 |     | %VTH_REF |
| 10°C VTHERM Threshold (10°C)                             | 10°C                 | Decreasing Temperature |     | 69.8 |     | %VTH_REF |
| 10°C VTHERM Threshold with Hysteresis (11°C)             | 10°C <sub>HYST</sub> | Increasing Temperature |     | 68.6 |     | %VTH_REF |
| 45°C VTHERM Threshold (45°C)                             | 45°C                 | Increasing Temperature |     | 31.3 |     | %VTH_REF |
| 45°C VTHERM Threshold with Hysteresis (44°C)             | 45°C <sub>HYST</sub> | Decreasing Temperature |     | 32.3 |     | %VTH_REF |
| 50°C VTHERM Threshold (50°C)                             | 50°C                 | Increasing Temperature |     | 27.0 |     | %VTH_REF |
| 50°C VTHERM Threshold with Hysteresis (49°C)             | 50°C <sub>HYST</sub> | Decreasing Temperature |     | 27.8 |     | %VTH_REF |
| 60°C VTHERM Threshold (60°C)                             | 60°C                 | Increasing Temperature |     | 19.4 |     | %VTH_REF |
| 60°C VTHERM Threshold with Hysteresis (50°C)             | 60°C <sub>HYST</sub> | Decreasing Temperature |     | 27.0 |     | %VTH_REF |

## 1.5. I<sup>2</sup>C™ Interface Timing Requirements

Electrical characteristics T<sub>J</sub> = -40°C to 125°C, V<sub>IN</sub> = 5.3V. See Figure 2.5 for an illustration of the timing specifications given in Table 1.5.

**Table 1.5 I<sup>2</sup>C™ Interface Timing Characteristics**

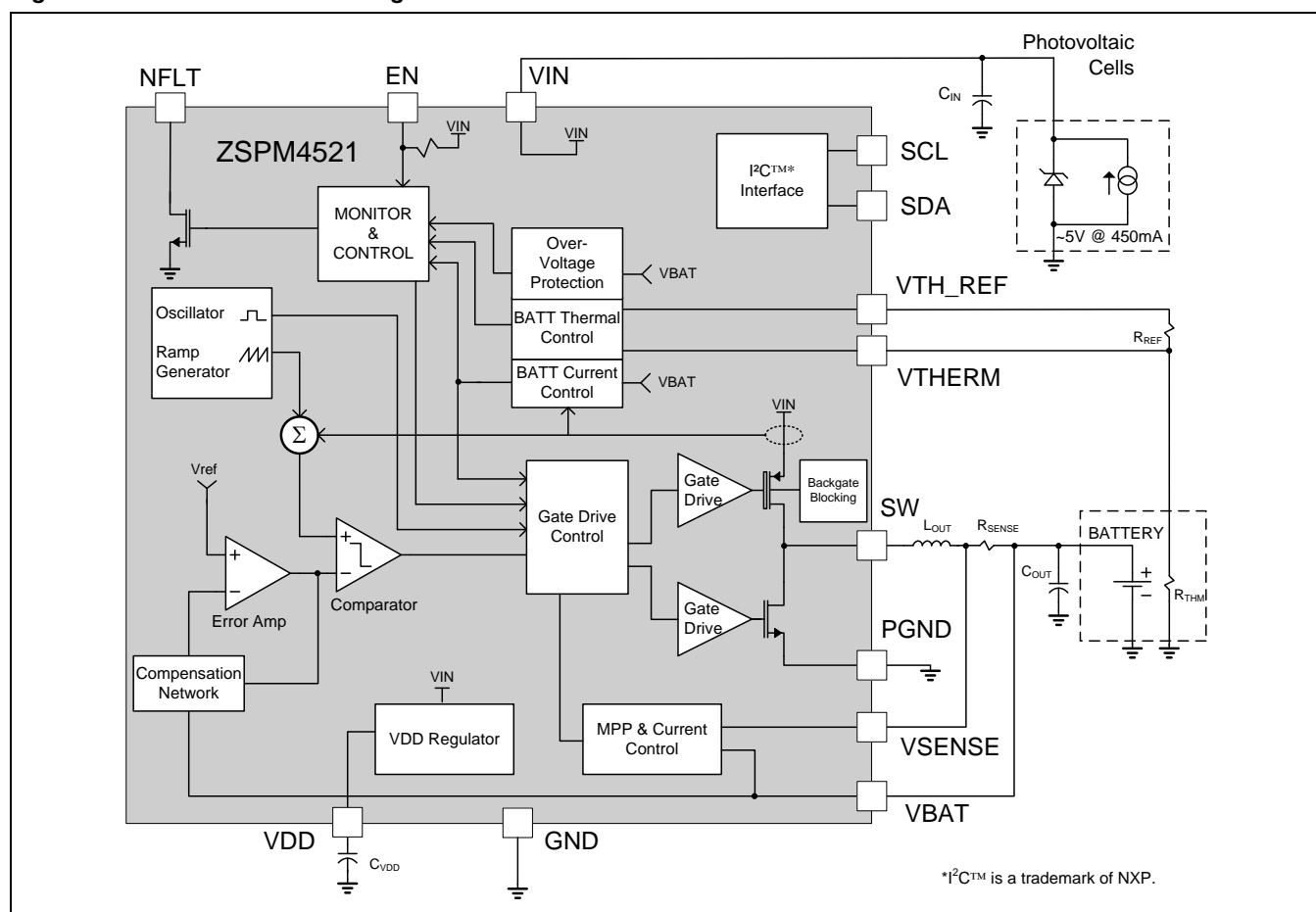
| Parameter                                                                                                                                        | Symbol           | Standard Mode |      | Fast Mode <sup>1)</sup> |     | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------------|------|-------------------------|-----|------|
|                                                                                                                                                  |                  | Min           | Max  | Min                     | Max |      |
| I <sup>2</sup> C™ Clock Frequency                                                                                                                | f <sub>scl</sub> | 0             | 100  | 0                       | 400 | kHz  |
| I <sup>2</sup> C™ Clock High Time                                                                                                                | t <sub>sch</sub> | 4             |      | 0.6                     |     | μs   |
| I <sup>2</sup> C™ Clock Low Time                                                                                                                 | t <sub>scl</sub> | 4.7           |      | 1.3                     |     | μs   |
| I <sup>2</sup> C™ Tolerable Spike Time <sup>2)</sup>                                                                                             | t <sub>sp</sub>  | 0             | 50   | 0                       | 50  | ns   |
| I <sup>2</sup> C™ Serial Data Setup Time                                                                                                         | t <sub>sds</sub> | 250           |      | 250                     |     | ns   |
| I <sup>2</sup> C™ Serial Data Hold Time                                                                                                          | t <sub>sdh</sub> | 0             |      | 0                       |     | μs   |
| I <sup>2</sup> C™ Input Rise Time <sup>2)</sup>                                                                                                  | t <sub>icr</sub> |               | 1000 |                         | 300 | ns   |
| I <sup>2</sup> C™ Input Fall Time <sup>2)</sup>                                                                                                  | t <sub>icf</sub> |               | 300  |                         | 300 | ns   |
| I <sup>2</sup> C™ Output Fall Time; 10pF to 400pF Bus <sup>2)</sup>                                                                              | t <sub>ocf</sub> |               | 300  |                         | 300 | ns   |
| I <sup>2</sup> C™ Bus Free Time Between Stop and Start                                                                                           | t <sub>buf</sub> | 4.7           |      | 1.3                     |     | μs   |
| I <sup>2</sup> C™ Start or Repeated Start Condition Setup Time                                                                                   | t <sub>sts</sub> | 4.7           |      | 0.6                     |     | μs   |
| I <sup>2</sup> C™ Start or Repeated Start Condition Hold Time                                                                                    | t <sub>sth</sub> | 4             |      | 0.6                     |     | μs   |
| I <sup>2</sup> C™ Stop Condition Setup Time <sup>2)</sup>                                                                                        | t <sub>sps</sub> | 4             |      | 0.6                     |     | μs   |
| <sup>1)</sup> The I <sup>2</sup> C™ interface will operate in either standard or fast mode.<br><sup>2)</sup> Parameter not tested in production. |                  |               |      |                         |     |      |

## 2 Functional Description

The ZSPM4521 is a fully-integrated Li-Ion battery charger IC based on a highly-efficient switching topology. It includes a maximum power point tracking (MPPT) function to optimize its input voltage in order to extract the maximum possible power from photovoltaic (PV) cells. It is configurable for termination voltage, charge current, and additional variables to allow optimum charging conditions for a wide range of Li-Ion batteries. A 1MHz internal switching frequency facilitates low-cost LC filter combinations. Figure 2.1 provides a block diagram.

When the battery voltage is below 3.0V, the ZSPM4521 enters a pre-charge state and applies a small, programmable charge current to safely charge the battery to a level for which full-charge current can be applied. Once the Full-Charge Mode has been initiated, the ZSPM4521 will maximize available charge current to the battery by adjusting its duty cycle to regulate its input voltage to the MPP voltage of the photovoltaic (PV) cell. If sufficient current is available from the PV cell to exceed the safe 1C charge rate of the battery, then the programmable 1C current limit function will take precedence over the MPPT control function and the PV cell voltage will rise above the MPP value.

**Figure 2.1 ZSPM4521 Block Diagram**



When the battery voltage has increased enough to go into maintenance mode, the PWM control loop will force a constant voltage across the battery. Once in Constant Voltage Mode, current is monitored to determine when the battery is fully charged. See Figure 2.2 for a diagram of the charging states.

The regulation voltage as well as the 1C charging current can be set to change based on the battery temperature. There are four temperature ranges for which the regulation voltage can be set independently: 0°C to 10°C, 10°C to 45°C, 45°C to 50°C, and 50°C to 60°C. The ZSPM4521 will stop charging if the temperature passes the descending temperature threshold at 0°C or the ascending threshold at 60°C. These thresholds have 10 degrees of hysteresis. The intermediate points have 1 degree of hysteresis.

## 2.1. Internal Protection

### 2.1.1. VIN Under-Voltage Lockout

The device is held in the off state until the EN pin voltage is HIGH ( $\geq 2.2V$ ) and VIN reaches 3.15V (typical). There is a 200mV hysteresis on this input, which requires the input to fall below 2.95V (typical) before the device will disable.

### 2.1.2. Internal Current Limit

The current through the inductor  $L_{OUT}$  is sensed on a cycle-by-cycle basis and if the current limit ( $I_{OCD}$ ; see section 1.4) is reached, the ZSPM4521 will abbreviate the cycle. The current limit is always active when the regulator is enabled.

### 2.1.3. Thermal Shutdown

If the junction temperature of the ZSPM4521 exceeds 170°C (typical), the SW output will tri-state to protect the device from damage. The NFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will attempt to start up again. If the device reaches 170°C, the shutdown/restart sequence will repeat.

### 2.1.4. VBAT Over-Voltage Protection

The ZSPM4521 has a battery protection circuit designed to shut down the charging profile if the battery voltage is greater than the termination voltage. The termination voltage can change based on user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the ZSPM4521 in a fault condition.

## 2.2. Fault Handling

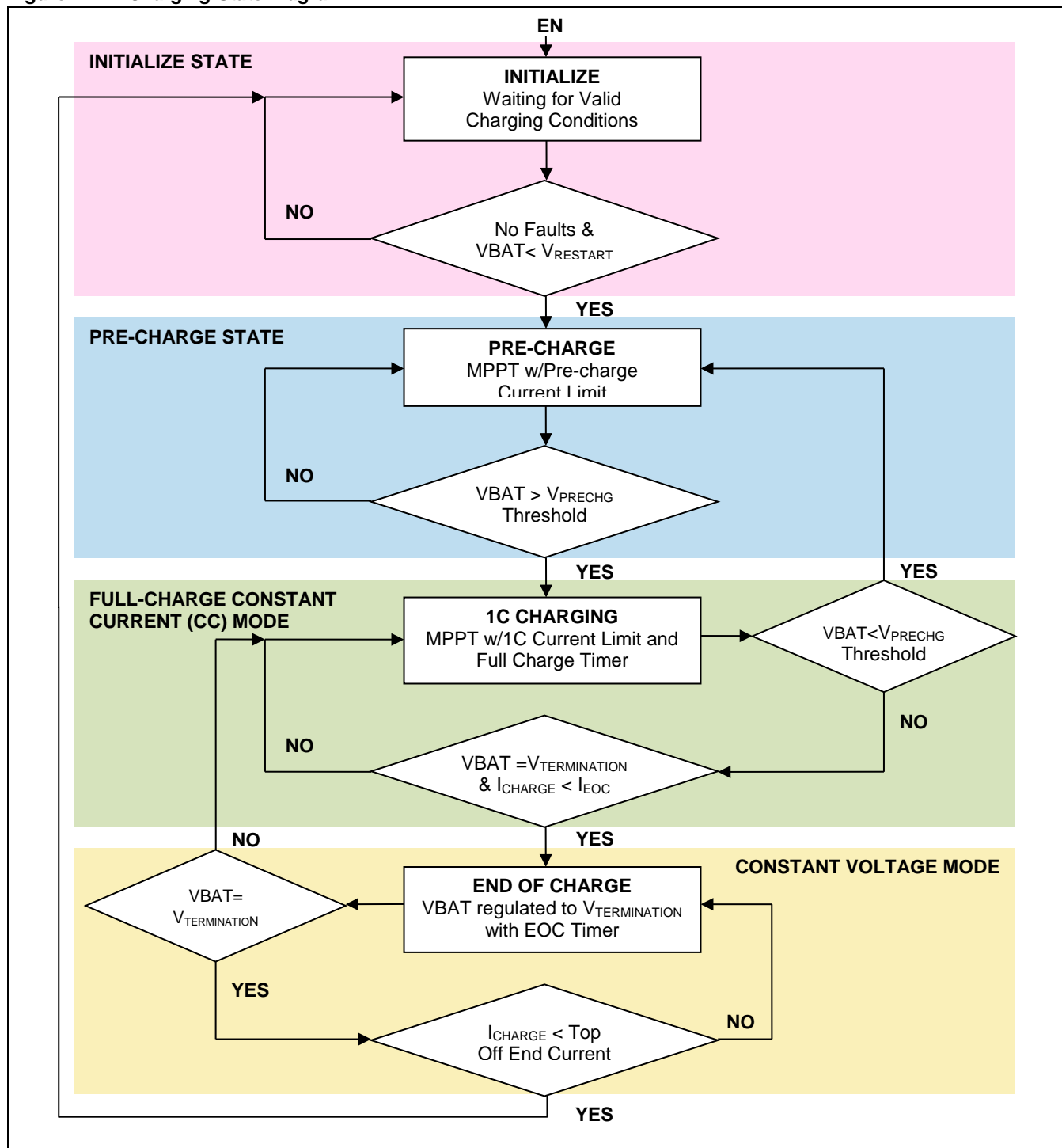
### 2.2.1. NFLT Pin Functionality

In the event of a battery over-voltage, the battery temperature being outside of the safe charging range, or the full charge timer expiring, charging stops and the NFLT pin is pulled low. When the fault condition is no longer present, the device will enter the INITIALIZE state (see Figure 2.2), but the NFLT pin will remain low until the STATUS register (00<sub>HEX</sub>) is read (see Table 2.2). When the STATUS register is read, the NFLT pin will go high until a new fault is detected.

### 2.2.2. Other Faults

When an open thermistor, thermal shutdown, VIN under-voltage, or top-off time-out are detected, charging immediately stops and the corresponding bit in the STATUS register (00<sub>HEX</sub>) is set. The device will enter the INITIALIZE state until the fault is no longer detected.

Figure 2.2 Charging State Diagram



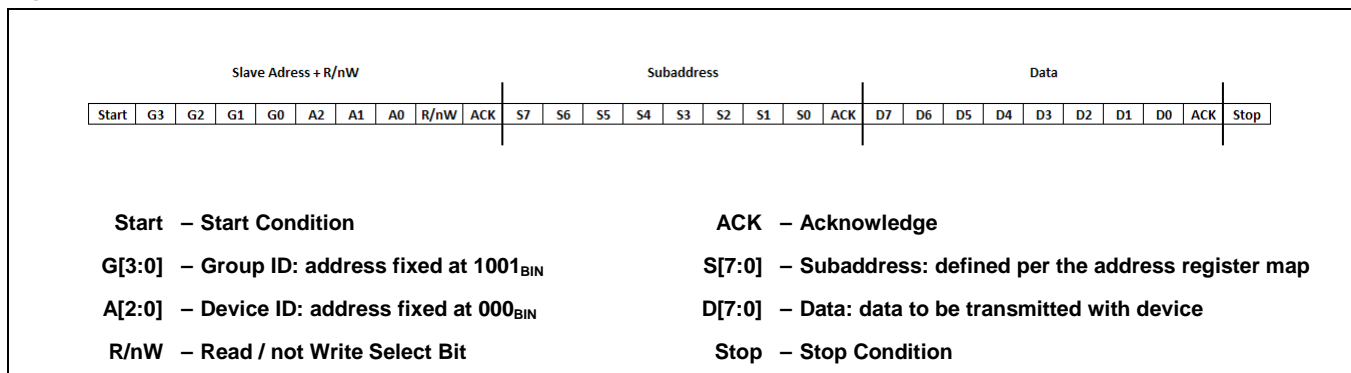
## 2.3. Serial Interface

The ZSPM4521 features an I<sup>2</sup>C™ slave interface that offers advanced control and diagnostic features. It supports standard and fast mode data rates and auto-sequencing, and it is compliant to I<sup>2</sup>C™ standard version 3.0.

I<sup>2</sup>C™ operation offers configuration control for termination voltages, charge currents, and charge timeouts. This configurability allows optimum charging conditions in a wide range of Li-Ion batteries. I<sup>2</sup>C™ operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS register is set and the NFLT pin is pulled low. Whenever a warning is detected, the associated status bit in the STATUS register is set, but the NFLT pin is not pulled low. Reading the STATUS register resets the fault and warning status bits, and the NFLT pin is released after all fault status bits have been reset.

### 2.3.1. I<sup>2</sup>C™ Subaddress Definition

**Figure 2.3 Subaddress in I<sup>2</sup>C™ Transmission**



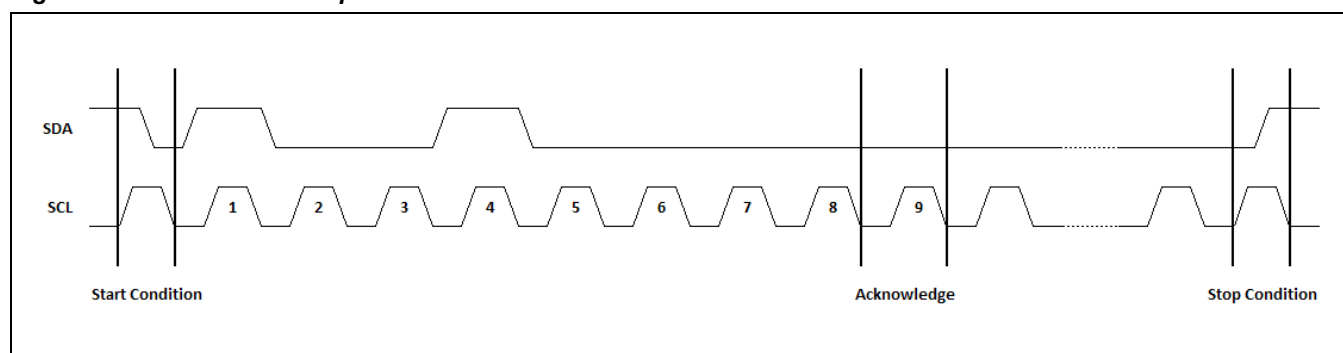
### 2.3.2. I<sup>2</sup>C™ Bus Operation

The ZSPM4521's I<sup>2</sup>C™ is a two-wire serial interface; the two lines are serial clock (SCL) and serial data (SDA) (see Figure 2.4). SDA must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. To ensure proper operation, setup and hold times must be met (see Table 1.5). The device that initiates the I<sup>2</sup>C™ transaction becomes the master of the bus.

Communication is initiated by the master sending a START condition, which is a high-to-low transition on SDA while the SCL line is high. After the START condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (read = 1; write = 0). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK-related clock pulse. On the I<sup>2</sup>C™ bus, during each clock pulse, only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as START or STOP control conditions. A low-to-high transition on SDA while the SCL input is high indicates a STOP condition and is sent by the master.

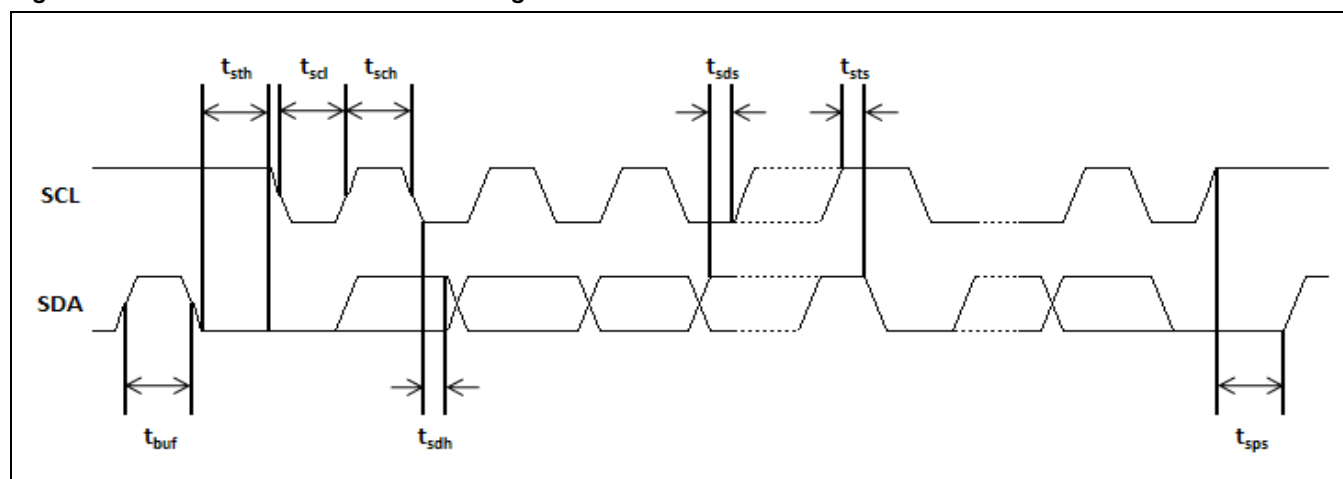
Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit from the receiver. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a STOP condition.

**Figure 2.4**  $I^2C^{\text{TM}}$  Start / Stop Protocol



See Table 1.5 for the definitions and specifications for the timing parameters labeled in Figure 2.5.

**Figure 2.5**  $I^2C^{\text{TM}}$  Data Transmission Timing





## 2.4. Status and Configuration Registers

**Table 2.1 Register Descriptions (Device Address = 48<sub>HEX</sub>)**

| Register | Address           | Name                      | Default           | Description                          |
|----------|-------------------|---------------------------|-------------------|--------------------------------------|
| 0        | 00 <sub>HEX</sub> | STATUS                    | 00 <sub>HEX</sub> | Status bit register                  |
| 1        | N/A               | N/A                       | N/A               | Register not implemented             |
| 2        | 02 <sub>HEX</sub> | CONFIG1 <sup>1)</sup>     | EEPROM            | Configuration register               |
| 3        | 03 <sub>HEX</sub> | CONFIG2 <sup>1)</sup>     | EEPROM            | Configuration register               |
| 4        | 04 <sub>HEX</sub> | CONFIG3 <sup>1)</sup>     | EEPROM            | Configuration register               |
| 5        | 05 <sub>HEX</sub> | CONFIG4 <sup>1)</sup>     | EEPROM            | Configuration register               |
| 6        | 06 <sub>HEX</sub> | CONFIG5 <sup>1)</sup>     | EEPROM            | Configuration register               |
| 7-16     | N/A               | N/A                       | N/A               | Registers not implemented            |
| 17       | 11 <sub>HEX</sub> | CONFIG_ENABLE             | 00 <sub>HEX</sub> | Enable configuration register access |
| 18       | 12 <sub>HEX</sub> | EEPROM_CTRL <sup>1)</sup> | 00 <sub>HEX</sub> | EEPROM control register              |

<sup>1)</sup> CONFIGx and EEPROM\_CTRL registers are only accessible when the CONFIG\_ENABLE register is written with the EN\_CFG bit set to 1 (see Table 2.8).

**Table 2.2 STATUS Register—Address 00<sub>HEX</sub>**

Note: All of the STATUS register bits are READ-only.

| DATA BIT   | D7                                               | D6    | D5      | D4       | D3  | D2     | D1     | D0      |
|------------|--------------------------------------------------|-------|---------|----------|-----|--------|--------|---------|
| FIELD NAME | BATT_OV                                          | 1C_TO | TEMP_0C | TEMP_60C | TSD | TOP_TO | VIN_UV | TH_OPEN |
| FIELD NAME | BIT DEFINITION <sup>1)</sup>                     |       |         |          |     |        |        |         |
| BATT_OV    | VBAT over-voltage.                               |       |         |          |     |        |        |         |
| 1C_TO      | Full charge timer has timed out.                 |       |         |          |     |        |        |         |
| TEMP_0C    | Thermistor indicates battery temperature < 0°C.  |       |         |          |     |        |        |         |
| TEMP_60C   | Thermistor indicates battery temperature > 60°C. |       |         |          |     |        |        |         |
| TSD        | Thermal shutdown.                                |       |         |          |     |        |        |         |
| TOP_TO     | Top-off timer has timed out.                     |       |         |          |     |        |        |         |
| VIN_UV     | VIN under-voltage.                               |       |         |          |     |        |        |         |
| TH_OPEN    | Thermistor open (battery not present).           |       |         |          |     |        |        |         |

<sup>1)</sup> Faults are defined as BATT\_OV, 1C\_TO, TEMP\_0C, and TEMP\_60C. Warnings are defined as TSD, TOP\_TO, VIN\_UV, and TH\_OPEN. Faults cause the NFLT pin to be pulled low. Warnings do not cause the NFLT pin to be pulled low. All status bits are cleared after STATUS register read access. The NFLT pin will go to high impedance (open-drain output) after the STATUS register has been read and all status bits have been reset.

**Table 2.3 Configuration Register CONFIG1—Address 02<sub>HEX</sub>**

Note: All of the CONFIG1 register bits are READ/WRITE.

| DATA BIT                                                                                                                                                                                                                                                                                    | D7            | D6                                            | D5               | D4                                                                                                              | D3 | D2                                                                 | D1 | D0 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------|----|--------------------------------------------------------------------|----|----|
| FIELD NAME                                                                                                                                                                                                                                                                                  | PRE_CHRG[1:0] |                                               | V_TERM_0_10[2:0] |                                                                                                                 |    | V_TERM_10_45[2:0]                                                  |    |    |
| FIELD NAME                                                                                                                                                                                                                                                                                  |               | BIT DEFINITION                                |                  |                                                                                                                 |    |                                                                    |    |    |
| PRE_CHRG[1:0] <sup>1)</sup>                                                                                                                                                                                                                                                                 |               | Pre-charging configuration                    |                  | 00 <sub>BIN</sub> – 50mA<br>01 <sub>BIN</sub> – 100mA<br>10 <sub>BIN</sub> – 185mA<br>11 <sub>BIN</sub> – 370mA |    |                                                                    |    |    |
| V_TERM_0_10[2:0] <sup>2)</sup>                                                                                                                                                                                                                                                              |               | Voltage termination:<br>0-10°C configuration  |                  | 000 <sub>BIN</sub> – 3.94V<br>001 <sub>BIN</sub> – 4.00V                                                        |    | 100 <sub>BIN</sub> – 4.12V<br>101 <sub>BIN</sub> – 4.15V           |    |    |
| V_TERM_10_45[2:0] <sup>2)</sup>                                                                                                                                                                                                                                                             |               | Voltage termination:<br>10-45°C configuration |                  | 010 <sub>BIN</sub> – 4.05V<br>011 <sub>BIN</sub> – 4.10V                                                        |    | 110 <sub>BIN</sub> – 4.18V<br>111 <sub>BIN</sub> – Invalid setting |    |    |
| 1) PRE_CHRG Note: Maximum output current when V <sub>BAT</sub> < 3.0V.<br>2) V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.4 for 45-50°C and 50-60°C). For <0°C and >60°C, charging is disabled and a fault is set. |               |                                               |                  |                                                                                                                 |    |                                                                    |    |    |

**Table 2.4 Configuration Register CONFIG2—Address 03<sub>HEX</sub>**

Note: All of the CONFIG2 register bits are READ/WRITE.

| DATA BIT                                                                                                                                                                                                         | D7       | D6                                            | D5                | D4 | D3                                                                                                                             | D2                | D1 | D0 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----------------------------------------------|-------------------|----|--------------------------------------------------------------------------------------------------------------------------------|-------------------|----|----|
| FIELD NAME                                                                                                                                                                                                       | EOC[1:0] |                                               | V_TERM_45_50[2:0] |    |                                                                                                                                | V_TERM_50_60[2:0] |    |    |
| FIELD NAME                                                                                                                                                                                                       |          | BIT DEFINITION                                |                   |    |                                                                                                                                |                   |    |    |
| EOC[1:0] <sup>1)</sup>                                                                                                                                                                                           |          | End of charge configuration                   |                   |    | 00 <sub>BIN</sub> – 50mA<br>01 <sub>BIN</sub> – 100mA<br>10 <sub>BIN</sub> – 185mA<br>11 <sub>BIN</sub> – 370mA                |                   |    |    |
| V_TERM_45_50[2:0] <sup>2)</sup>                                                                                                                                                                                  |          | Voltage termination:<br>45-50°C configuration |                   |    | 000 <sub>BIN</sub> – 3.94V<br>001 <sub>BIN</sub> – 4.00V                                                                       |                   |    |    |
| V_TERM_50_60[2:0] <sup>2)</sup>                                                                                                                                                                                  |          | Voltage termination:<br>50-60°C configuration |                   |    | 010 <sub>BIN</sub> – 4.05V<br>011 <sub>BIN</sub> – 4.10V                                                                       |                   |    |    |
|                                                                                                                                                                                                                  |          |                                               |                   |    | 100 <sub>BIN</sub> – 4.12V<br>101 <sub>BIN</sub> – 4.15V<br>110 <sub>BIN</sub> – 4.18V<br>111 <sub>BIN</sub> – Invalid setting |                   |    |    |
| 1) EOC Note: Maximum output current when V <sub>BAT</sub> ≥ 3.0V.                                                                                                                                                |          |                                               |                   |    |                                                                                                                                |                   |    |    |
| 2) V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.3 for 0-10°C and 10-45°C). For <0°C and >60°C, charging is disabled and a fault is set. |          |                                               |                   |    |                                                                                                                                |                   |    |    |

**Table 2.5 Configuration Register CONFIG3—Address 04<sub>HEX</sub>**

Note: All of the CONFIG3 register bits are READ/WRITE.

| DATA BIT                                                                                                                                                                                                                | D7                      | D6                                               | D5 | D4 | D3                          | D2 | D1                           | D0 |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|--------------------------------------------------|----|----|-----------------------------|----|------------------------------|----|
| FIELD NAME                                                                                                                                                                                                              | MAX_CHRG_CURR_0_10[3:0] |                                                  |    |    | MAX_CHRG_CURR_10_45[3:0]    |    |                              |    |
| FIELD NAME                                                                                                                                                                                                              |                         | BIT DEFINITION                                   |    |    |                             |    |                              |    |
| MAX_CHRG_CURR_0_10[3:0] <sup>1)</sup>                                                                                                                                                                                   |                         | Maximum charge current:<br>0-10°C configuration  |    |    | 0000 <sub>BIN</sub> – 50mA  |    | 1000 <sub>BIN</sub> – 800mA  |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0001 <sub>BIN</sub> – 100mA |    | 1001 <sub>BIN</sub> – 900mA  |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0010 <sub>BIN</sub> – 200mA |    | 1010 <sub>BIN</sub> – 1000mA |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0011 <sub>BIN</sub> – 300mA |    | 1011 <sub>BIN</sub> – 1100mA |    |
| MAX_CHRG_CURR_10_45[3:0] <sup>1)</sup>                                                                                                                                                                                  |                         | Maximum charge current;<br>10-45°C configuration |    |    | 0100 <sub>BIN</sub> – 400mA |    | 1100 <sub>BIN</sub> – 1200mA |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0101 <sub>BIN</sub> – 500mA |    | 1101 <sub>BIN</sub> – 1300mA |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0110 <sub>BIN</sub> – 600mA |    | 1110 <sub>BIN</sub> – 1400mA |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    | 0111 <sub>BIN</sub> – 700mA |    | 1111 <sub>BIN</sub> – 1500mA |    |
|                                                                                                                                                                                                                         |                         |                                                  |    |    |                             |    |                              |    |
| 1) MAX_CHRG_CURR Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C (see Table 2.6 for 45-50°C and 50-60°C). For <0°C and >60°C, charging is disabled and a fault is set. |                         |                                                  |    |    |                             |    |                              |    |

**Table 2.6 Configuration Register CONFIG4—Address 05<sub>HEX</sub>**

Note: All of the CONFIG4 register bits are READ/WRITE.

| DATA BIT                                                                                                                                                                                                               | D7                       | D6 | D5                                               | D4 | D3                          | D2 | D1                           | D0 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----|--------------------------------------------------|----|-----------------------------|----|------------------------------|----|
| FIELD NAME                                                                                                                                                                                                             | MAX_CHRG_CURR_45_50[3:0] |    |                                                  |    | MAX_CHRG_CURR_50_60[3:0]    |    |                              |    |
| FIELD NAME                                                                                                                                                                                                             |                          |    | BIT DEFINITION                                   |    |                             |    |                              |    |
| MAX_CHRG_CURR_45_50[3:0] <sup>1)</sup>                                                                                                                                                                                 |                          |    | Maximum charge current:<br>45-50°C configuration |    | 0000 <sub>BIN</sub> – 50mA  |    | 1000 <sub>BIN</sub> – 800mA  |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0001 <sub>BIN</sub> – 100mA |    | 1001 <sub>BIN</sub> – 900mA  |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0010 <sub>BIN</sub> – 200mA |    | 1010 <sub>BIN</sub> – 1000mA |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0011 <sub>BIN</sub> – 300mA |    | 1011 <sub>BIN</sub> – 1100mA |    |
| MAX_CHRG_CURR_50_60[3:0] <sup>1)</sup>                                                                                                                                                                                 |                          |    | Maximum charge current:<br>50-60°C configuration |    | 0100 <sub>BIN</sub> – 400mA |    | 1100 <sub>BIN</sub> – 1200mA |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0101 <sub>BIN</sub> – 500mA |    | 1101 <sub>BIN</sub> – 1300mA |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0110 <sub>BIN</sub> – 600mA |    | 1110 <sub>BIN</sub> – 1400mA |    |
|                                                                                                                                                                                                                        |                          |    |                                                  |    | 0111 <sub>BIN</sub> – 700mA |    | 1111 <sub>BIN</sub> – 1500mA |    |
| 1) MAX_CHRG_CURR Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C (see Table 2.5 for 0-10°C and 10-45°C). For <0°C and >60°C, charging is disabled and a fault is set. |                          |    |                                                  |    |                             |    |                              |    |

**Table 2.7 Configuration Register CONFIG5—Address 06<sub>HEX</sub>**

Note: All of the CONFIG5 register bits are READ/WRITE.

| DATA BIT                                                                                                                                                                                                                                                                                                               | D7      | D6                                                                                                                                                                                                                                                                                                                                                        | D5          | D4 | D3 | D2         | D1 | D0 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|----|----|------------|----|----|
| FIELD NAME                                                                                                                                                                                                                                                                                                             | TOP_END | TH                                                                                                                                                                                                                                                                                                                                                        | TOP_TO[2:0] |    |    | 1C_TO[2:0] |    |    |
| FIELD NAME                                                                                                                                                                                                                                                                                                             |         | BIT DEFINITION                                                                                                                                                                                                                                                                                                                                            |             |    |    |            |    |    |
| TOP_END <sup>1)</sup>                                                                                                                                                                                                                                                                                                  |         | Top-off end configuration<br>0 <sub>BIN</sub> – 25mA<br>1 <sub>BIN</sub> – 92mA                                                                                                                                                                                                                                                                           |             |    |    |            |    |    |
| TH <sup>2)</sup>                                                                                                                                                                                                                                                                                                       |         | Thermistor configuration<br>0 <sub>BIN</sub> – 10kΩ<br>1 <sub>BIN</sub> – 100kΩ                                                                                                                                                                                                                                                                           |             |    |    |            |    |    |
| TOP_TO[2:0] <sup>3)</sup>                                                                                                                                                                                                                                                                                              |         | Top off timer time out configuration<br>000 <sub>BIN</sub> – 0 minutes<br>001 <sub>BIN</sub> – 20 minutes<br>010 <sub>BIN</sub> – 40 minutes<br>011 <sub>BIN</sub> – 60 minutes<br>100 <sub>BIN</sub> – 80 minutes<br>101 <sub>BIN</sub> – 100 minutes<br>110 <sub>BIN</sub> – 120 minutes<br>111 <sub>BIN</sub> – Disable time out timer                 |             |    |    |            |    |    |
| 1C_TO[2:0] <sup>4)</sup>                                                                                                                                                                                                                                                                                               |         | Full charge timer time out configuration<br>000 <sub>BIN</sub> – Disable full charge timer<br>001 <sub>BIN</sub> – 200 minutes<br>010 <sub>BIN</sub> – 400 minutes<br>011 <sub>BIN</sub> – 600 minutes<br>100 <sub>BIN</sub> – 800 minutes<br>101 <sub>BIN</sub> – 1000 minutes<br>110 <sub>BIN</sub> – 1200 minutes<br>111 <sub>BIN</sub> – 1400 minutes |             |    |    |            |    |    |
| 1) TOP_END Note: Charging stops when $V_{VBAT} = V_{TERMINATION}$ and $I_{OUT} < TOP\_END$<br>2) TH Note: Setting for nominal thermistor and reference resistor value.<br>3) TOP_TO Note: Timer starts when $V_{VBAT} = V_{TERMINATION}$ and $I_{OUT} < EOC$ .<br>4) 1C_TO Note: Timer starts when $V_{VBAT} > 3.0V$ . |         |                                                                                                                                                                                                                                                                                                                                                           |             |    |    |            |    |    |

**Table 2.8 Enable Configuration Register CONFIG\_ENABLE—Address 11<sub>HEX</sub>**

Note: The reset value for all of the CONFIG\_ENABLE register bits is 0.

| DATA BIT   | D7       | D6                                                                                                                                                                                                         | D5       | D4       | D3       | D2       | D1       | D0     |
|------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|----------|----------|----------|--------|
| FIELD NAME | Not used | Not used                                                                                                                                                                                                   | Not used | Not used | Not used | Not used | Not used | EN_CFG |
| READ/WRITE | R        | R                                                                                                                                                                                                          | R        | R        | R        | R        | R        | R/W    |
| FIELD NAME |          | BIT DEFINITION                                                                                                                                                                                             |          |          |          |          |          |        |
| EN_CFG     |          | Enable-access control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02 <sub>HEX</sub> to 06 <sub>HEX</sub> )<br>0 <sub>BIN</sub> – Disable access<br>1 <sub>BIN</sub> – Enable access |          |          |          |          |          |        |

**Table 2.9 EEPROM Control Register EEPROM\_CTRL—Address 12<sub>HEX</sub>**

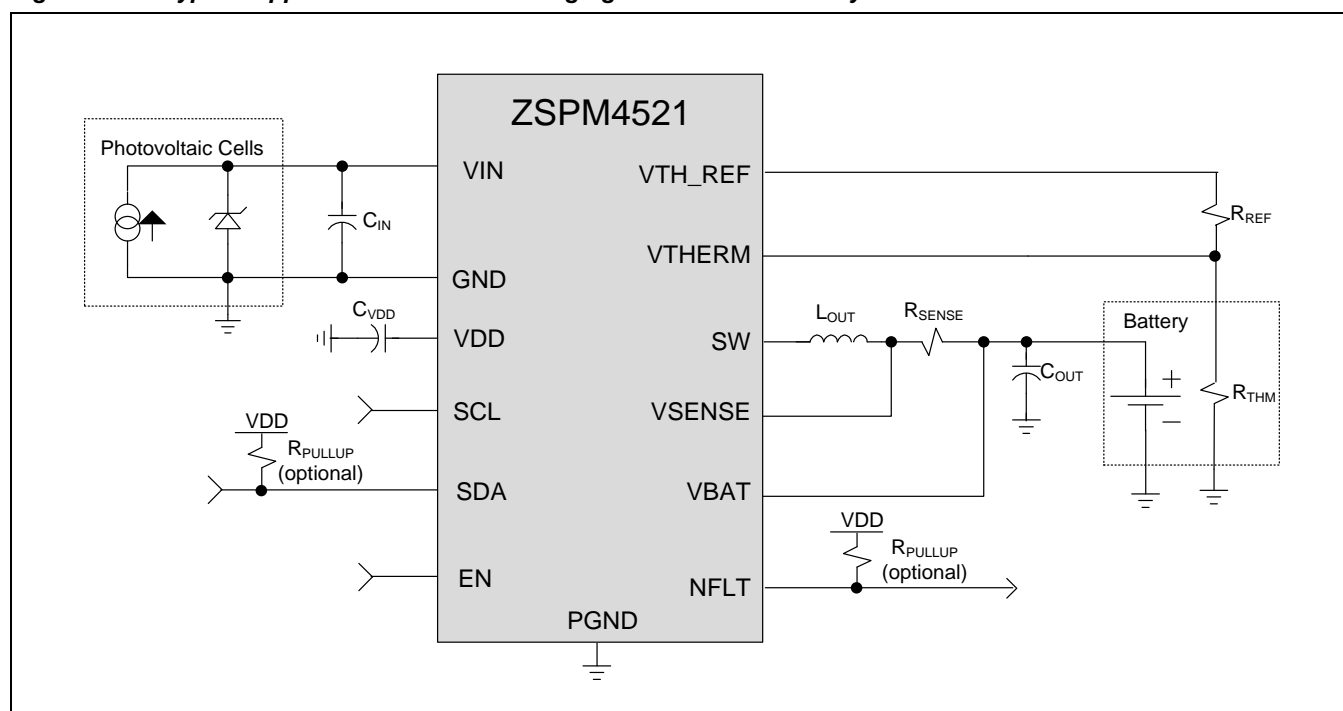
Note: The reset value for all of the EEPROM\_CTRL register bits is 0.

| DATA BIT                                                      | D7       | D6                                                                                                                                                                                                                                                                                                                                                             | D5       | D4       | D3       | D2       | D1       | D0      |
|---------------------------------------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|----------|----------|----------|---------|
| FIELD NAME                                                    | Not used | Not used                                                                                                                                                                                                                                                                                                                                                       | Not used | Not used | Not used | Not used | Not used | EE_PROG |
| READ/WRITE                                                    | R        | R                                                                                                                                                                                                                                                                                                                                                              | R        | R        | R        | R        | R        | R/W     |
| FIELD NAME                                                    |          | BIT DEFINITION                                                                                                                                                                                                                                                                                                                                                 |          |          |          |          |          |         |
| EE_PROG <sup>1)</sup>                                         |          | EEPROM program control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02 <sub>HEX</sub> to 06 <sub>HEX</sub> )<br><br>0 <sub>BIN</sub> – Disable EEPROM programming<br><br>1 <sub>BIN</sub> – Enable EEPROM programming with data from configuration registers CONFIG1 through CONFIG5 (addresses 02 <sub>HEX</sub> to 06 <sub>HEX</sub> ) |          |          |          |          |          |         |
| 1) EE_PROG Note: Inputs VIN and EN must be present for 200ms. |          |                                                                                                                                                                                                                                                                                                                                                                |          |          |          |          |          |         |

## 3 Application Circuits

### 3.1. Typical Application Circuit

**Figure 3.1** Typical Application Circuit for Charging a Lithium-Ion Battery via Photovoltaic Cells



### 3.2. Selection of External Components

Note that the internal compensation is optimized for a  $4.7\mu\text{F}$  output capacitor ( $C_{OUT}$ ) and a  $4.7\mu\text{H}$  output inductor ( $L_{OUT}$ ). Table 1.3 provides recommended ranges for most of the following components.

#### 3.2.1. $C_{OUT}$ Output Capacitor

To keep the output ripple low, a low ESR (less than  $35\text{m}\Omega$ ) ceramic capacitor is recommended for the  $4.7\mu\text{F}$  output filter capacitor. The ESR should not exceed  $100\text{m}\Omega$ .

#### 3.2.2. $L_{OUT}$ Output Inductor

For best performance, an inductor with a saturation current rating higher than the maximum  $V_{OUT}$  load requirement plus the inductor current ripple should be used for the  $4.7\mu\text{H}$  output filter inductor.

#### 3.2.3. $C_{IN}$ Bypass Capacitor for Input from Photovoltaic Source

For best performance, a low ESR ceramic capacitor should be used for the  $10\mu\text{F}$  input supply bypass capacitor. If it is not a low ESR ceramic capacitor, a  $0.1\mu\text{F}$  ceramic capacitor should be added in parallel to  $C_{IN}$ .

#### 3.2.4. **C<sub>VDD</sub> Bypass Capacitor for VDD Internal Reference Voltage Output**

For best performance, a low ESR ceramic capacitor should be used for the 100nF bypass capacitor from the VDD pin to ground.

#### 3.2.5. **R<sub>SENSE</sub> Output Sensing Resistor**

The typical value for the output sensing resistor is 50mΩ.

#### 3.2.6. **Pull-up Resistors**

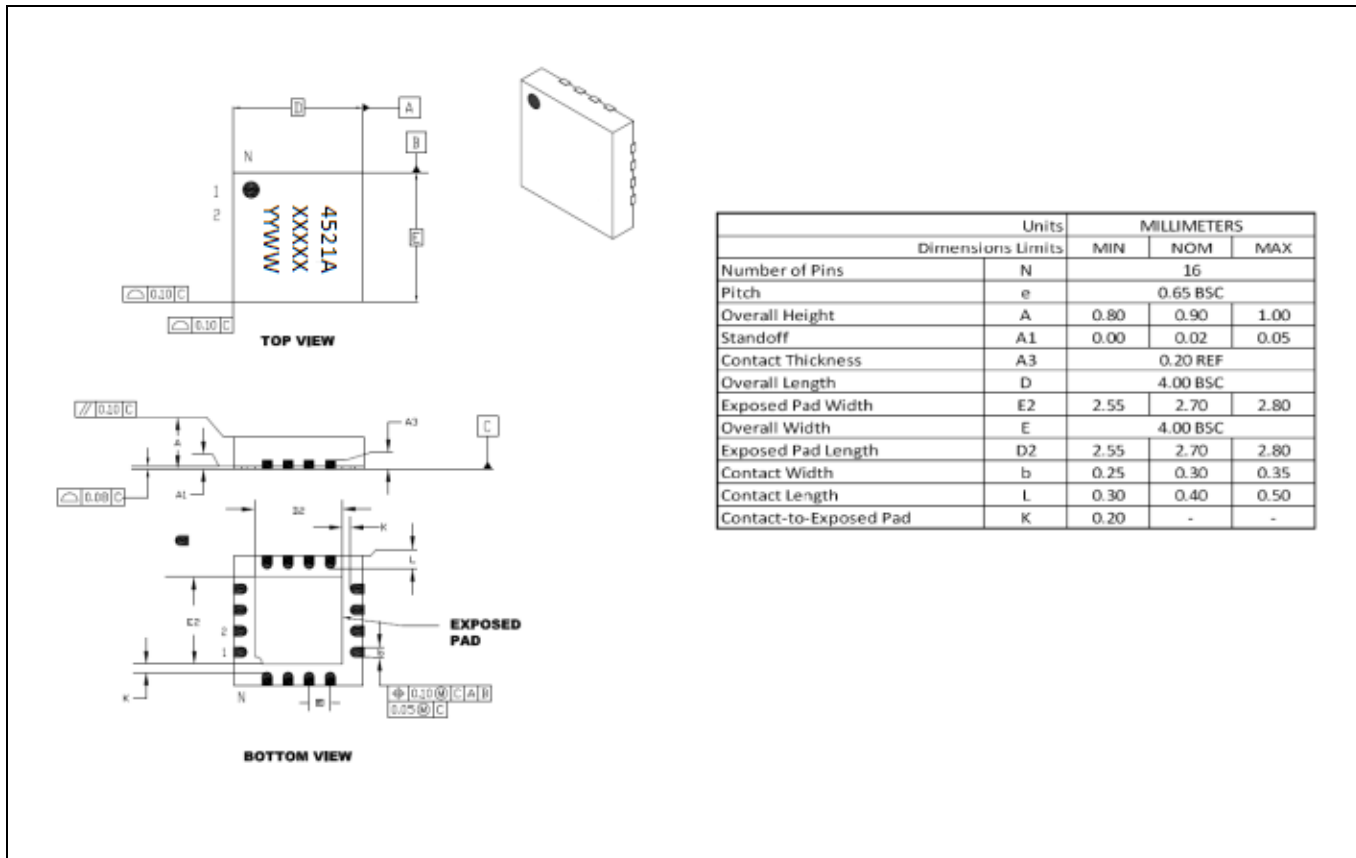
For proper function of the I<sup>2</sup>C™ interface, the SDA pin must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor.

For proper function of the fault-warning signal on the NFLT pin, it must be connected to a positive supply (VDD) through an external pull-up resistor.

## 4 Pin Configuration and Package

### 4.1. ZSPM4521 Package Dimensions

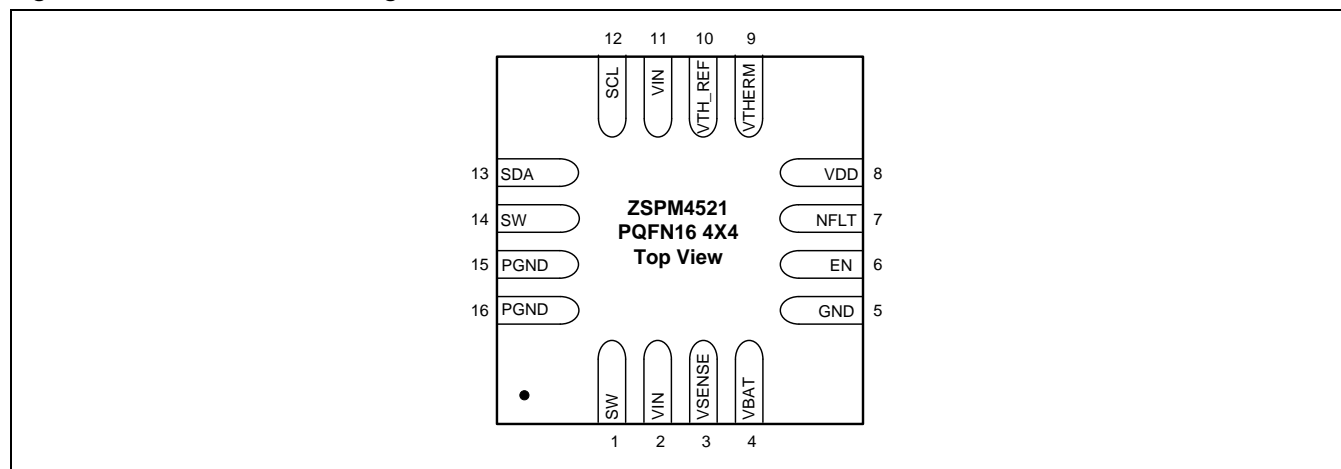
Figure 4.1 PQFN-16 Package Dimensions





## 4.2. Pin-Out Assignments

**Figure 4.2 ZSPM4521 Pin Assignments**



## 4.3. Pin Description for 16-Pin PQFN (4 x 4 mm)

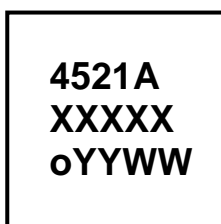
**Table 4.1 Pin Description**

| Pin # | Name   | Function                              | Description                                                                                                              |
|-------|--------|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| 1     | SW     | Switching Voltage Node                | Connect to $L_{OUT}$ 4.7 $\mu$ H (typical) inductor. Also connect to additional SW pin 14.                               |
| 2     | VIN    | Photovoltaic Input Voltage            | Input voltage from the photovoltaic cell. Also connect to $C_{IN}$ . Also connect to additional VIN pin 11.              |
| 3     | VSENSE | Current Sense Positive Input          | Positive input for the MPPT current loop.                                                                                |
| 4     | VBAT   | Output Voltage                        | Regulator feedback input.                                                                                                |
| 5     | GND    | GND                                   | Primary ground for the majority of the device except the low-side power FET.                                             |
| 6     | EN     | Enable Input                          | When EN is high ( $\geq 2.2V$ ), the device is enabled. Ground the pin to disable the device. Includes internal pull-up. |
| 7     | NFLT   | Inverted Fault                        | Open-drain output.                                                                                                       |
| 8     | VDD    | Internal 3.3V Supply Output           | Connect to a 100nF capacitor to GND.                                                                                     |
| 9     | VTERM  | Battery Temperature Sensor Minus Node | Negative node for the thermistor, which must be located in close proximity to the battery.                               |

| Pin # | Name    | Function                                 | Description                                                                                    |
|-------|---------|------------------------------------------|------------------------------------------------------------------------------------------------|
| 10    | VTH_REF | Battery Temperature Sensor Positive Node | Positive node for the thermistor, which must be located in close proximity to the battery.     |
| 11    | VIN     | Photovoltaic Input Voltage               | Additional VIN pin for input voltage from the photovoltaic cell; connect to VIN pin 2.         |
| 12    | SCL     | Clock Input                              | I <sup>2</sup> C™ clock input.                                                                 |
| 13    | SDA     | Data Input/Output                        | I <sup>2</sup> C™ data (open-drain output).                                                    |
| 14    | SW      | Switching Voltage Node                   | Additional SW pin; connect to SW pin 1.                                                        |
| 15    | PGND    | Power GND                                | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 16. |
| 16    | PGND    | Power GND                                | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 15. |

#### 4.4. Package Markings

Figure 4.3 Marking Diagram 16-Pin PQFN (4 x 4 mm)



XXXXX: Lot Number (last five digits)  
O: Pin 1 mark  
YY: Year  
WW: Work Week

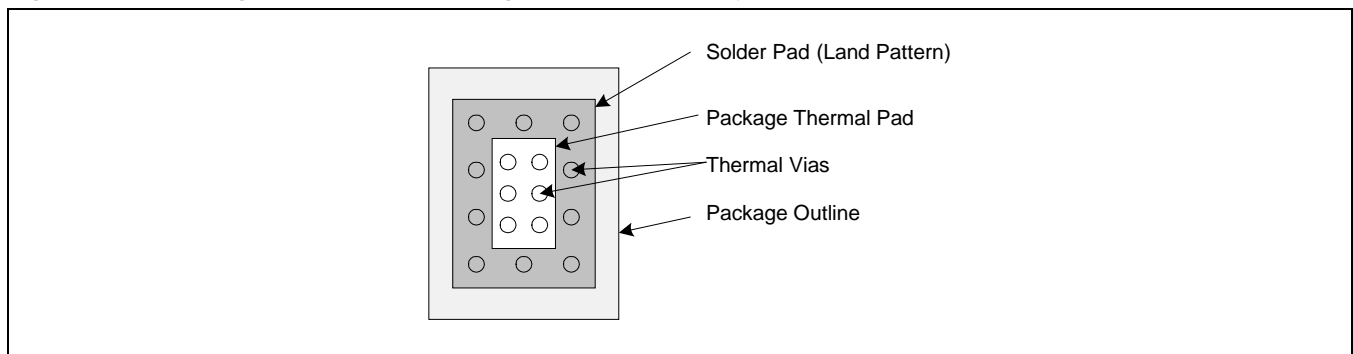
## 5 Layout Recommendations

To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

### 5.1. Multi-Layer PCB Layout

The following are guidelines for mounting the exposed pad ZSPM4521 on a multi-layer PCB with ground a plane. In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, and thickness of copper, etc.

**Figure 5.1 Package and PCB Land Configuration for Multi-Layer PCB**



**Figure 5.2 JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View**

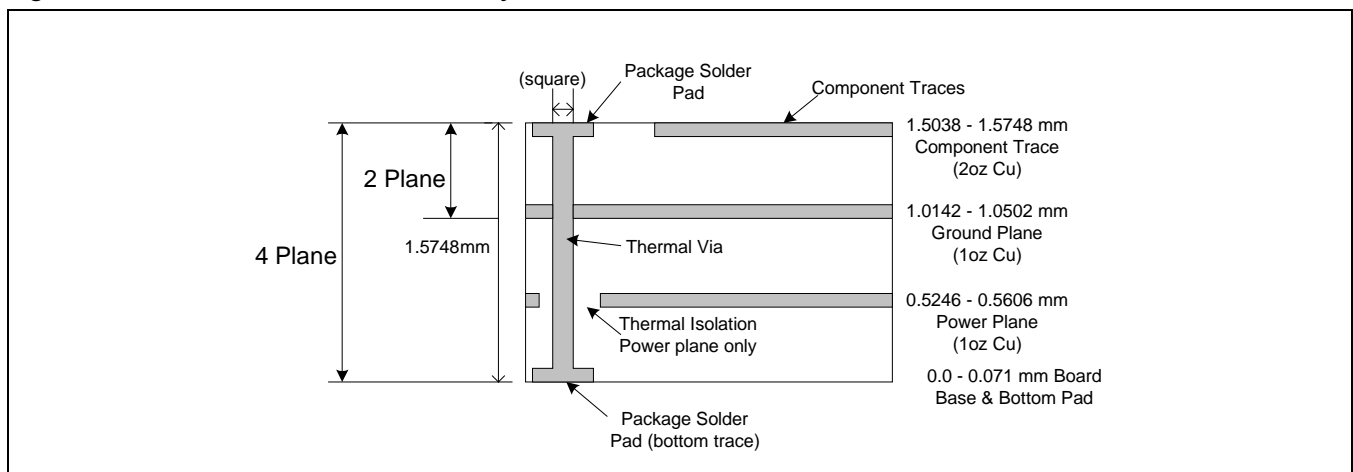
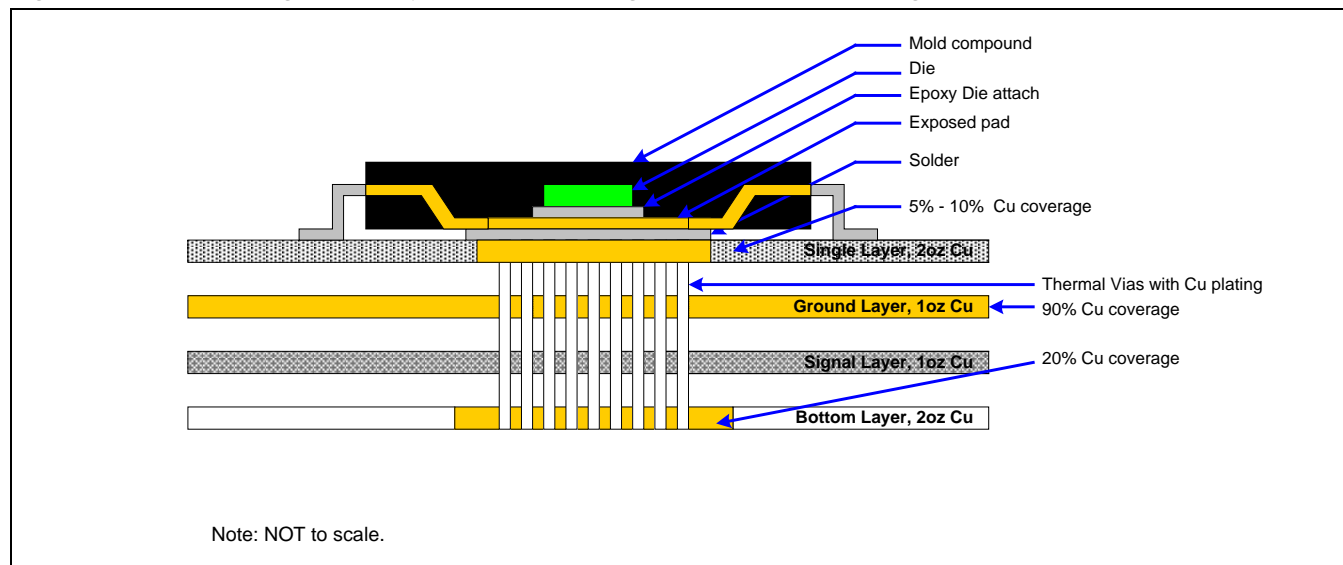


Figure 5.3 is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations, and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators might need to be de-rated for higher ambient temperatures. The de-rated value will depend on calculated worst-case power dissipation and the thermal management implementation in the application.

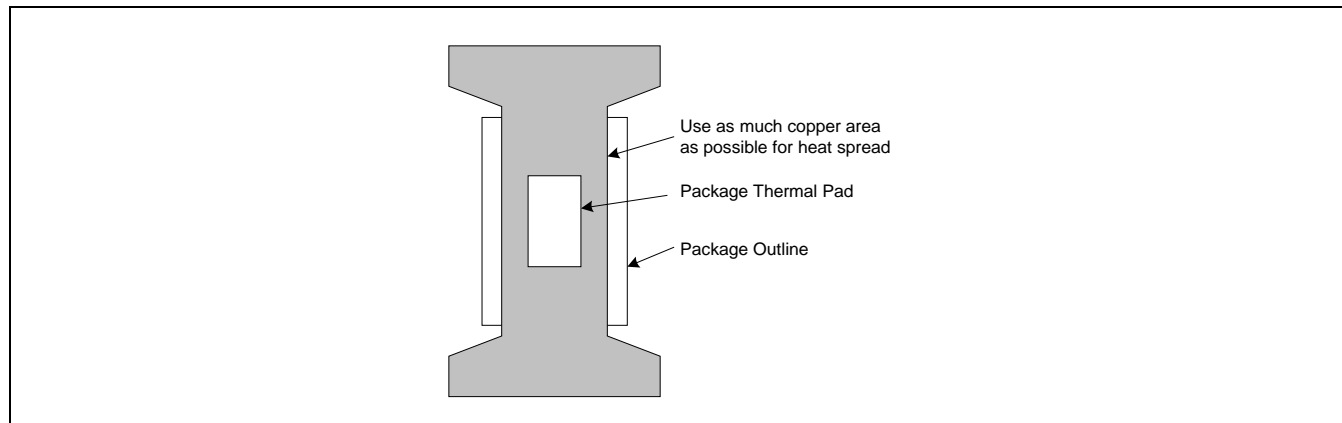
**Figure 5.3 Conducting Heat Away from the Die using an Exposed Pad Package**



## 5.2. Single-Layer PCB Layout

Layout recommendations for a single-layer PCB: Utilize as much copper area for power management as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as much copper trace as possible to dissipate the heat.

**Figure 5.4 Application Using a Single-Layer PCB**

**Important:** If the attachment method is NOT implemented correctly, the functionality of the product is NOT guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

## 6 Ordering Information

| Ordering Code | Description                                                              | Package                             |
|---------------|--------------------------------------------------------------------------|-------------------------------------|
| ZSPM4521AA1W  | ZSPM4521 High Efficiency Li-Ion Battery Charger for Photovoltaic Sources | 16-pin PQFN / 7" Reel (1000 parts)  |
| ZSPM4521AA1R  | ZSPM4521 High Efficiency Li-Ion Battery Charger for Photovoltaic Sources | 16-pin PQFN / 13" Reel (3300 parts) |
| ZSPM4521KIT   | ZSPM4521 Evaluation Kit                                                  |                                     |

## 7 Related Documents

| Document                                                                                   |
|--------------------------------------------------------------------------------------------|
| <i>ZSPM4521 Feature Sheet</i>                                                              |
| <i>ZSPM4521 Evaluation Kit Description</i>                                                 |
| <i>ZSPM4521 Application Note – Solar Powered Battery Management and Charging Solutions</i> |

Visit IDT's website [www.IDT.com](http://www.IDT.com) or contact your nearest sales office for the latest version of these documents.

## 8 Document Revision History

| Revision | Date              | Description                                                                                                                             |
|----------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 1.00     | February 14, 2013 | First release.                                                                                                                          |
| 1.01     | October 3, 2014   | Revision of specification for VTH_REF output voltage in Table 1.4.<br>Updates for contact information and imagery on cover and headers. |
|          | January 27, 2016  | Changed to IDT branding.                                                                                                                |



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