mem_test

Documentation

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1 Introduction

The purpose of this IP is to test memories connected to the AXI bus. The block allows writing and checking patterns over a large memory area quickly (one transfer every clock cycle) compared to software.

1.1 Feature List

- Up to 64-bit address space
- 16-1024 bit data width
- Configurable memory range to work on
- High-performance (back-to back write/read operations)
- Single execution and continuous execution possible
- Different patterns
    - Write own address to each location
    - Walking 1s
    - Counter
    - Pseudo Random Numbers
- Integrated error counters
- Latching of the address of the first error

2 Test Description

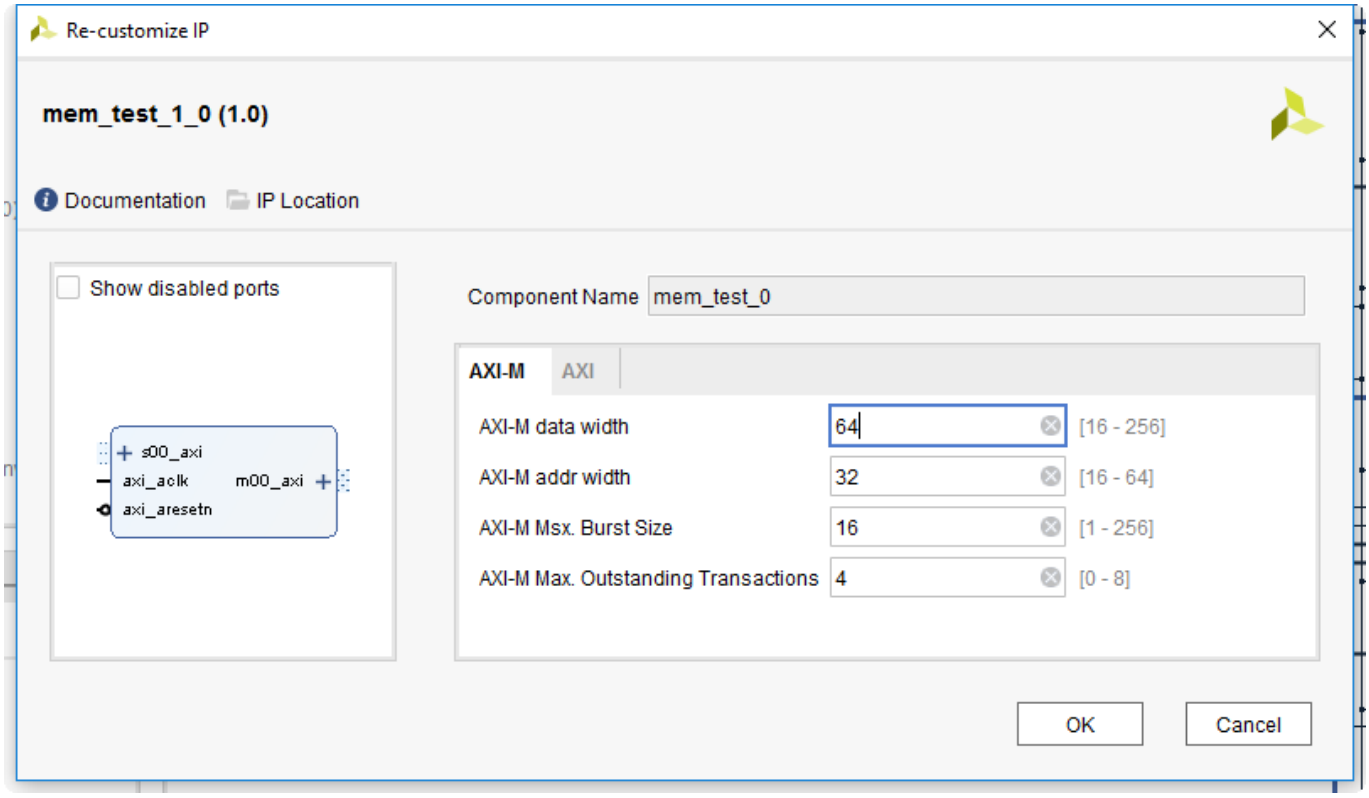
If a test is executed, the selected pattern is written to the memory range chosen. After the full range was written, it is read-back and checked. Errors are counted and the address of the first error is latched for more detailed analysis. In continuous mode, this flow is repeated until the user stops the test.

Additionally the memory tester supports only writing or only checking the pattern. This allows speeding up tests that involve software. An example for testing whether writing to one address really only affects one cell is given below:

1. Use the IP core to fill the whole memory with a pattern
2. Change exactly one address
3. Use the IP core to check the whole memory
4. Check the IP core results. There should now be exactly one error and the latched address of this error (first error) should be at the expected address.

3 Interfaces

3.1 GUI



The GUI allows setting all main parameters of the AXI master interface to access the memory. To achieve maximum performance, the maximum bust size should be chosen large and the number of outstanding transactions should be large enough that transfers are occurring back-to-back (usually 4 is sufficient).

Usually it makes sense to choose the data-width equal the width of the data-bus of the memory.

3.2 Ports

The ports are self-explaining. Note that both AXI interfaces run on the same clock.

If this does not fir the project requirements, it is recommended to add a AXI clock crossing to the *s00_axi* interface since performance is less important there. Address Map

Registers should not be accessed directly. Use the driver provided with the IP-Core whenever possible.

3.3 Registers

3.3.1 Overview

Byte Address Offset	Name	Description
0x000	START	Start command register
0x004	STOP	Stop command register
0x00C	MODE	Mode selection register
0x010	SIZE_LO	Test memory area size (lower 32-bits)
0x014	SIZE_HI	Test memory area size (upper 32-bits)
0x018	ADDR_LO	Test memory start address (lower 32-bits)
0x01C	ADDR_HI	Test memory start address (upper 32-bits)
0x020	PATTERN	Pattern selection
0x024	STATUS	Test status register
0x028	ERRORS	Error counter
0x02C	FIRSTERR_LO	First error address (lower 32-bits)
0x030	FIRSTERR_HI	First error address (upper 32-bits)
0x034	ITER	Test iteration counter

3.3.2 Register Descriptions

3.3.2.1 START – Start command register (0x000)

Field	Bit(s)	Type	Reset	Description
START	0	W	0	Write ‘1’ to start the test

The start command does reset all counters.

3.3.2.2 STOP – Stop command register (0x004)

Field	Bit(s)	Type	Reset	Description
STOP	0	W	0	Write ‘1’ to stop the test (only for continuous mode)

3.3.2.3 MODE – Mode selection register (0x00C)

Field	Bit(s)	Type	Reset	Description
MODE	2:0	RW	0	Test mode 0 Single write-and-check 1 Continuous write-and-check 2 Single write-only 3 Single check-only

3.3.2.4 SIZE_LO – Test memory area size (lower 32-bits) (0x010)

Field	Bit(s)	Type	Reset	Description
SIZE[31:0]	31:0	RW	0	Lower 32-bits of the test memory area size

3.3.2.5 SIZE_HI – Test memory area size (upper 32-bits) (0x014)

Field	Bit(s)	Type	Reset	Description
SIZE[63:32]	31:0	RW	0	Upper 32-bits of the test memory area size

3.3.2.6 ADDR_LO – Test memory area start address (lower 32-bits) (0x018)

Field	Bit(s)	Type	Reset	Description
ADDR[31:0]	31:0	RW	0	Lower 32-bits of the test memory area start address

3.3.2.7 ADDR_HI – Test memory area start address (upper 32-bits) (0x01C)

Field	Bit(s)	Type	Reset	Description
ADDR[63:32]	31:0	RW	0	Upper 32-bits of the test memory area start address

3.3.2.8 PATTERN – Pattern selection (0x020)

Field	Bit(s)	Type	Reset	Description
PATTERN	2:0	RW	0	Test pattern to use 0 Counter 1 Walking 1s 2 Own-Address 3 PRBN-16

The PRBN-16 pattern is extended to the chosen data-width by shifting the LSB through the upper bits [x:16] of the data-bus.

3.3.2.9 STATUS – Test status register (0x024)

Field	Bit(s)	Type	Reset	Description
STATUS	2:0	R	0	Test pattern to use 0 Idle 1 Writing 2 Reading 3 AXI-Error 6 Internal Error 7 Unknown

The states *AXI-Error*, *Internal Error* and *Unknown* are for debugging purposes only. They should never occur during real operation and if they occur, they cannot be left (they are all fatal). In this case, contact the developer.

3.3.2.10 ERRORS – Error counter (0x028)

Field	Bit(s)	Type	Reset	Description
ERRORS	31:0	R	0	Number of errors detected during pattern checking. This number is updated live during the test and reset whenever a test is started.

3.3.2.11 FIRSTERR_LO – First error address (lower 32-bits) (0x02C)

Field	Bit(s)	Type	Reset	Description
FIRST[31:0]	31:0	RW	0	Lower 32-bits of the address of the first error that occurred in a test (first after the test is started).

3.3.2.12 FIRSTERR_HI – First error address (upper 32-bits) (0x030)

Field	Bit(s)	Type	Reset	Description
FIRST [63:32]	31:0	RW	0	Upper 32-bits of the address of the first error that occurred in a test (first after the test is started).

3.3.2.13 ITER – Iteration counter (0x034)

Field	Bit(s)	Type	Reset	Description
ITERATIONS	31:0	R	0	Number of iterations executed in continuous mode. The counter is automatically reset if a test is started.