ASM-HEMT 101.5.0

Advanced SPICE Model for HEMTs

Technical Manual

Current Authors:
Sourabh Khandelwal and Fredo Chavez

Macquarie University

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1 Introduction

In recent years GaN based high electron mobility transistors (GaN HEMTs) have emerged as a promising candidate for high power, high voltage and high frequency applications [1]. To exploit the full potential of these devices, accurate and robust circuit simulation is required. The accuracy and convergence of simulations depend heavily on the compact model used for GaN HEMTs. Physics-based compact models are preferred because of their well-known advantages of better model scalability w.r.t. temperature, device geometry. They also give useful insights into the device operation. This manual describes a physics-based compact model[2] Advanced SPICE Model for GaN HEMTs: ASM-HEMT. Originating from [2] this model describes terminal currents, charges, trapping effects, thermal and flicker noise of GaN device accurately.

ASM-GaN model is developed for both radio-frequency (RF) and power electronics applications of these devices. This manual will describe the core and all the physical effects accounted for in the model to accurately model both flavors of the GaN-based device.

This manual describes the ASM-GaN-HEMT model in detail. A description of the model development, model equations, model parameters and parameter extraction procedure is provided in various sections of this document. In the next section, ASM-GaN-HEMT model development flow is provided. This section provides a concise description of incorporation of key device physics and challenges overcome to derive analytical formulations. Next, all the model expressions are described including the physical constants etc. used in the model calculations.

2 ASM-HEMT 101.5.0 Model Description

Advanced SPICE model for GaN HEMTs, ASM-GaN-HEMT is a physics-based model for these devices. The model can be structured into following three parts: 1. Core channel-charge or surface-potential calculations, 2. Core terminal current and charge model and 3. Models for real device effects in the device. This document covers description of all the three parts of the model.

The formation of the 2-DEG is the core of the HEMT device operation and we focused first on developing a physics-based model for the 2-DEG charge density n_s. The main challenge in modeling the 2-DEG charge density is due to the complicated variation of the Fermi-level E_f with n_s in the quantum well. Schrodinger and Poisson's equations along with the carrier statistics when applied to the AlGaN/GaN HEMT system result in the transcendental equations given in [3]. From a compact modeling point of view, analytical solutions are desirable since a solution based on numerical techniques will result in a drastic reduction of the circuit simulation speed. We have developed analytical solution for these equations by dividing the variation of E_f with the gate voltage V_g into various regions. These regions are physically meaningful and are based on the position of E_f w.r.t the energy levels E_0 and E_1. Analytical solutions are found in all the regions and the regions are combined into a single unified expression highly accurate in all the regions. The details of the model can be found in [3, 4].

The core model formulations are then used to develop a model for the drain-current I_d of GaN HEMTs. To derive the model we made use of the current continuity and performed the necessary integration of the surface-potential along the channel under the gate. We have a fully analytical solution for I_d. After this, we incorporate various real device effects appropriately into the core model. These real device effects include: velocity saturation effect, mobility field dependence, subthreshold-slope degradation, non-linear series resistances, channel-length modulation, drain-induced barrier lowering, self-heating effect and temperature dependence. Physically-linked parameters are introduced in the model to keep the model analytical and hence useful for circuit simulation. The developed model has been validated against measurement data in several publications [4–10].

For accurate simulation of transient and frequency response of the device its capacitances need to be modeled correctly. A rigorous charge model for all the terminal charges in the device is present in ASM-GaN-HEMT model. Our charge model follows from Ward-Dutton partitioning and adheres to charge conservation for good convergence properties. Additionally, ASM-GaN-HEMT model also includes models for gate-current I_g [11], thermal and flicker noise in GaN HEMTs [12, 13]. The models for terminal

charges, gate-current and noise also use the same core calculations making the model fully consistent. Furthermore, for modeling of radio-frequency devices, trapping effects are also modeled with the help of RC network sub-circuits in the model as described in the section on trapping effects model.

This completes the overview description of ASM-GaN-HEMT model. More details on each of the parts of the model can be seen in next sections of this manual.

3 ASM-HEMT 101.5.0 Model Equations

Physical and numerical constants, Voltage equations, Temperature dependent equations, surface potential, intrinsic charge and basic current equations are presented in this section. Note that the model parameters are indicated in capital letters in the equations below and in the parameter tables in the manual for better readability, but the parameters are in small letters in the code.

3.1 Physical Constants

Physical quantities in ASM-HEMT are in S.I. units unless specified otherwise.

$q = 1.6 \times 10^{-19}$

$\epsilon_{AlGaN} = 10.66 \times 10^{-11}$

$K_B = 8.636 \times 10^{-5} eV/K$

$\gamma_0 = 2.12 \times 10^{-12}$

$\gamma_1 = 3.73 \times 10^{-12}$

$DOS = 3.24 \times 10^{17}$

Smoothing constant $ep_{psi} = 0.3$

3.2 Voltages Calculation and Pre Conditioning

3.2.1 Voltages Calculation

$$V_{ds} = V_d - V_s \tag{3.2.1}$$

$$V_{gs} = V_g - V_s \tag{3.2.2}$$

$$V_{gd} = V_g - V_d \tag{3.2.3}$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01} \tag{3.2.4}$$

$$\begin{aligned} V_{off,DIBL} =& VOFF - (ETA0 - TRAPETA0 \cdot vcap + eta0_{trap}) \\ & \cdot \left(\frac{V_{dsx} \cdot VDSCALE}{\sqrt{V_{dsx}^2 + VDSCALE^2}} \right) \end{aligned} \tag{3.2.5}$$

$$V_{gs,min} = V_{off,DIBL}(T) + V_{tv} ln\left(L/(2Wq \cdot DOS \cdot V_{tv}^2)\right) \tag{3.2.6}$$

$$V_{gs,eff} = \frac{1}{2}((V_{gs} - V_{gs,min}) + \sqrt{(V_{gs} - V_{gs,min})^2 + 0.0001}) \tag{3.2.7}$$

$$V_{g0} = V_{gs,eff} - V_{off,DIBL} \tag{3.2.8}$$

$$V_{g0,eff} = \frac{1}{2}\left(V_{g0} + \sqrt{V_{g0}^2 + 4ep_{psi^2}}\right) \tag{3.2.9}$$

$$V_{dsat} = \frac{(2VSAT(T)/\mu_{eff})L \cdot V_{g0,eff}}{(2VSAT(T)/\mu_{eff})L + V_{g0,eff}} \tag{3.2.10}$$

$$V_{d,eff} = V_{ds}\left(1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{DELTA}\right)^{\frac{-1}{DELTA}} \tag{3.2.11}$$

$$V_{gd0} = V_{g0} - V_{d,eff} \tag{3.2.12}$$

$$V_{gd,eff} = \frac{1}{2}\left(V_{gd0} + \sqrt{V_{gd0}^2 + 4ep_{psi}^2}\right) \tag{3.2.13}$$

3.2.2 Bias Independent Calculations

$$C_g = \frac{\epsilon_{AlGaN}}{TBAR} \tag{3.2.14}$$

$$C_{g,fp} = \frac{\epsilon_{AlGaN}}{DFP} \tag{3.2.15}$$

$$C_{epi} = \frac{\epsilon_{AlGaN}}{TEPI} \tag{3.2.16}$$

$$C_{g,sfp} = \frac{\epsilon_{AlGaN}}{DSFP} \tag{3.2.17}$$

$$\beta = \frac{C_g}{q \cdot DOS \cdot K_B \cdot T_{dev}} \tag{3.2.18}$$

$$\alpha_n = \frac{e}{\beta} \tag{3.2.19}$$

$$\alpha_d = \frac{1}{\beta} \tag{3.2.20}$$

3.3 Temperature Dependence

$$T_{dev} = T + V(rth) \tag{3.3.1}$$

$$cdsc = 1 + NFACTOR + (CDSCD + cdscd_{trap}) \cdot V_{dsx} \tag{3.3.2}$$

$$V_{tv} = KB \cdot T_{dev} cdsc \tag{3.3.3}$$

$$\begin{aligned} V_{off,DIBL}(T) =& V_{off,DIBL} - \left(\frac{T_{dev}}{TNOM} - 1\right) \cdot KT1 \\ &+ TRAPVOFF \cdot vcap + voff_{trap} + \frac{C_{epi}}{C_{epi} + C_g} \cdot V_{sb} \end{aligned} \tag{3.3.4}$$

$$U0(T) = U0 \left(\frac{T_{dev}}{TNOM}\right)^{UTE} \tag{3.3.5}$$

$$VSAT(T) = VSAT \left(\frac{T_{dev}}{TNOM}\right)^{AT} \tag{3.3.6}$$

$$\begin{aligned} NS0ACCS(T) =& NS0ACCS \left(1 - KNS0 \left(\frac{T_{dev}}{TNOM} - 1\right)\right) \\ &\cdot (1 + K0ACCS \cdot V_{g0,eff}) + \frac{KSUB \cdot V_{bs} \cdot C_{epi}}{q} \end{aligned} \tag{3.3.7}$$

$$VSATACCS(T) = VSATACCS \left(\frac{T_{dev}}{TNOM}\right)^{ATS} \tag{3.3.8}$$

$$U0ACCS(T) = U0ACCS \left(\frac{T_{dev}}{TNOM}\right)^{UTES} \tag{3.3.9}$$

$$\begin{aligned} NS0ACCD(T) =& NS0ACCS \left(1 - KNS0 \left(\frac{T_{dev}}{TNOM} - 1\right)\right) \\ &\cdot (1 + K0ACCD \cdot V_{g0,eff}) + \frac{KSUB \cdot V_{bs} \cdot C_{epi}}{q} \end{aligned} \tag{3.3.10}$$

$$U0ACCD(T) = U0ACCD\left(\frac{T_{dev}}{TNOM}\right)^{UTES} \tag{3.3.11}$$

$$RSC(T) = RSC\left(1 + KRSC\left(\frac{T_{dev}}{TNOM} - 1\right)\right) \tag{3.3.12}$$

$$RDC(T) = RDC\left(1 + KRSC\left(\frac{T_{dev}}{TNOM} - 1\right)\right) \tag{3.3.13}$$

$$VBI(T) = VBI - \left(\frac{T_{dev}}{TNOM} - 1\right) KTVBI \tag{3.3.14}$$

$$CFG(T) = CFG - \left(\frac{T_{dev}}{TNOM} - 1\right) KTCFG \tag{3.3.15}$$

3.4 Surface Potential Calculation

Variation of surface potential with terminal gate voltage can be calculated as

$$\psi_x(V_g) = V_f(V_g) + V_x \tag{3.4.1}$$

where V_f is the potential corresponding to Fermi level in triangular potential well and V_x is the voltage at the point at which surface potential is to be calculated.

V_f Calculation

Assuming the hetero junction as triangular potential well, we can get the position of sub bands by solving the Schrodinger's equation as under[14]

$$E_n(eV) = (\frac{\hbar^2}{2m_1})\left(\frac{3}{2}\pi q\mathcal{E}\right)^{\frac{2}{3}}\left(n + \frac{2}{3}\right) \tag{3.4.2}$$

where $\mathcal{E}$ is electric field across the triangular potential well, n can take values 0,1,2..etc., m_1 is effective mass of electron in triangular well and $\hbar$ is Planck's constant. Considering only two lower subbands

$$E_0 = k_0 \mathcal{E}^{\frac{2}{3}} \tag{3.4.3}$$

$$E_1 = k_1 \mathcal{E}^{\frac{2}{3}} \tag{3.4.4}$$

By solving the Poisson's equation, we can get the relationship between electric field and sheet charge density

$$\epsilon \mathcal{E} = q n_s \tag{3.4.5}$$

Substituting (3.4.5) in (3.4.3) and (3.4.4)

$$E_0 = \gamma_0 \mathcal{E}^{\frac{2}{3}} \tag{3.4.6}$$

$$E_1 = \gamma_1 \mathcal{E}^{\frac{2}{3}} \tag{3.4.7}$$

Applying Fermi Dirac statistics,

$$n_s = DOS \int_{E_0}^{E_1} \frac{dE}{1 + e^{\frac{q(E-E_f)}{kT}}} + 2DOS \int_{E_1}^{\infty} \frac{dE}{1 + e^{\frac{q(E-E_f)}{kT}}} \tag{3.4.8}$$

where DOS is 2 dimensional density of states(DOS) in GaN. (It is DOS between E_0 and E_1 and 2DOS for above E_1)[14] By solving the integration,

$$n_s = DOS V_{tv} \left(ln[(1 + e^{(E_f - E_0)/V_{tv}})(1 + e^{(E_f - E_1)/V_{tv}})] \right) \tag{3.4.9}$$

Assuming AlGaN layer is completely ionized, from charge balance condition, we can get[15] [16]

$$n_s = \frac{\epsilon}{qd} (V_{g0} - V_f) = \frac{C_g}{q} (V_{g0} - V_f) \tag{3.4.10}$$

where $C_g = \frac{\epsilon}{d}$ (d is taken as process parameter, $TBAR$).

Solving Equations (3.4.6),(3.4.7),(3.4.9) and (3.4.10) for V_f is a difficult task as these equations are transcendental in nature.Variation of sub bands and V_f in the triangular potential well with V_g makes the calculation complicated.[17] Variation of V_f with V_g can be captured by dividing the operating region into three:

1) Sub-V_{off} region where $V_g < V_{off}$

In this region, $|E_f| >> E_0$, E_1 and $V_f \approx V_{g0}$ [18]. Applying these conditions to equation(3.4.9)

$$n_{s,sub-V_{off}} = 2DOSV_{tv}e^{\frac{V_{g0}}{V_{tv}}} \tag{3.4.11}$$

Substituting (3.4.10) in (3.4.11)

$$V_{f,sub-V_{off}} = V_{g0} - \frac{2qDV_{tv}}{C_g}e^{\frac{V_{g0}}{V_{tv}}} \tag{3.4.12}$$

2) $V_g > V_{off}$ and $E_f < E_0$

Since E_1 is more higher than E_f, neglecting $e^{\frac{(E_f-E_1)}{V_{tv}}}$ in (3.4.9) and applying $ln(1+x) \approx x$ for $x < 0$ [18]

$$n_s = DV_{th}e^{\frac{E_f-E_0}{V_{tv}}} \tag{3.4.13}$$

Using (3.4.3) and (3.4.10) in (3.4.13)

$$V_f{}^{\mathcal{I}} = V_{g0}\left(\frac{V_{th}ln(\beta V_{g0}) + \gamma_0(\frac{C_gV_{g0}}{q})^{\frac{2}{3}}}{V_{g0} + V_{tv} + \frac{2\gamma_0}{3}(\frac{C_gV_{g0}}{q})^{\frac{2}{3}}}\right) \tag{3.4.14}$$

where $\beta = C_g/(qDOS \cdot V_{tv})$.

3) $V_g > V_{off}$ and $E_f < E_0$

Since $E_1 >> E_f$, neglecting $e^{\frac{(E_f-E_1)}{V_{tv}}}$ in 3.4.9 and applying $ln(1+x) \approx lnx$ for $x > 0$

$$n_s = D(E_f - E_0) \tag{3.4.15}$$

Using (3.4.3) and (3.4.10) in (3.4.15)

$$V_f{}^{\mathcal{II}} = V_{g0}\left(\frac{\beta V_{th}V_{g0} + \gamma_0(\frac{C_gV_{g0}}{q})^{\frac{2}{3}}}{V_{g0}(1+\beta V_{tv}) + \frac{2\gamma_0}{3}(\frac{C_gV_{g0}}{q})^{\frac{2}{3}}}\right) \tag{3.4.16}$$

Combining V_f equations (3.4.14), (3.4.16) in $V_g > V_{off}$ regions [19]

$$V_{f,above} = V_{g0}(1 - H(V_{g0})) \tag{3.4.17}$$

where

$$H(V_{g0}) = \frac{V_{g0} + V_{tv}[1 - ln(\beta V_{gon})] - \frac{\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}}{V_{g0}(1 + \frac{V_{tv}}{V_{god}}) + \frac{2\gamma_0}{3}(\frac{C_g V_{g0}}{q})^{\frac{2}{3}}} \tag{3.4.18}$$

Here, V_{g0n} and V_{g0d} are functions of V_{g0} given by the interpolation expression

$$V_{g0x} = \frac{V_{g0}\alpha_x}{\sqrt{V_{g0}^2 + \alpha_x^2}} \tag{3.4.19}$$

where $\alpha_n = e/\beta$ and $\alpha_d = 1/\beta$

Combining Sub-V_{off} region V_f equation (3.4.12) with $V_g > V_{off}$ region equation (3.4.17)

$$V_{f,unified} = V_{g0} - \frac{2V_{tv}ln(1 + e^{\frac{V_{g0}}{2V_{tv}}})}{\frac{1}{H(V_{g0,eff})} + (\frac{C_g}{qD})e^{-\frac{V_{g0}}{2V_{tv}}}} \tag{3.4.20}$$

Here $V_{g0,eff}$ is equal to V_{g0} above V_{off} and is on the order of thermal voltage when $V_g < V_{off}$ and $1/V_{g0,p}$ becomes very small and equation(3.4.12) is obtained whereas in $V_g > V_{off}$, equation (3.4.17) is obtained.

But at V_off, subbands E_0 and E_1 are close to E_f. We cannot take $E_f - E_0$ and $E_f - E_1 \approx E_f$. The calculation becomes complicated. So we use Householder's numerical calculation method[20] to get the accuracy upto femto volts. The final value for E_f is obtained using the iterative re-evaluation as under

$$V_f = V_{f,unified} - \frac{p}{q}\left(1 + \frac{pr}{2q^2}\right) \tag{3.4.21}$$

Computation of p,q and r can be done as shown in the table above. From 3.4.1, ψ can be determined at source end by $\psi_s = V_f + V_s$. For potential at drain end, V_{g0} and $V_{g0,eff}$ are replaced by V_{gd0} and $V_{gd,eff}$ respectively and can be calculated by $\psi_d = V_f + V_{d,eff}$.

Table 1: Expression for Quantities in 3.4.21

Quantity	Expression
$k_{0,1}$	$\gamma_{0,1}\left(\frac{C_g}{q}\right)^{2/3}$
V_{gef}	$V_g - V_{off} - E_f$
$\xi_{0,1}$	$\exp\left(\frac{E_{f,unified} - k_{0,1}V_{gef}^{2/3}}{V_{th}}\right)$
p	$\frac{C_g}{q}V_{gef} - \sum_{i=0}^{1} DV_{th}\ln(\xi_i + 1)$
q	$-\frac{C_g}{q} - \sum_{i=0}^{1}\frac{D}{1+\xi_i^{-1}}\left(1 + (2/3)k_i V_{gef}^{-1/3}\right)$
r	$\sum_{i=0}^{1}\frac{\frac{2}{9}V_{gef}^{-4/3}Dk_i(1+\xi_i^{-1}) + \frac{D}{V_{th}}\left(1+\frac{2}{3}k_i V_{gef}^{-1/3}\right)^2}{\left(1+\xi_i^{-1}\right)^2}$

3.5 Intrinsic Charge Calculation

Accurate modelling of intrinsic charges require proper assignment of channel charge to the terminals. Q_g can be calculated as [3]

$$Q_g = -\int_0^L qWn_s(V_g, V_x)dx = -\int_0^L qWC_g(V_g 0 - \psi(x))dx \tag{3.5.1}$$

By using current continuity equation i.e., equating currents at drain end and at any point in the channel and neglecting the saturation of current we can get,[21]

$$dx = \frac{L(V_g 0 - \psi + V_{tv})}{V_g 0 - \psi_m + V_{th}}(\psi_d - \psi_s) \tag{3.5.2}$$

By substituting 3.5.2 in 3.5.1 and by integrating the equation wrt ψ, we can get

$$Q_g = \frac{C_g LW}{V_{g0} - \psi_m + V_{tv}}[V_{g0}^2 + \frac{1}{3}(\psi_d^2 + \psi_s^2 + \psi_d\psi_s) - V_{g0}(\psi_d + \psi_s - V_{tv}) - V_{tv}\psi_m] \tag{3.5.3}$$

Ward-Dutton's partitioning method [22] is used to determine the drain and source terminal charges.

$$Q_d = \int_0^L \frac{x}{L}Q_{ch}(V_g, V_x)dx \tag{3.5.4}$$

$$Q_s = \int_0^L \left(1 - \frac{x}{L}\right) Q_{ch}(V_g, V_x) dx \tag{3.5.5}$$

$$Q_g = -Q_s - Q_d \tag{3.5.6}$$

By integrating equation (3.5.2) from source to any arbitrary point in the channel, we can get x in terms of ψ

$$x = \frac{L(\psi(x) - \psi_s)}{V_{g0} - \psi_m + V_{tv}} \left(V_{g0} + V_{tv} - \frac{\psi(x) + \psi_s}{2}\right) \tag{3.5.7}$$

Substituting 3.5.7 and 3.5.2 in 3.5.4,one can get [23]

$$\begin{aligned} Q_d = -\frac{C_g LW}{120(V_{g0} - \psi_m + V_{tv})^2} [12\psi_d^3 + 8\psi_s^3 + \psi_s^2(16\psi_d - 5(V_{tv} + 8V_{g0})) \\ +2\psi_s(12\psi_d^2 - 5\psi_d(5V_{tv} + 8V_{g0}) + 10(V_{tv} + V_{g0})(V_{tv} + 4V_{g0})) \\ +15\psi_d^2(3V_{tv} + 4V_{g0}) - 60V_{g0}(V_{tv} + V_{g0})^2 \\ +20\psi_d(V_{tv} + V_{g0})(2V_{tv} + 5V_{g0})] \end{aligned} \tag{3.5.8}$$

Q_s can be obtained by using $Q_s = -Q_g - Q_d$ [24].

3.6 Drain Current Model

The drain current at any point x along the channel under the gradual channel approximation with drift diffusion model can be expressed as [25] [26],

$$I_d = -\mu W Q_{ch} \frac{d\psi}{dx} + \mu W V_{th} \frac{dQ_{ch}}{dx} \tag{3.6.1}$$

Using $Q_{ch} = C_g(V_{g0} - \psi)$, taking dx to the left side and integrating from 0 to L, we get I_dL and on right side, integrating wrt $d\psi$ from source side to the drain side potential, we get current equation as [27]

$$I_d = \frac{W}{L} \mu C_g (V_g 0 - \psi_m + V_{th}) \psi_{ds} \tag{3.6.2}$$

Where $\psi_m = (\psi_d + \psi_s)/2$, $\psi_d s = (\psi_d - \psi_s)$

3.7 Self Heating Model

The self-heating effect is modeled using an R-C network approach, which consists of thermal resistance(RTH) and thermal capacitance(CTH) [28]. The thermal node voltage gives the rise in temperature, which is added to the die temperature.

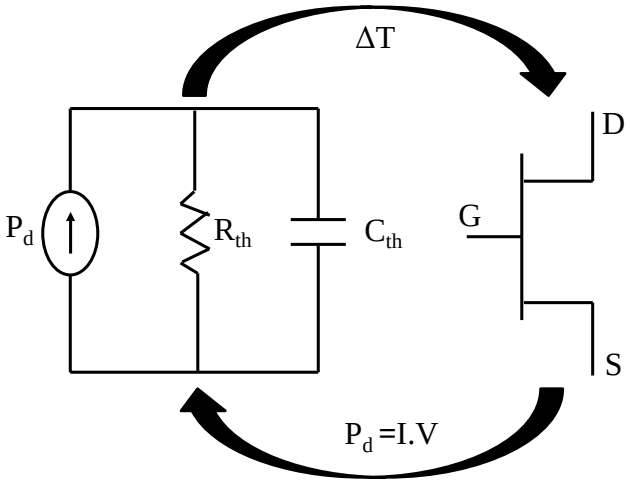

Figure 1: R-C thermal network for self-heating effect

3.8 Mobility Degradation

Mobility degradation can be modeled as [29]

$$\mu_{eff} = \frac{U0(T)}{1 + UA \cdot E_{y,eff} + UB \cdot E_{y,eff}^2 + UC \cdot E_b} \tag{3.8.1}$$

where μ_0 is the low field mobility, UA, UB and UC are model parameters to be extracted from experimental data and $E_{y,eff}$ is the effective vertical field calculated using Gauss's law as $E_{y,eff} = Q_{ch}/\epsilon_{AlGaN}$ with $Q_{ch} = \frac{C_g}{\epsilon_{AlGaN}}|V_{g0} - \psi_m|$, and E_b is the substrate electric field. E_b is calculated as,

$$E_b = \frac{|V_{bs} - \psi_s|}{TEPI} \tag{3.8.2}$$

μ_{eff} is placed in drain current equation instead of μ.

3.9 Short Channel Effects

Short channel effects play an important role in determining the near to accurate currents.

3.9.1 Velocity Saturation

Velocity saturation is modeled as [29]

$$\mu_{eff,sat} = \frac{\mu_{eff}}{\sqrt{1 + (\mu_{eff}/VSAT \cdot E_x)^2}} \tag{3.9.1}$$

where E_x is the lateral electric field and can be taken as $(\psi_d - \psi_s)/L = \psi_d s/L$ with L as the channel length of the device.

$$\mu_{eff,sat} = \frac{\mu_{eff}}{\sqrt{1 + THESAT^2 \cdot \psi_{ds}^2}} \tag{3.9.2}$$

where $THESAT$ is a model parameter with initial value $\mu_{eff}/VSAT \cdot L$.

3.9.2 DIBL

DIBL effect is included in V_{off} modeling.

$$\begin{aligned} V_{off,DIBL} =& VOFF - (ETA0 - TRAPETA0 \cdot vcap + eta0_{trap}) \\ & \cdot \left(\frac{V_{dsx} \cdot VDSCALE}{\sqrt{V_{dsx}^2 + VDSCALE^2}} \right) \end{aligned} \tag{3.9.3}$$

3.9.3 Subthreshold Slope

Subthreshold slope tells us about the leakage currents in the device. More subthreshold slope means more leakage currents. It is modeled in ASM-HEMT as follows:

$$cdsc = 1 + NFACTOR + (CDSCD + cdscd_{trap}) \cdot V_{dsx} \tag{3.9.4}$$

3.9.4 Channel Length Modulation

Channel length modulation reduces the effective length of the device thereby increasing the current in it. It is modeled in ASM-HEMT as under [30]

$$I_{ds,clm} = I_{ds}\left(1 + LAMBDA \cdot (V_{dsx} - V_{d,eff})\right) \tag{3.9.5}$$

3.10 Access Region and Parasitic Resistances

Access region resistances are important in HEMTs as the distance between gate edge and source and drain edges are large and in the order of few μm. It can be modeled as bias dependent resistance.

3.10.1 Source Region Resistance

It includes bias dependent access region resistance, source contact resistance and resistance due to traps. If $RDSMOD = 1$

$$\begin{aligned} R_{source} =& \frac{RSC(T)}{W \cdot NF} + TRAPRS \cdot vcap \\ &+ \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS(T) \cdot U0ACCS(T)} \\ &\cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCS}\right)^{\frac{-1}{MEXPACCS}} \end{aligned} \tag{3.10.1}$$

where

$I_{sat,source} = W \cdot NF \cdot NS0ACCS(T) \cdot VSATACCS(T)$

If $RDSMOD$ is zero, then $R_{source} = 10^{-6}$

3.10.2 Drain Region Resistance

It includes bias dependent access region resistance, source contact resistance and resistance due to traps. If $RDSMOD = 1$

$$R_{drain} = \frac{RDC(T)}{W \cdot NF} + TRAPRD \cdot vcap + R_{trap}(T) + ron_{trap} + \frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD(T) \cdot U0ACCD(T)} \cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,drain}}\right)^{MEXPACCD}\right)^{\frac{-1}{MEXPACCD}} \tag{3.10.2}$$

where $I_{sat,drain} = W \cdot NF \cdot NS0ACCD(T) \cdot VSATACCS(T)$

If $RDSMOD$ is zero, then $R_{drain} = 10^{-6}$

If parameter AR is given in the model card the increase in access region resistance is modeled with the following formulation.

$$kv = \sqrt{1 + AT} \cdot I_{ds} \tag{3.10.3}$$

$$kvv = \frac{kv}{I_{sat,accs}} \tag{3.10.4}$$

$$t_0 = 1 + AR + kvv^2 \tag{3.10.5}$$

$$t_1 = \sqrt{t_0 - 2 \cdot kvv} + \sqrt{t_0 + 2 \cdot kvv} \tag{3.10.6}$$

$$id_{eff} = \frac{2 \cdot kv}{t_1} \tag{3.10.7}$$

$$R_{source} = \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS \cdot U0ACCS} \cdot \frac{1}{1 - (I_{d,eff}/I_{sat,accs})} \tag{3.10.8}$$

3.10.3 Gate Region Conductance

It is modeled as under

$$R_{gate} = RSHG\left(\frac{XGW + W/(3 \cdot NGCON)}{NGCON \cdot NF \cdot L}\right) \tag{3.10.9}$$

If $R_{gate} > 0$

$G_{gate} = 1/R_{gate}$

else

$G_{gate} = 10^3$

3.11 Parasitic Capacitances

3.11.1 Access Region Capacitances

The access region capacitance particularly at the drain end of the device, which shows up in drain-source capacitance(C_{ds}), takes the form of a bias dependent depletion capacitance and is formulated as under

$$C_{accd} = \frac{CJ0}{(1 + \frac{V_{ds}}{VBI})^{MZ}} \tag{3.11.1}$$

3.11.2 Overlap Capacitances

CGSO, CDSO, CGDO and CGDL are presented as model parameters to include overlap capacitance effects.

3.11.3 Fringing Capacitances

Model parameters, CFD and CFG are included to get the effects of fringing capacitances.

3.12 Trap Model

The presence of traps at the surface, in the barrier and the buffer layer are well-known in GaN HEMTs. These traps affect device characteristics significantly and give rise to the effects known as drain-lag, gate-lag, knee walk-out, dynamic on-resistance etc. The trapping effects are modeled in ASM-HEMT model with the help of a sub-circuit. We have three different trapping effects models which users can select: TRAPMOD=1, 2 and 3 as described below. When TRAPMOD is set to 0, trapping effects are not modeled.

The topology for TRAPMOD=1 is shown in figure below.

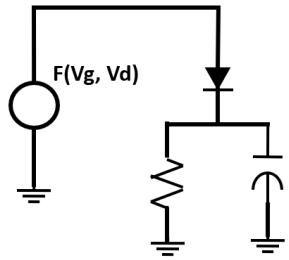

Figure 2: Modeling trapping effects in GaN HEMTs with the voltage Vtrap in this sub-circuit for TRAPMOD=1

The trap-voltage V_{trap} generated is fed back into the model and it updated parameters like the cut-off voltage, DIBL, source and drain-resistances to capture the effects of traps.

The topology for TRAPMOD=2 is shown below. In this case two different RC sub-circuits are used.

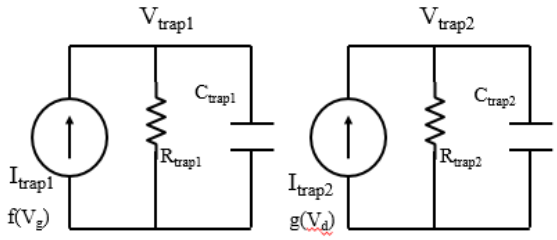

Figure 3: Modeling trapping effects in GaN HEMTs with the voltage Vtrap1 and Vtrap2 in this sub-circuit

The trap voltages V_{trap1} and V_{trap2} update the parameters cut-off voltage, sub-threshold slope, source and drain-resistances to capture the effects of traps. In this case, since the trap generation current is both a function of V_d and V_g this model is more flexible.

The topology for trap-model TRAPMOD=3 is shown below.

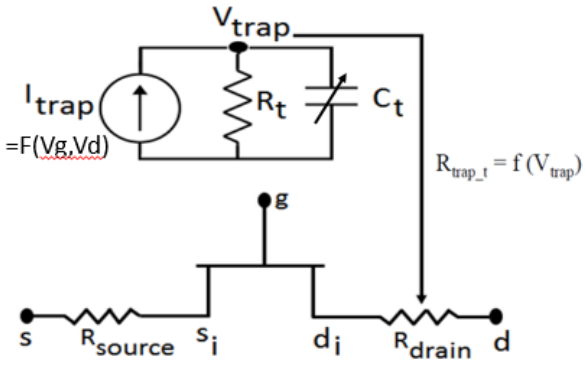

Figure 4: Modeling trapping effects in GaN HEMTs with the RC sub-circuit

This is recommended for modeling the GaN power device dynamic ON-resistance. Only the drain-side resistance is affected in this trap model.

A new dynamic trap model is introduced in this version of the model. This is created with Shockley-Read-Hall recombination generation physics. The circuit representation of the dynamic trap model is shown in Fig. 5.

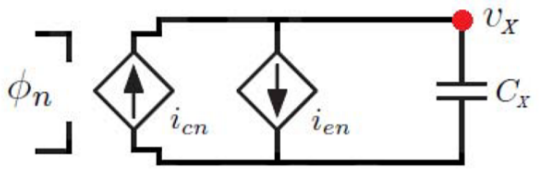

Figure 5: Circuit representation of dynamic trap model selected by TRAPMOD=5.

A trapped charge is represented by the charge on the capacitor CX. The voltage V_x is the trapping potential. A capture of charge is modeled with the current source I_{cn} and the release of charge from the trap is modeled with the current source I_{en}. The external biases (Vds and Vgs) affect the the forcing potential ϕ_n which in-turn controls the current I_{cn}.

$$\phi_n = ln(exp(\alpha \cdot V_{gs} + \alpha_d \cdot V_{gd} + \beta \cdot V_{ds} + \gamma) + \eta) \tag{3.12.1}$$

The trap emission rate has a strong temperature dependence with activation energy EA. The product $CX.EN$ models the trap emission frequency.

$$EN = ENO \cdot exp(\frac{EA}{k \cdot T_{dev}} - \frac{EA}{k \cdot T_{nom}}) \tag{3.12.2}$$

The capture current is modelled with,

$$I_{cn} = CX \cdot EN \cdot (VXMAX - V_x) \cdot (exp(2 \cdot \phi_n) - 1) \cdot \frac{1}{2} \tag{3.12.3}$$

where VXMAX is the maximum trap potential and is a model parameter. The emission current is modelled with,

$$I_{en} = CX \cdot EN \cdot V_x \tag{3.12.4}$$

The generated trap potential then affects the effective cut-off voltage (V_{off}), source side access charge density ($n_{s,acc}$), and the drain size access charge density ($n_{d,acc}$). The degradation in V_{off} with V_x is modeled with DLVOFF. The degradation in $n_{s,acc}$ with V_x is modeled with DLNS0S. The degradation in $n_{d,acc}$ with V_x is modeled with DLNS0D.

The behavior of change in V_{off}, $n_{s,acc}$, and $n_{d,acc}$ with the trap potential V_x is modeled with the function given below.

$$T0 = VINP \cdot VMAX \tag{3.12.5}$$

$$T1 = \sqrt{VINP \cdot VINP + VMAX \cdot VMAX} \tag{3.12.6}$$

$$pout = PTUNE \cdot PIN \cdot \frac{T0}{T1} \tag{3.12.7}$$

where VINP maps to the trap potential V_x, VMAX maps to the parameter VDLMAX which controls the saturation of parameter change with trapping, PIN maps to parameter value without traps, PTUNE maps to parameters DLVOFF, DLNS0S, and DLNS0D, and *pout* is the final parameter value after accounting for trapping.

Two trapping network with the above structure and formulations are implemented in TRAPMOD=5. Each of the network has its own set of model parameters.

3.13 Gate Current Model

The modeling of gate current in ASM-HEMT is implemented by using two diodes; one is for gate-to-source current and another is for gate-to-drain current. The current expressions used in GATEMOD=1 are given below.

$$I_{gs} = W \cdot L \cdot NF \cdot \left[IGSDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[exp\left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.13.1}$$

$$I_{gd} = W \cdot L \cdot NF \cdot \left[IGDDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGD \right] \left[exp\left\{ \frac{V_{gd}}{NJGD \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.13.2}$$

where $IGSDIO$ and $IGDDIO$ represent saturation currents of gate-source and gate-drain junction diodes, respectively. $NJGS$ and $NJGD$ are the diode current ideality factors and parameters $KTGS$ and $KTGD$ are used to capture the temperature dependence of gate saturation current.

GATEMOD=1 is simple diode-like reverse current model. GaN HEMTs can have larges reverse leakage due to Poole-Frenkel effect. Following formulations are implemented in the model for Poole-Frenkel reverse current. These get invoked when GATEMOD=2.

$$I_{gs,dio} = W \cdot L \cdot NF \cdot \left[IGSDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[exp\left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.13.3}$$

$I_{gs,dio}$ is the same as GATEMOD=1. Following additional formulations are added for Poole-Frenkel leakage.

$$E_{field} = Vgs/TBAR \tag{3.13.4}$$

$$RIGSDIO_T = RIGSDIO + exp(T/TNOM - 1) * RKTGS \tag{3.13.5}$$

$$I_{gs} = I_{gs,dio} \cdot \left(1 + RIGSDIO_T * E_{field} \cdot exp(\frac{\sqrt{Vgs} + EBREAKS}{RNJGS * K_B * T}) \right) \tag{3.13.6}$$

For p-GaN devices GATEMOD=3 is introduced in ASM-HEMT. The gate-source current formulation for GATEMOD=3 is given below. Parameter AGS is introduced to model the varying ideality factor in these devices.

$$I_{gs,dio} = W \cdot NF \cdot IGSDIO \cdot \left[exp\left\{ \frac{(V_{gs})^{AGS}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \cdot \left[exp\left\{ \frac{(V_{bi,s})}{NJGS \cdot K_B \cdot T_{dev}} \right\} \right] \tag{3.13.7}$$

For the reverse leakage, formulation same as Eq. 3.13.6 is used in GATEMOD=3 too. Due to the coupled nature of forward- and reverse current formulations, the model extraction process needs to carefully consider both conditions simultaneously. The parameters cannot be independently fitted due to the coupled formulations.

The ambient temperature is modelled with temperature dependence on parameters IGSDIO, VBIS and NJGS as described below.

$$NJGS(T) = NJGS + KTNJGS \cdot (\frac{T_{dev}}{T_{nom}} - 1) \tag{3.13.8}$$

$$VBIS(T) = VBIS + KTVBIS \cdot (\frac{T_{dev}}{T_{nom}} - 1) \tag{3.13.9}$$

$$IGSDIO(T) = IGSDIO \cdot exp(KTGS(\frac{T_{dev}}{T_{nom}} - 1)) \tag{3.13.10}$$

The above equations are for gate-source part of the gate-current. Similar equations exist in the model for the gate-drain part of the total gate-current.

3.14 Field Plate Model

3.14.1 Sub-circuit representation

Field plate incorporation in a device modulates the 2DEG charge formed at the AlGaN/GaN heterojunction. We therefore assign transistor properties to the regions of the device directly under the field plate, in addition to the intrinsic device. The equivalent sub-circuit representation of the device with a standard field plate topology of a gate-connected and source-connected field-plate is shown as under[7]:

For each of the transistors T_1, T_2 and T_3, the surface potential calculation is done as performed in section Surface Potential Calculation above. This is followed by calculation of intrinsic charges as explained in sub-section Intrinsic Charge Calculation and assigned accordingly to intrinsic nodes within the device.

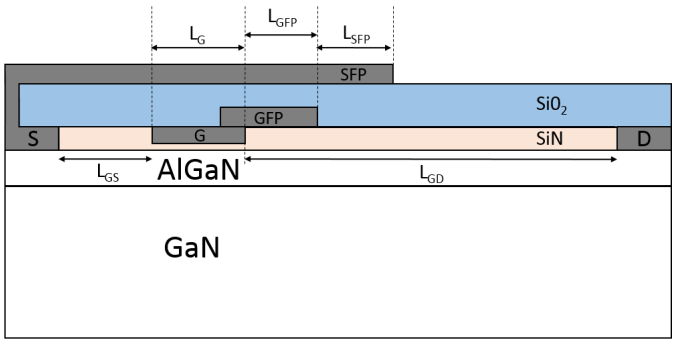

Figure 6: Cross-sectional view of the dual FP device showing the gate and source FPs and their appropriate connections to gate and source respectively.

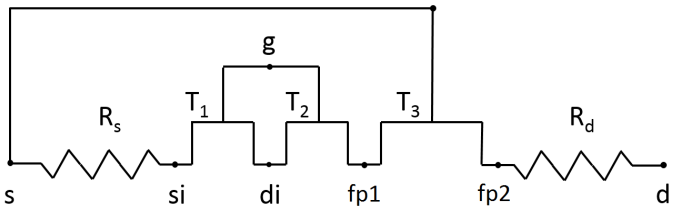

Figure 7: Model representation of the device. T_1, T_2 and T_3 denote Intrinsic, Gate FP and Source FP transistors respectively. The intrinsic nodes within the device are also indicated.

3.14.2 MOD selectors for field plate

We present a field-plate model with multiple field plates options (maximum 4 field-plates), in which we provide flexibility to the user where each field-plate could be set to either no field-plate, or gate-connected or source-connected field-plate as per the device structure. Following flags in the model are used to set the field-plate configuration to either "No field-plate" ($FPXMOD = 0$), "Gate-connected field-plate" ($FPXMOD = 1$) or "Source-connected field-plate" ($FPXMOD = 2$), where X represents the field-plate index. Based on the field-plate configuration, intrinsic drain-source (V_{ds_fpx}) and gate-source (V_{gs_fpx}) voltages for the x^{th} field-plate is assigned.

If $FP1MOD = 1$, then

Gate field plate module is selected. For the Gate Field Plate Transistor, the surface potential calculation is done as performed for the intrinsic transistor which is defined

in a functional form. The new set of calculations is done with appropriate voltages, variables and parameters e.g (voltage V_{ds} is replaced by $V_{ds_{fp1}}$, parameters L and $VOFF$ are replaced by $LFP1$ and $VOFFFP1$ respectively, variable C_g is replaced by $C_{g_{fp1}}$ etc).

If $FP1MOD = 2$, then

Source field plate module is selected. Similar to what was done for $FPMOD = 1$, however, the only difference being in gate-source voltage ($V_{gs_{fp1}}$), which in this case becomes the voltage between the extrinsic source node and the intrinsic source terminal of the field-plate transistor.

As a final outcome, we obtain drain current, intrinsic charges of the field-plate transistors which are assigned as per the field-plate configuration.

Similar procedure is followed for other field-plate modules ($FP2MOD, FP3MOD$ and $FP4MOD$).

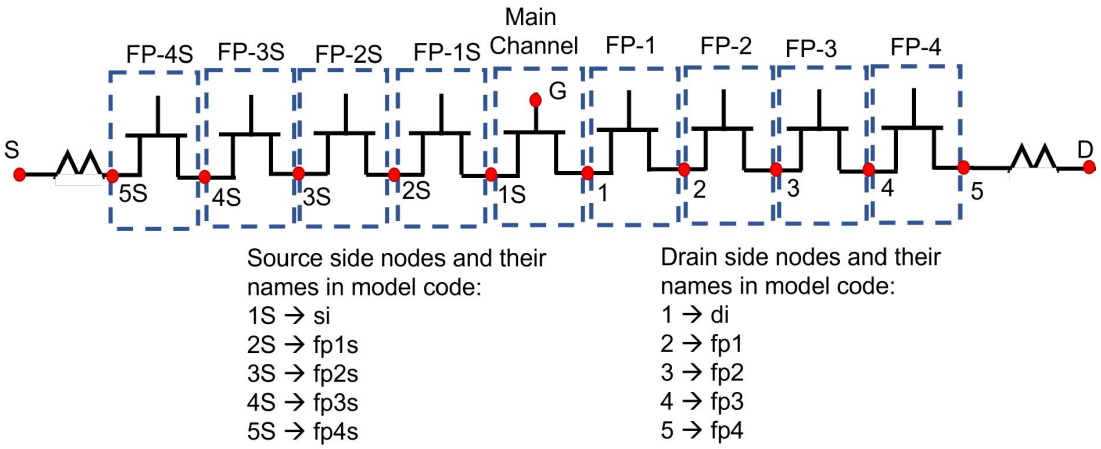

Figure 8: Model representation of the device. All eight field-plates are shown in the figure. These can be configured with the field-plate model selector switches. The nodes due to the full implementation of field-plate model are also shown.

A computationally efficient method to account for field-plates is introduced in the ASM-HEMT model. This formulation is selected by setting FASTFPMOD=1. If FASTFPMOD=1 is set all the field-plates are calculated with the fast field plate formulations. When FASTFPMOD is set to 1, the parameters which can be used to tune

the field-plate capacitances are: VOFFFPx, DFPx, LFPx, KTFPx, GAMMA0FPx, GAMMA1FPx, and NFACTORFPx. Other field-plate parameters will not play a role when FASTFPMOD=1 is enabled.

3.14.3 Cross Coupling Capacitances

In case of the dual field-plate topology ($FP1MOD = 1$ and $FP2MOD = 2$) i.e one with a gate-connected and a source-connected field plate, the gate-connected field plate transistor modulates the 2DEG lying beneath the source-connected field plate ($2DEG_{FP2}$) through fringing field whereas the source-connected field plate transistor modulates the 2DEG lying beneath the gate-connected field plate ($2DEG_{FP1}$) , leading to cross-coupling capacitance components in C_{gd} and C_{sd} respectively in the form of additional plateaus. The two associated cross-coupling charges are evaluated in terms of the existing gate charge formulation as given below.

$$Q_{cc,cgd} = -CFP2SCALE \times WL_{FP2}C_{g,FP2}\Bigg\{V_{go,FP2} - \frac{1}{2}\left(\psi_{s,FP2} + \psi_{d,FP2}\right) + \frac{\left(\psi_{d,FP2} - \psi_{s,FP2}\right)^2}{12\Big(V_{go,FP2} - \frac{K_BT}{q} - \frac{1}{2}\left(\psi_{s,FP2} + \psi_{d,FP2}\right)\Big)^2}\Bigg\} \tag{3.14.1}$$

$$Q_{cc,csd} = -CFP1SCALE \times WL_{FP1}C_{g,FP1}\Bigg\{V_{go,FP1} - \frac{1}{2}\left(\psi_{s,FP1} + \psi_{d,FP1}\right) + \frac{\left(\psi_{d,FP1} - \psi_{s,FP1}\right)^2}{12\Big(V_{go,FP1} - \frac{K_BT}{q} - \frac{1}{2}\left(\psi_{s,FP1} + \psi_{d,FP1}\right)\Big)^2}\Bigg\} \tag{3.14.2}$$

$Q_{cc,cgd}$ and $Q_{cc,csd}$ represents the cross-coupling charge between the $FP1-2DEG_{FP2}$ and $FP2-2DEG_{FP1}$ respectively. $CFP2SCALE$ and $CFP1SCALE$ denote dimensionless scaling factors that determine the strength of cross-coupling plateaus observed in C_{gd} and C_{sd} respectively. These charges are assigned between the gate of one field-plate transistor and the source node of the other field-plate transistor.

3.14.4 Substrate Capacitance

The introduction of a substrate electrode introduces a capacitance between the substrate and the other three intrinsic device nodes namely the gate, drain and source where the GaN buffer acts as a dielectric. The substrate-drain capacitance (C_{subd}), however, needs more attention since it forms a part of the overall output terminal capacitance (C_{oss}). We associate some charges to the substrate node and divide it into the regional substrate charges corresponding to the intrinsic transistor (Q_{subi}), FP1 transistor (Q_{sub1}) and FP2 transistor (Q_{sub2}). Each one of these quantities is basically a scaled value of the 2DEG for each transistor controlled by its own gate. So, effectively we model the substrate as a back-field-plate, with the GaN layer as the dielectric, which to some extent modulates the channel 2DEG. The regional substrate charges are evaluated using the existing gate charge formulation given as

$$Q_{sub,K} = -CSUBSCALE,K \times WL_K C_{g,K} \Bigg\{ V_{go,K} - \frac{1}{2}\left(\psi_{s,K} + \psi_{d,K}\right) + \frac{\left(\psi_{d,K} - \psi_{s,K}\right)^2}{12\Big(V_{go,K} - \frac{K_B T}{q} - \frac{1}{2}\left(\psi_{s,K} + \psi_{d,K}\right)\Big)^2} \Bigg\} \tag{3.14.3}$$

where K is i, 1 and 2 for intrinsic transistor, FP1 transistor and FP2 transistor respectively. CSUBSCALE,K is a dimensionless scaling factor that controls the magnitude of the regional substrate charges.

These charges are assigned between the substrate node and the source of the corresponding transistor to calculate the substrate capacitance.

3.14.5 Quantum Mechanical Effects

Due to the quantum nature of the 2DEG charge at the hetero-interface, the centroid shift of the probability distribution functions needs to be accounted for in the model. The resulting increase in the barrier thickness, reduces the gate capacitance [31] per unit area which subsequently is used in all the intrinsic charge equations.

$$C_g = \frac{\epsilon_{AlGaN}}{TBAR + ADOS/(1 + CDOS \cdot (Q_g/QM0))^{BDOS}} \tag{3.14.4}$$

3.15 Noise Model

Thermal and Flicker noise models are included in ASM-HEMT model.

3.15.1 Flicker Noise Model

Our unified flicker noise model takes both the theories of mobility fluctuation and carrier number fluctuation into account. The power spectral density (PSD) of the mean square fluctuations in number of occupied traps is given as [32],[33]

$$S_N(f) = N_t \frac{k_B T_{dev}}{N_{P_t} f^{EF}} \tag{3.15.1}$$

where N_t is the concentration of traps (in cm^{-2}) and f is the frequency of operation. The N_{P_t} factor comes from tunneling probability and EF is a modeling parameter.This in turn gives the drain current noise PSD as

$$S_{if}(f) = \frac{S_N(f)}{WL^2} \int_0^L \left(\frac{\partial I_{DS}}{\partial N_t} \right)^2 dx \tag{3.15.2}$$

Also,

$$I_{DS} = \mu W(-Q_{ch}(x)) \frac{\partial \psi}{\partial x} \tag{3.15.3}$$

$$\partial I_{DS} = \mu W(-Q_{ch}) \frac{\partial \psi}{\partial x} \left[\frac{1}{-Q} \frac{\partial(-Q)}{\partial N_t} \pm \frac{1}{\mu} \frac{\partial \mu}{N_t} \right] \partial N_t \tag{3.15.4}$$

$$\partial I_{DS} = I_{DS} \left[\frac{qR}{-Q_{ch}} \pm \frac{1}{\mu} \frac{\partial \mu}{\partial N_t} \right] \partial N_t \tag{3.15.5}$$

where $R = \frac{1}{q} \frac{\partial(-Q_{ch})}{\partial N_t}$. The + or - sign depends on whether a trap is neutral or charged when filled, which will increase or decrease mobility. Using (3.15.2) and (3.15.5), we get

the drain current noise PSD as [12]

$$S_{if}(f) = \frac{k_B T}{W L^2 f^{EF}} \frac{I_{DS}^2 K_r}{C_g^2} \Big[NOIA V_{th} C_g \left(\frac{1}{Q_{ch,d}} - \frac{1}{Q_{ch,s}} \right) + (NOIA + NOIB V_{th} C_g) ln \left(\frac{Q_{ch,d}}{Q_{ch,s}} \right) \tag{3.15.6}$$

$$+ (NOIB + NOIC V_{th} C_g)(-Q_{ch,d} + Q_{ch,s}) + \frac{NOIC}{2}(Q_{ch,d}^2 - Q_{ch,s}^2) \Big] \tag{3.15.7}$$

where $K_r = L/\left[(V_{go} - \psi_m + V_{th})(\psi_d - \psi_s)\right]$, $Q_{ch,(d/s)} = qC_g\left(V_{go} - \psi_{(d/s)}\right)$ and $NOIA$, $NIOIB$ and $NOIC$ are parameters that include terms like N_{P_t} and N_t.

3.15.2 Thermal Noise Model

The noise PSD can be given as[34]

$$S_{it} = \frac{4k_B T_{dev}}{I_D L_{eff}^2} \int_{\psi_s}^{\psi_d} g^2(\psi) d\psi \tag{3.15.8}$$

where $g(\psi) = \mu_{eff,sat} W(qn_s)$.
The final noise PSD can therefore be written as [13]

$$S_{it} = \frac{4k_B T_{dev}}{I_D L_{eff}^2} (\mu_{eff,sat} W q C_g)^2 \left(V_{go}^2 \psi_{ds} + \frac{\psi_d^3 - \psi_s^3}{3} - V_{go}\left(\psi_d^2 - \psi_s^2\right) \right) \tag{3.15.9}$$

3.15.3 Drain-source breakdown model

The drain-source breakdown current $I_{ds,bv}$ is calculated using the following formulations.

$$I_{ds,bv} = ASL \cdot W \cdot NF \cdot (e^{\frac{(Vds - BVDSL)}{NSL \cdot V_{th}}} - e^{\frac{(-BVDSL)}{NSL \cdot V_{th}}}) \tag{3.15.10}$$

The breakdown model have temperature dependence given by,

$$NSLT = NSL \cdot \left(1 + KASL \cdot (\frac{T}{Tnom} - 1)\right) \tag{3.15.11}$$

$$BVDSLT = BVDSL \cdot \left(1 + KBVDSL \cdot (\frac{T}{Tnom} - 1)\right) \tag{3.15.12}$$

$$ASLT = ASL \cdot \left(1 + KASL \cdot (\frac{T}{Tnom} - 1)\right) \tag{3.15.13}$$

3.15.4 Gate Resistance Model

ASM-HEMT model has two different gate resistance models. User can choose by setting the model ag RGATEMOD. RGATEMOD=1 is a simple gate resistance model. RGATEMOD=2 is advanced gate resistance model which takes into account the difference in low- and high-frequency gate resistance behavior. The model schematic for the two gate resistance models are shown below.

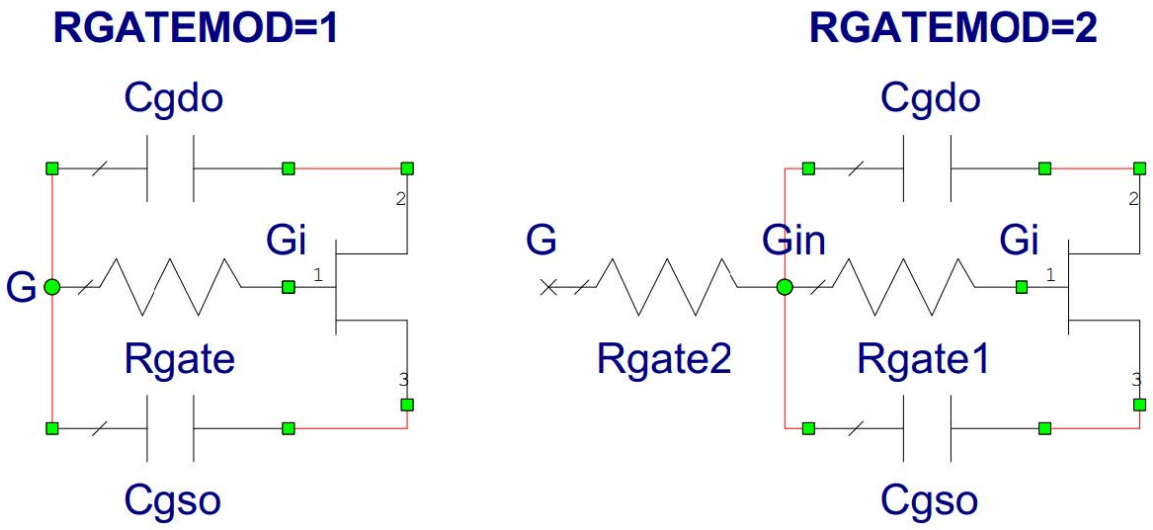

Figure 9: Gate resistance models in ASM-HEMT.

3.16 Substrate Leakage Model

Drain to substrate and Source to substrate leakage current can occur in devices under high drain-substrate and source-substrate conditions. This is modelled with following formulations.

$$T3 = max(V_{db} - VBIDB, 0) \tag{3.16.1}$$

$$I_{db} = W \cdot NF \cdot IDBL \cdot \left[exp\left\{ \frac{T3}{NBD \cdot K_B \cdot T_{dev}} \right\} - 1 \right] \tag{3.16.2}$$

A graph showing drain and the substrate current is shown below.

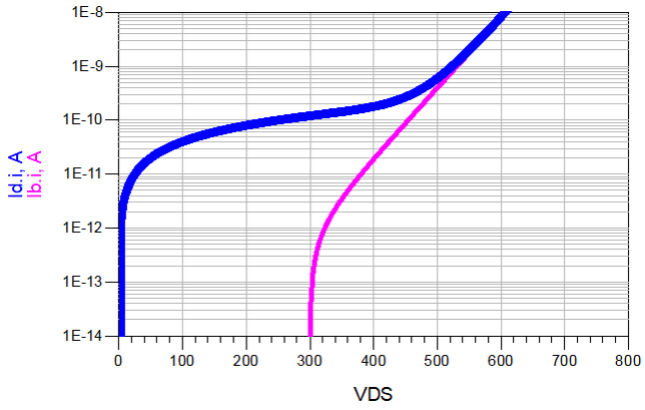

Figure 10: Substrate leakage current simulations showing drain and substrate current.

The above equations describe the drain-to-substrate leakage. Equivalent equations for source-to-substrate leakage is implemented in the model.

4 Parameter List

4.1 Process Parameters

Note that the parameters listed here are in capital letters for better readability but they are in small letters in the code.

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
TNOM	°C	27	-	-	Nominal Temperature
TBAR	m	2.5e-8	0.1e-9	∞	Thickness of the AlGaN Layer
TEPI	m	1.64e-6	0.1e-9	∞	Thickness of the GaN epi Layer
MULT_I		1.0	0.0	∞	MULT factor for current.
MULT_Q		1.0	0.0	∞	MULT factor for charge.
MULT_FN		MULT_I	0.0	∞	MULT factor for flicker noise.
L	m	0.25e-6	20e-9	∞	Designed Gate Length
W	m	200e-6	20e-9	∞	Designed Gate Width
NF	-	1	1	∞	Number of fingers(Integer)
LSG	m	1e-6	0	∞	Length of Source-Gate Access Region
LDG	m	1e-6	0	∞	Length of Drain-Gate Access Region
EPSILON	F/m	10.66e-11	0	∞	Dielectric permittivity of AlGaN layer
GAMMA0I	-	2.12e-12	0	1	Schrodinger-Poisson solution variable
GAMMA1I	-	3.73e-12	0	1	Schrodinger-Poisson solution variable

4.2 Model Controllers

Name	Unit	Default	Min	Max	Description
RDSMOD	-	1	0	1	Selects Access region Resistance Model; 0-simplified, 1-more accurate
GATEMOD	-	0	0	3	Model to turn OFF/ON the gate current model;0 to turn off,1 to turn on simple model, 2 to turn on gate current model with Poole-Frenkel reverse current, 3 gate current for p-GaN
SHMOD	-	1	0	1	Self Heating Model Controller; 0-Turns OFF Self Heating Model 1-Turns ON Self Heating Model
TRAPMOD	-	0	0	5	Selects Trap Model;0-Turns off the model; 1-turns on RF trap model; 2-turns on pulsed IV trap model; 3-turns on basic trap model;4: Model with separate gate and drain-lag; 5: Dynamic trap model
FNMOD	-	0	0	1	Selects Flicker noise Model; 0-Turns off the model 1 to turn on
TNMOD	-	0	0	1	Selects Thermal noise Model; 0-Turns off the model 1 to turn on
FP1MOD	-	0	0	2	Drain-side Field Plate 1 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP2MOD	-	0	0	2	Drain-side Field Plate 2 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP3MOD	-	0	0	2	Drain-side Field Plate 3 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP4MOD	-	0	0	2	Drain-side Field Plate 4 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate

FP1SMOD	-	0	0	2	Source-side Field Plate 1 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP2SMOD	-	0	0	2	Source-side Field Plate 2 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP3SMOD	-	0	0	2	Source-side Field Plate 3 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
FP4SMOD	-	0	0	2	Source-side Field Plate 4 Model Selector; 0- No Field Plate; 1- Gate Field Plate; 2- Source Field Plate
RGATEMOD	-	1	0	1	Switch to turn on/off gate Resistance; 0-Turns off the resistance 1 to turn on
FASTFPMOD	-	0	0	1	Fast field plate model selector, 0: OFF and 1: ON.

4.3 Basic Model Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
VOFF	V	-2.0	-100	5	Cut-off Voltage
U0	$m^2/V-s$	170e-3	-	-	Low field mobility
UA	V^{-1}	0e-9	0	∞	Mobility Degradation Coefficient
UB	V^{-2}	0e-18	0	∞	Second Order Mobility Degradation Coefficient
UC	V^{-1}	0e-9	0	∞	Mobility Degradation Coefficient with V_{bs}
VSAT	m/s	1.9e5	1e3	∞	Saturation Velocity
DELTA	-	2	2	∞	Exponent of Vdeff
LAMBDA	V^{-1}	0	0	∞	Channel Length Modulation Coefficient
ETA0	-	0e-3	0	∞	DIBL Parameter
VDSCALE	V	5	0	∞	DIBL Scaling VDS
THESAT	V^{-2}	1	1	∞	Velocity Saturation Parameter

NFACTOR	-	0.5	0	∞	Sub-VOFF Slope parameters
CDSCD	-	1e-3	0	∞	Sub-VOFF Slope Change due to Drain Voltage
IMIN	A	1e-15	-	-	Minimum Drain Current
GDSMIN	S	1e-12	0	∞	Shunt conductance across channel and all field plates
TGDSMIN	S	0	0	∞	Temperature dependence for minimum leakage conductance parameter GDSMIN

4.3.1 Access Region Resistance Model Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
VSATACCS	cm/s	50e3	0	∞	Saturation Velocity for access region
NS0ACCS	C/m^{-2}	5e17	1e5	∞	2-DEG Charge Density per square meter in Source Access Region
NS0ACCD	C/m^{-2}	5e17	1e5	∞	2-DEG Charge Density per square meter in Drain Access Region
K0ACCS	-	0	-	-	Dependence of access region charge at source side on gate voltage
K0ACCD	-	0	-	-	Dependence of access region charge at drain side on gate voltage
KSUB	-	0	-	-	Dependence of access region charge on substrate voltage
U0ACCS	$m^2/V-s$	155e-3	0	∞	Source Side Access Region Mobility
U0ACCD	$m^2/V-s$	155e-3	0	∞	Drain Side Access Region Mobility
MEXPACCS	-	2	0	∞	Exponent for Source side Access Region Resistance Model
MEXPACCD	-	2	0	∞	Exponent for Drain side Access Region Resistance Model
RSC	$Ohm-m$	1e-4	0	∞	Source Contact Resistance
RDC	$Ohm-m$	1e-4	0	∞	Drain Contact Resistance

4.3.2 Gate Current Model Parameters

Name	Unit	Default	Min	Max	Description
IGSDIO	A/m^{-2}	1.0	-	-	Gate-source junction diode saturation current
NJGS	-	2.5	-	-	Gate-source junction diode current ideality factor
IGDDIO	A/m^{-2}	-	-	-	Gate-drain junction diode saturation current
NJGD	-	2.5	-	-	Gate-drain junction diode current ideality factor
KTGS	-	0.0	-	-	Temperature co-efficient of gate-source junction diode current
KTGD	-	0.0	-	-	Temperature coefficient of gate-drain junction diode current
RIGSDIO	A/m^{-2}	1.0	-	-	Gate-source junction reverse diode current multiplier, active when GATEMOD=2
RNJGS	-	80	-	-	Gate-source junction diode current slope factor for reverse bias, active when GATEMOD=2
RIGDDIO	A/m^{-2}	-	-	-	Gate-drain junction reverse diode current multiplier, active when GATEMOD=2
RNJGD	-	80	-	-	Gate-drain junction diode current slope factor for reverse bias, active when GATEMOD=2
RKTGS	-	0.0	-	-	Temperature co-efficient of gate-source reverse junction current, active when GATEMOD=2
RKTGD	-	0.0	-	-	Temperature co-efficient of gate-drain reverse junction current, active when GATEMOD=2

EBREAKS	-	0.0	-	-	Parameter to model large reverse bias reverse current, active when GATEMOD=2
EBREAKD	-	0.0	-	-	Parameter to model large reverse bias reverse current, active when GATEMOD=2
AGS	-	1.0	0	50	GATEMOD=3 parameter for tuning ideality factor variation with bias in G-S
AGD	-	1.0	0	50	GATEMOD=3 parameter for tuning ideality factor variation with bias in G-D

4.3.3 Trap Model Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
RTRAP3	Ohm	1.0	0	∞	Trap Network Resistance
CTRAP3	F	1.0e-4	0	∞	Trap Network Capacitance
VATRAP	-	10	0	∞	Division Factor for V(trap1)
VDLR1	-	2	-	-	Slope for Region1
VDLR2	-	20	-	-	Slope for Region2
WD	-	0.016	-	-	Weak dependence of VDLR1 on V_{dg}
VTB	-	250	0	∞	Break Point for V_{dg} Effect on V_{on}
SCT	-	1	0	∞	Slope parameter for CT variation with V_{gs}
DELTAX	m	50	0	∞	Smoothing Constant
CDLAG	-	5e-9	0	∞	Trap Network Capacitance
RDLAG	-	10	0	∞	Trap Network Resistance
IDIO	A	1e0	0	∞	Saturation current parameter when TRAPMOD=1
ATRAPVOFF	-	0.1	-∞	∞	V_{off} change due to trapping effects
BTRAPVOFF	-	0.3	0	∞	V_{off} change proportional to input power due to trapping effects

ATRAPETA0	-	0	-∞	∞	$ETA0$ change due to trapping effects
BTRAPETA0	-	0.05	-∞	∞	$ETA0$ change proportional to input power due to trapping effects
ATRAPRS	-	0.1	-∞	∞	RS change due to trapping effects
BTRAPRS	-	0.6	-∞	∞	RS change proportional to input power due to trapping effects
ATRAPRD	-	0.5	-∞	∞	RD change due to trapping effects
BTRAPRD	-	0.6	-∞	∞	RD change proportional to input power due to trapping effects
RTRAP1	Ohm	1	-	-	Trap network resistance
RTRAP2	Ohm	1	-	-	Trap network resistance
CTRAP1	F	10e-6	-	-	Trap network capacitance
CTRAP2	F	1e-6	-	-	Trap network capacitance
A1	-	0.1	-	-	Trap contribution to V_{OFF} (1st network)
VOFFTR	-	0.01	-	-	Trap contribution to V_{OFF} (2nd network)
CDSCDTR	-	0.01	-	-	Trap contribution to CDSCD (2nd network)
ETA0TR	-	0.01	-	-	Trap contribution to DIBL (2nd network)
RONTR1	-	0.01	-	-	Trap contribution to R_{on} (1st network)
RONTR2	-	0.01	-	-	Trap contribution to R_{on} (2nd network)
RONTR3	-	0.01	-	-	Bias independent trap contribution to R_{on}
ALPHAX	-	0.0	-inf	inf	Vgs dependence of trapping
ALPHAXD	-	0.0	-inf	inf	Vgd dependence of trapping
BETAX	-	0.05	-inf	inf	Vd dependence of trapping
GAMMAX	-	0.0	-inf	inf	Steady state or zero bias trapping parameter
ENO	-	1e4	0	inf	Nominal temperature emission rate
EA	-	0.5	0	inf	Activation energy of traps
CX	-	1e-7	0	inf	Trap capacitance

VXMAX	-	0.5	0	inf	Maximum trapping voltage
CY	-	1e-7	0	inf	Trap capacitance for 2nd network
ALPHAY	-	0.0	-inf	inf	Vgs dependence of 2nd trapping network
ALPHAYD	-	0.0	-inf	inf	Vgd dependence of 2nd trapping network
BETAY	-	0.05	-inf	inf	Vd dependence of 2nd trapping network
GAMMAY	-	0.0	-inf	inf	Steady state or zero bias 2nd trapping parameter
ENO1	-	1e4	0	inf	Nominal temperature emission rate for 2nd trapping network
EA1	-	0.5	0	inf	Activation energy of traps for 2nd trapping network
VYMAX	-	0.5	0	inf	Maximum trapping voltage

4.3.4 Field Plate Model Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
IMINFP1	A	1.0e-15	0	∞	Minimum Drain Current FP1 region
VOFFFP1	V	-25.0	-500.0	5	VOFF for FP1
DFP1	m	50.0e-9	0.1e-9	∞	Distance of FP1 from 2-DEG Charge
LFP1	m	1.0e-6	0	∞	Length of FP1
KTFP1	-	50.0e-3	-∞	∞	Temperature Dependence for VOFFFP1
U0FP1	$m^2/V-s$	100.0e-3	0	∞	FP1 region mobility
VSATFP1	m/s	100.0e3	0	∞	Saturation Velocity of FP1 region
NFACTORFP1	-	0.5	0	∞	Sub-VOFF Slope parameters
CDSCDFP1	-	0	0	∞	Sub-VOFF Slope Change due to Drain Voltage
ETA0FP1	-	1.0e-9	0	∞	DIBL Parameter
VDSCALEFP1	V	10.0	0	∞	DIBL Scaling VDS
GAMMA0FP1	-	2.12e-12	0	1.0	Schrodinger-Poisson solution variable
GAMMA1FP1	-	3.73e-12	0	1.0	Schrodinger-Poisson solution variable

IMINFP2	A	1.0e-15	0	∞	Minimum Drain Current FP2 region
VOFFFP2	V	-50.0	-500.0	5	VOFF for FP2
DFP2	m	100.0e-9	0.1e-9	∞	Distance of FP2 from 2-DEG Charge
LFP2	m	1.0e-6	0	∞	Length of FP2
KTFP2	-	50.0e-3	-∞	∞	Temperature Dependence for VOFFFP2
U0FP2	$m^2/V-s$	100.0e-3	0	∞	FP2 region mobility
VSATFP2	m/s	100.0e3	0	∞	Saturation Velocity of FP2 region
NFACTORFP2	-	0.5	0	∞	Sub-VOFF Slope parameters
CDSCDFP2	-	0	0	∞	Sub-VOFF Slope Change due to Drain Voltage
ETA0FP2	-	1.0e-9	0	∞	DIBL Parameter
VDSCALEFP2	V	10.0	0	∞	DIBL Scaling VDS
GAMMA0FP2	-	2.12e-12	0	1.0	Schrodinger-Poisson solution variable
GAMMA1FP2	-	3.73e-12	0	1.0	Schrodinger-Poisson solution variable
IMINFP3	A	1.0e-15	0	∞	Minimum Drain Current FP3 region
VOFFFP3	V	-75.0	-500.0	5	VOFF for FP3
DFP3	m	150.0e-9	0.1e-9	∞	Distance of FP3 from 2-DEG Charge
LFP3	m	1.0e-6	0	∞	Length of FP3
KTFP3	-	50.0e-3	-∞	∞	Temperature Dependence for VOFFFP3
U0FP3	$m^2/V-s$	100.0e-3	0	∞	FP3 region mobility
VSATFP3	m/s	100.0e3	0	∞	Saturation Velocity of FP3 region
NFACTORFP3	-	0.5	0	∞	Sub-VOFF Slope parameters
CDSCDFP3	-	0	0	∞	Sub-VOFF Slope Change due to Drain Voltage
ETA0FP3	-	1.0e-9	0	∞	DIBL Parameter
VDSCALEFP3	V	10.0	0	∞	DIBL Scaling VDS
GAMMA0FP3	-	2.12e-12	0	1.0	Schrodinger-Poisson solution variable
GAMMA1FP3	-	3.73e-12	0	1.0	Schrodinger-Poisson solution variable
IMINFP4	A	1.0e-15	0	∞	Minimum Drain Current FP4 region
VOFFFP4	V	-100.0	-500.0	5	VOFF for FP4
DFP4	m	200.0e-9	0.1e-9	∞	Distance of FP4 from 2-DEG Charge

LFP4	m	1.0e-6	0	∞	Length of FP4
KTFP4	-	50.0e-3	-∞	∞	Temperature Dependence for VOFFFP4
U0FP4	$m^2/V-s$	100.0e-3	0	∞	FP4 region mobility
VSATFP4	m/s	100.0e3	0	∞	Saturation Velocity of FP4 region
NFACTORFP4	-	0.5	0	∞	Sub-VOFF Slope parameters
CDSCDFP4	-	0	0	∞	Sub-VOFF Slope Change due to Drain Voltage
ETA0FP4	-	1.0e-9	0	∞	DIBL Parameter
VDSCALEFP4	V	10.0	0	∞	DIBL Scaling VDS
GAMMA0FP4	-	2.12e-12	0	1.0	Schrodinger-Poisson solution variable
GAMMA1FP4	-	3.73e-12	0	1.0	Schrodinger-Poisson solution variable

4.3.5 Capacitance Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
CGSO	F/m	1e-18	-	-	Gate-Source overlap capacitance parameter
CGDO	F/m	1e-18	-	-	Gate-Drain overlap capacitance parameter
CDSO	F/m	1e-18	-	-	Drain-Source capacitance parameter
CGDL	$F/m/V$	0e-15	-	-	Parameter for bias V_{ds} dependence in CGDO
VDSATCV	V	100	-	-	Saturation voltage at drain side in CV model
CBDO	F/m	0e-15	0	∞	Substrate capacitance parameter
CBSO	F/m	0e-15	0	∞	Substrate capacitance parameter
CBGO	F/m	0e-15	0	∞	Substrate capacitance parameter
CFG	F/m	0e-18	-	-	Gate fringing capacitance parameter
CFD	F/m	0e-12	-	-	Drain fringing capacitance parameter
CFGD	F/m	0e-13	0	∞	Fringing capacitance parameter
CFGDSM	F/m	1.0e-24	0	∞	Capacitance smoothing parameter
CFGD0	F/m	0e-12	0	∞	Fringing capacitance parameter

CJ0	F/m	0e-12	-	-	Zero V_{ds} access region capacitance parameter
VBI	V	0.9	-	-	Drain end built-in potential parameter
MZ	-	0.5	-	-	Parameter governing decay of C_{accd} for high V_{ds}
AJ	-	115e-3	-	-	Parameter for governing bias independent value of C_{ds} at low V_{ds}
DJ	-	1	-	-	Parameter governing decay of C_{accd} for high V_{ds}

4.3.6 Quantum Mechanical Effects

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
ADOSI	-	0	0	∞	Quantum mechanical effect prefactor cum switch in inversion
BDOSI	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0I	-	1e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSFP1	-	0	0	∞	Quantum mechanical effect pre-factor cum switch in inversion
BDOSFP1	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0FP1	-	1.0e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSFP2	-	0	0	∞	Quantum mechanical effect pre-factor cum switch in inversion
BDOSFP2	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0FP2	-	1.0e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSFP3	-	0	0	∞	Quantum mechanical effect pre-factor cum switch in inversion

BDOSFP3	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0FP3	-	1.0e-3	0	∞	Charge centroid parameter - starting point for QME in inversion
ADOSFP4	-	0	0	∞	Quantum mechanical effect pre-factor cum switch in inversion
BDOSFP4	-	1	0	∞	Charge centroid parameter - slope of CV curve under QME in inversion
QM0FP4	-	1.0e-3	0	∞	Charge centroid parameter - starting point for QME in inversion

4.3.7 Cross Coupling Capacitance Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
CFP1SCALE	-	0	0	∞	Coupling of charge under FP1
CFP2SCALE	-	0	0	∞	Coupling of charge under FP2
CFP3SCALE	-	0	0	∞	Coupling of charge under FP3
CFP4SCALE	-	0	0	∞	Coupling of charge under FP4
CSUBSCALEI	-	0	0	∞	Sub Capacitance scaling parameter
CSUBSCALE1	-	0	0	∞	Sub Capacitance scaling parameter
CSUBSCALE2	-	0	0	∞	Sub Capacitance scaling parameter
CSUBSCALE3	-	0	0	∞	Sub Capacitance scaling parameter
CSUBSCALE4	-	0	0	∞	Sub Capacitance scaling parameter

4.3.8 Gate Resistance Parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
XGW	-	0	0	∞	Dist from gate contact center to device edge
NGCON	-	1	1	2	Number of gate contacts
RSHG	Ω/square	0.1	0	∞	Gate sheet resistance

4.3.9 Noise Model Parameters

Name	Unit	Default	Min	Max	Description
NOIA	-	-1.5e29	-	-	Flicker Noise parameter
NOIB	-	1e32	-	-	Flicker Noise parameter
NOIC	-	0.55e34	-	-	Flicker Noise parameter
EF	-	1	0	∞	Exponent of frequency; Determines slope in log plot
TNSC	-	1	0	∞	Thermal noise scaling parameter

4.3.10 Drain-Source Breakdown Model Parameters

Name	Unit	Default	Min	Max	Description
BVDSL	V	200	10	∞	Drain-source breakdown voltage due to punch-through
ASL	A/m	0	0	∞	Breakdown current multiplier, also serves as model switch
NSL	-	10.0	1.0	∞	Exponent parameter in breakdown model
KASL	-	0.0	$-\infty$	∞	Temperature dependence of ASL
KNSL	-	0.0	$-\infty$	∞	Temperature dependence of NSL
KBVDSL	-	0.0	$-\infty$	∞	Temperature dependence of BVDSL

4.3.11 Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
AT	-	0	$-\infty$	∞	Temperature Dependence for saturation velocity
UTE	-	-0.5	-10	0	Temperature dependence of mobility
KT1	-	0e-3	$-\infty$	∞	Temperature Dependence for Voff
KNS0	-	0	-	-	Temperature Dependence for 2-DEG charge density at access region

ATS	-	0	-	-	Temperature Dependence for saturation velocity at access region
UTES	-	0	-	-	Temperature dependence of mobility at access region: Source Side
UTED	-	0	-	-	Temperature dependence of mobility at access region: Drain Side
KRSC	-	0	-	-	Temperature dependence of Source Contact Resistance for RDSMOD2
KRDC	-	0	-	-	Temperature dependence of Drain Contact Resistance for RDSMOD2
KTVBI	-	0	-	-	Temperature Dependence for VBI
KTCFG	-	0e-3	-	-	Temperature Dependence for Gate fringing capacitance
KTCFGD	-	0e-3	-	-	Temperature Dependence for fringing capacitance
RTH0	Ohm	5	0	∞	Thermal Resistance
CTH0	F	1e-9	0	∞	Thermal Capacitance
TALPHA	-	-2	-	-	Temperature exponent of Rtrap

4.3.12 Substrate leakage model parameters

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
ISBL	A/m^{-2}	0e-25	-	-	Source-to-substrate current multiplier parameter
NSB	-	100	-	-	Source-to-substrate non-linearity parameter
VBISB	V	-	-	-	Leakage current turn-on voltage parameter for source-to-substrate leakage.
IDBL	A/m^{-2}	0e-25	-	-	Drain-to-substrate current multiplier parameter
NDB	-	100	-	-	Drain-to-substrate non-linearity parameter

VBIDB	V	-	-	-	Leakage current turn-on voltage parameter for drain-to-substrate leakage.
KTISB	V	-	-	-	Temperature dependence for ISBL.
KTIDB	V	-	-	-	Temperature dependence for IDBL.
KTNSB	V	-	-	-	Temperature dependence for NSB.
KTNDB	V	-	-	-	Temperature dependence for NDB.
KTVBISB	V	-	-	-	Temperature dependence for VBISB.
KTVBIDB	V	-	-	-	Temperature dependence for VBIDB.

5 Parameter Extraction and Model Validation Tests

5.1 Parameter Extraction Procedure

5.1.1 DC I-V Parameter Extraction

The DC model parameter extraction flow for ASM-GaN-HEMT model can be summarized in the figure given below. The following steps describe the flow:

1. Set physical parameters in the model such as L, W, NF, $TBAR$, LSG and LDG. These parameters are generally available to the device technologist.

2. First the extractetion is focussed on getting the linear VD condition parameters. From linear drain-current bias conditions i.e. V_D 50 - 100 mV $ID-VG$ characteristics, extract the parameters such as $VOFF$ and $NFACTOR$. $VOFF$ is the cut-off voltage and is a very important parameter. A rough estimate of $VOFF$ is the VG values in the $ID-VG$ plot in linear scale from which ID starts to rise. This rough value can be fine-tuned as one moves along in the parameter extraction flow for best fits. $NFACTOR$ controls the sub-threshold slope of the device and this can be extracted by fitting the model to linear VD condition $ID-VG$ characteristics on logarithm scale.

The plots below show the affect of parameters on the device characteristics.

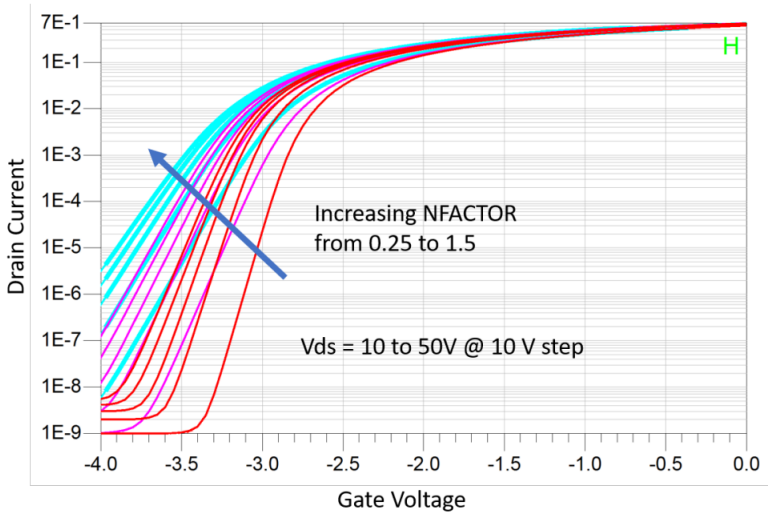

Figure 11: Effect of NFACTOR on Id-VG.

3. After $VOFF$ and $NFACTOR$ carrier low-field mobility $U0$ and mobility vertical-field dependence parameters UA and UB should be extracted from linear VD condition $ID-VG$ characteristics. Trans-conductance GM and its derivatives GM' and GM'' in the linear VD condition can be be accurately modeled using $U0$, UA and UB parameters. It is important to note here that the series resistance also affects linear $ID-VG$. It is helpful to keep the values of series resistance parameters RSC, $NS0ACCS, D$, $MEXPACSS, D$ to reasonable values for this step. The starting values for series resistance parameters (which will be fine-tuned) can be from special measurements like TLM structures or simply close to previously extracted devices.

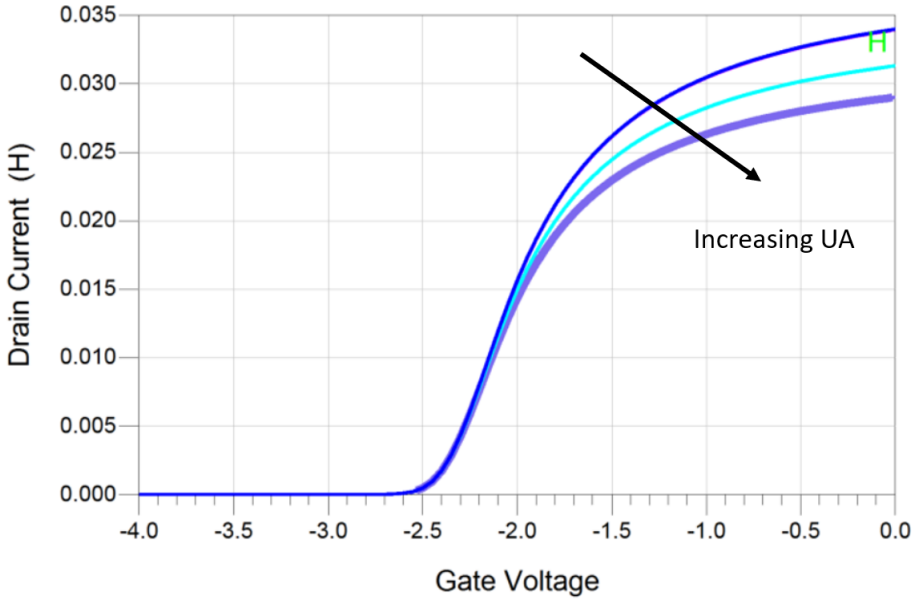

Figure 12: Effect of UA on Id-VG.

3.1 For devices in which substrate voltage is also applied. The variation in cut-off voltage, mobility and 2-DEG access region density is modeled with ASUB, UC, and KSUB model parameters. A plot showing ID-VG with varying substrate voltage is shown below.

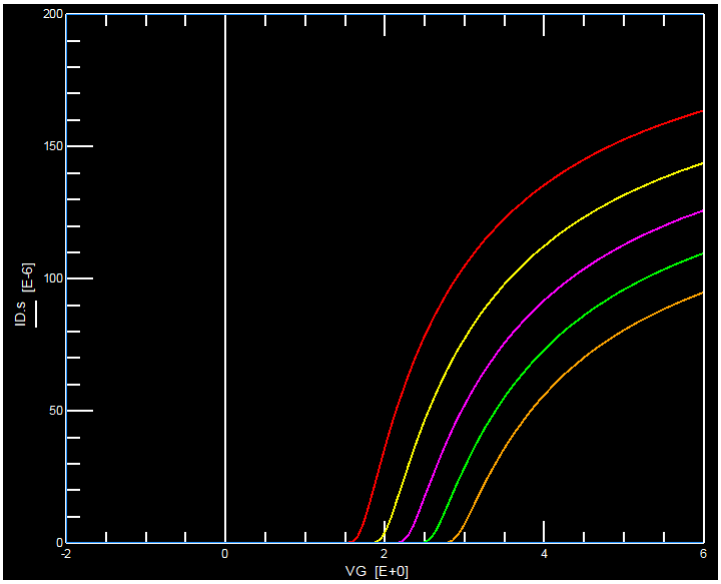

Figure 13: Modelling effects on substrate voltage on I-V with ASUB, KSUB and UC.

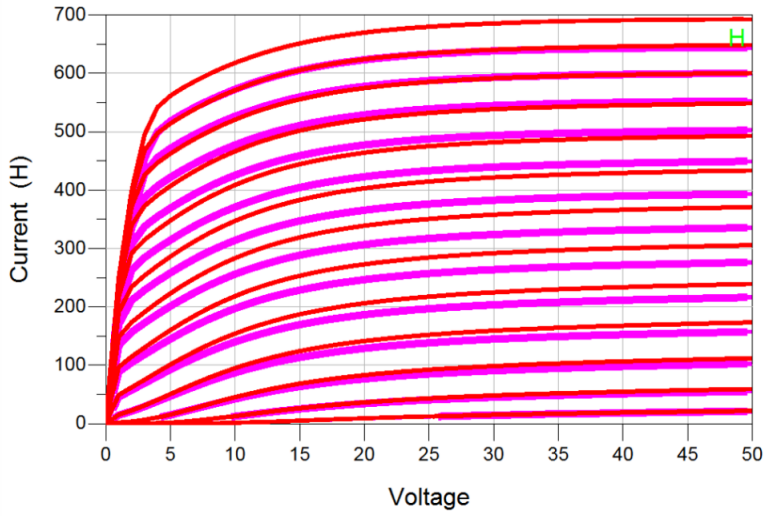

Figure 14: Effect of both RSC and RDC on Id-Vd.

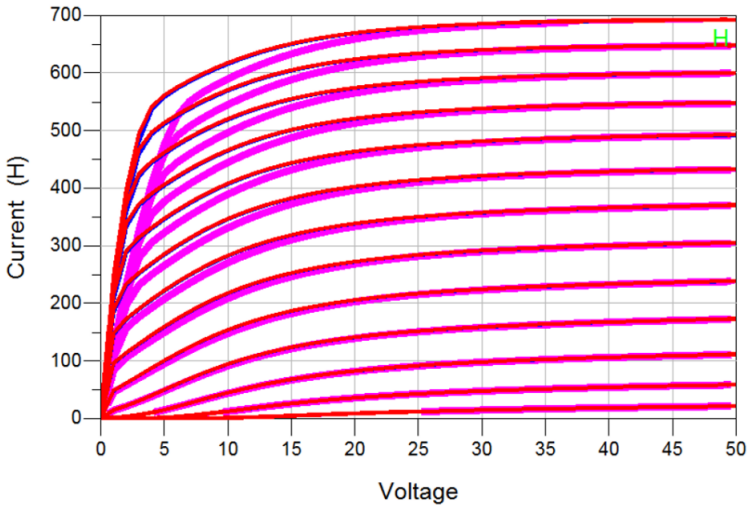

Figure 15: Effect of RDC only on Id-Vd.

4. With linear VD condition fitting done, the parameters from the high VD conditions should be extracted. As done above, first we focus on $ID - VG$ characteristics for high VD conditions and extract the sub-Voff or low-current region parameters. Due to the drain-induced barrier lowering effect, the cut-off voltage in high VD condition decreases and this can be modeled with the extraction of DIBL parameters $ETA0$ and $VDSCALE$. The sub-threshold slope also degrades for high VD conditions and this can be modeled with parameter $CDSCD$ in the ASM-GaN-HEMT model.

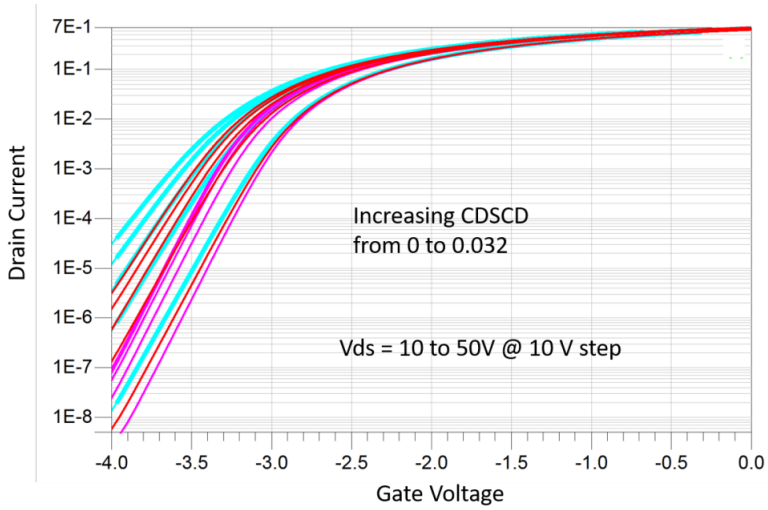

Figure 16: Effect of CDSCD on Id-Vg.

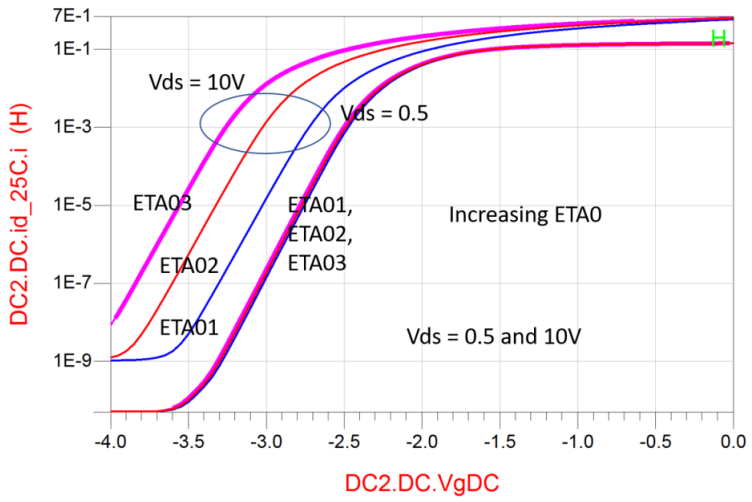

Figure 17: Effect of ETA0 on Id-Vg. ETA0 affects the saturation condition.

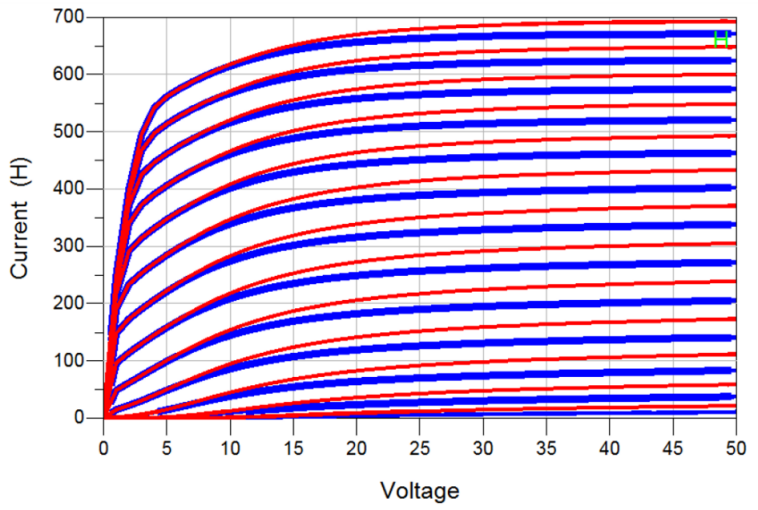

Figure 18: Effect of VDSCALE on Id-Vd. Red color curves are with lower VDSCALE.

5. Next, above-Voff fitting for high VD $ID-VG$ curved is done. The key parameters for this fitting are the velocity saturation parameters $VSAT$, channel-length modulation parameter ($LAMBDA$) and the non-linear series resistance parameters $NS0ACCS, S$, $MEXPACCS, D$ and $U0ACCS, D$. These parameters can be extracted by fitting high VD $ID-VG$ in linear scale. $VSAT$ is best extracted from intermediate current levels for which GM in high VD conditions is still rising with VG. The non-linear series resistance causes GM to drop with VG and the associated parameters should be tuned to fit this region. Self-heating will also have an impact in high current and high drain-voltage regions and the thermal-resistance of the device should be set to a reasonable value from special measurements or TCAD simulations or from previous knowledge. Accurate modeling of trans-conductance for different VD conditions can be achieved with the parameters indicated in this step. It is good to go back to linear $IDVG$ after this step and do a very fine adjustments for further improved fits.

6. Next, the output characteristics $ID-VD$ should be looked at. With $IDVG$ fitted under different VD conditions, $IDVD$ should be already accurately modeled. Parameters can be fine-tuned to get improvement, if required.

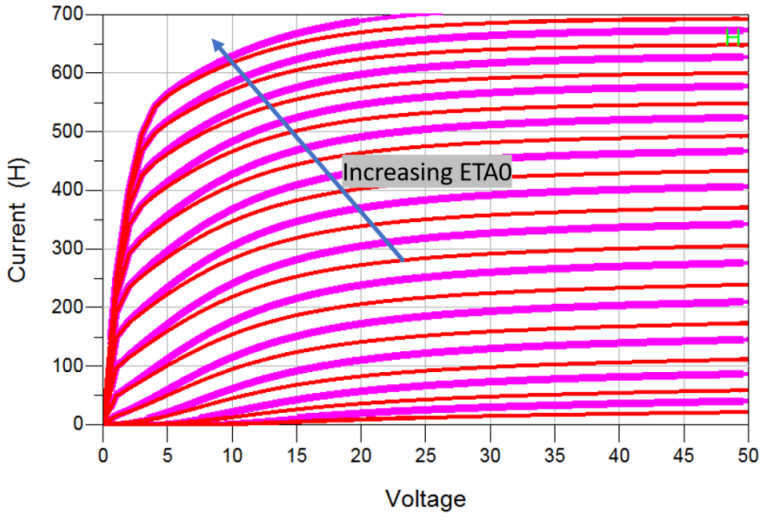

Figure 19: Effect of ETA0 on Id-Vd.

Above steps completes DC parameter extraction flow for ASM-GaN-HEMT model at room temperature. For modeling DC I-V's at other temperatures, temperature scaling equations on the key model parameters are implemented in the model. Using the temperature parameters DC I-V's at multiple temperatures can be modeled.

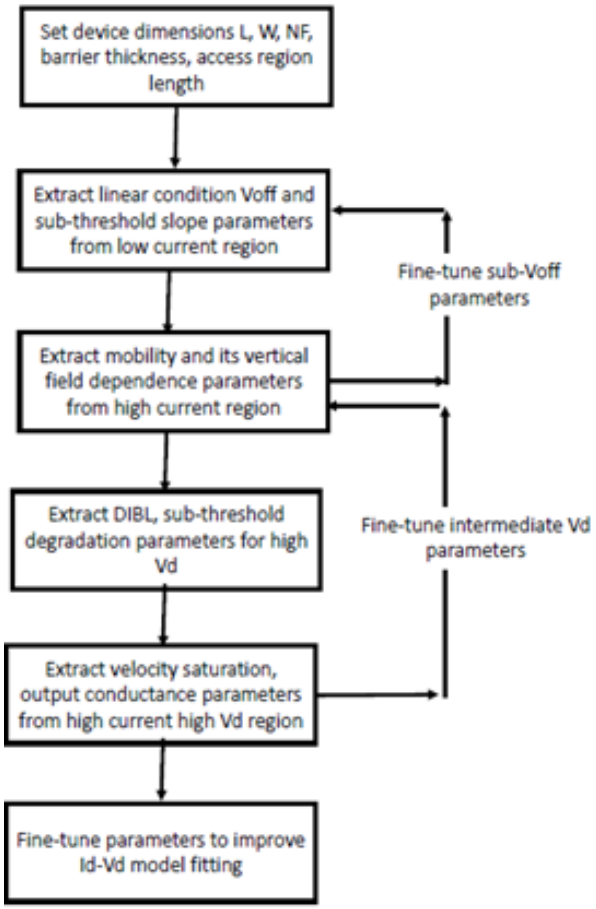

Figure 20: Parameter extraction procedure

5.1.2 Radio-frequency Parameter Extraction

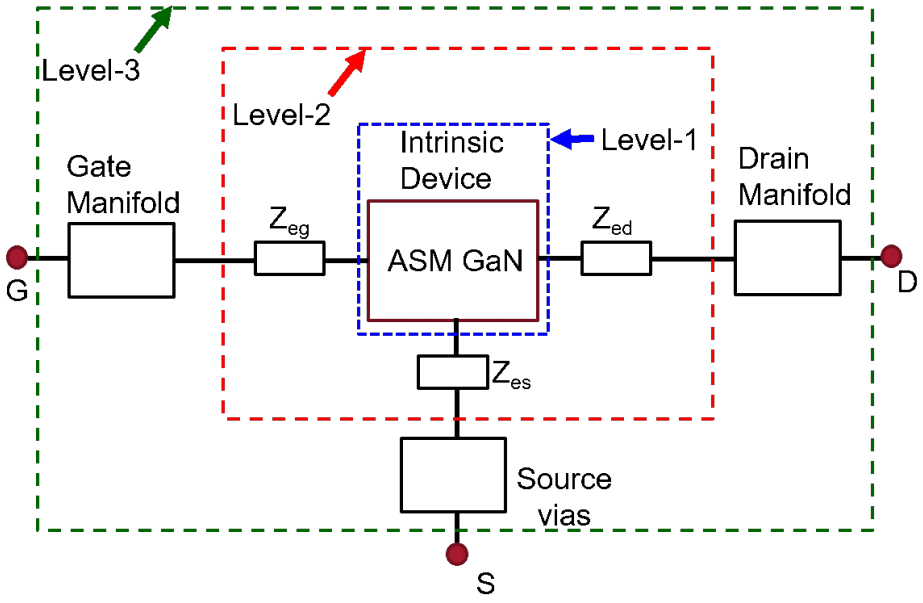

Figure 21: ASM GaN Model Intrinsic Device with parasitic for full radio-frequency model

After, DC parameters, S-parameter can be modeled with the model. For this, the parasitic components need to be accounted for and a sub-circuit should be build around the model to represent all the parasitic capacitances and inductances. The parasitic elements associated with the actual layout and the position of the measurement reference planes needs to be included with the intrinsic ASM GaN model. The complete model can be visualized as shown in Fig. 21, consisting of three levels: level-1 is the intrinsic ASM GaN model, level-2 is the model of electrode inductances, resistances, and capacitances associated with metal lines of the electrodes represented by Z_{ex} with x = g, d, or s, and level-3 are the parasitic elements for the source via, gate- and drain-manifolds. Level-3 parasitic effect can be either modeled with a lumped element network, or the S2P files from EM simulations can be directly used for modeling this region. Level-2 parasitic elements can be extracted from the standard extraction flow in literature.

Using the correct parasitic networks, the gate-source, gate-drain, and drain-source capacitance can be observed from measurements and the model from imaginary parts

of Y-parameters. The presence of field-plates influence the capacitance of the device. PLot below shows the affect of gate-connected field plate on Cgs.

After accounting for the field-plate capacitance with the help of field-plate geometry parameters $CGSO$ can be tuned to set the value of C_{gs} for V_{gs} biases below the cut-off voltage. he parameters $CGSO$, $ADOSI$, $BDOSI$ can be used to tune the C_{gs} versus V_{gs} behavior. $ADOSI$, and $BDOSI$ can tune the rate of C_{gs} increase with V_{gs}. $NFACTOR$ will also affect the bias dependence of Cgs, NFACTOR will also affect the slope of Log-ID versus Vg.

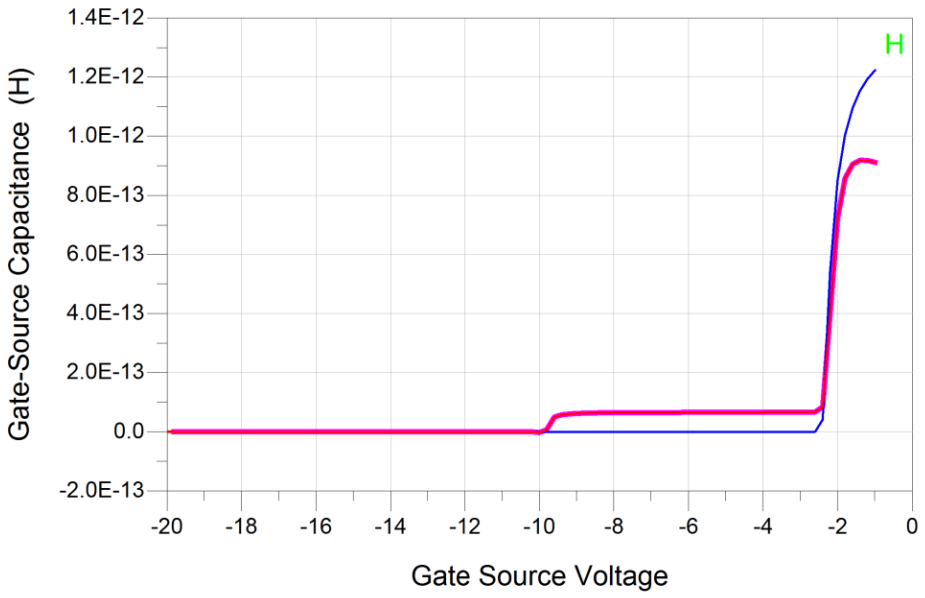

Figure 22: Gate connected field-plate affect Cgs. Blue is without field-plate and purple is with field-plate. The cut-off voltage is set to -10 V where the increase in capacitance can be seen.

Next, C_{gd} versus V_{ds} characteristics, the $CGDL$ and $VDSATCV$ parameter can be tuned to control the decrease in C_{gd} with the increase in V_{ds}. Typical behavior of Cgd and the effect of parameters on the behavior is shown in the plot below.

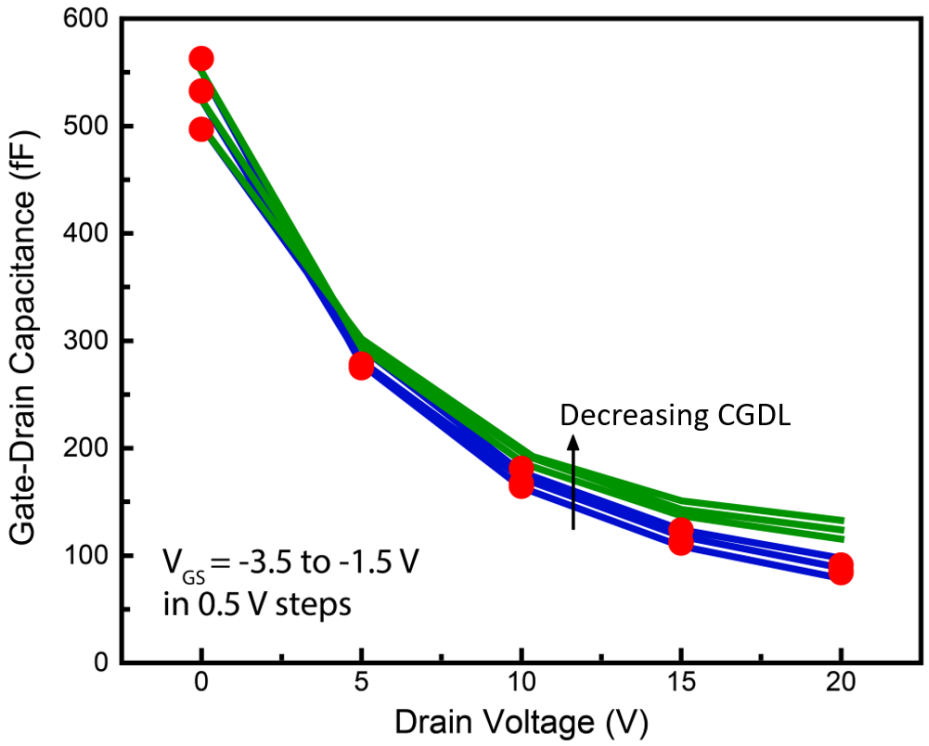

Figure 23: Cgd versus Vds and the impact of CGDL.

For fitting the C_{ds} parameters, $CDSO$, $CJ0$, AJ, and DJ can be used. In addition to these parameters, the presence of source connected field plate also affects Cds.

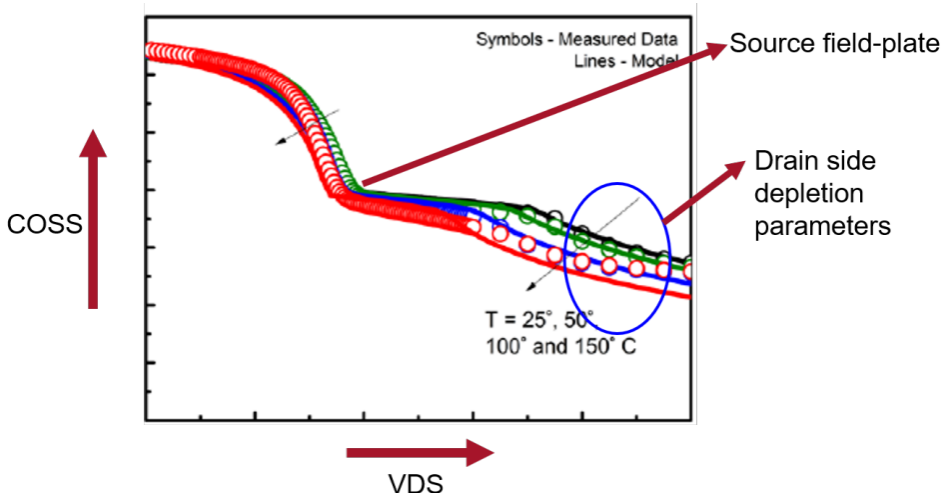

Figure 24: Cds versus Vds

The effect of gate-resistance seen at high frequency can be modeled with gate-resistance parameters $RSHG$ and XGW.

The small signal g_m, and g_{ds} for different bias conditions directly originates from already model I-V behavior and comes out reasonably close to the measured data for low frequency. At higher frequency, the frequency dependence in g_m and g_{ds} coming from self-heating can be tuned with $CTH0$ parameter.

After, S-parameter modeling at multiple DC bias points, large signal RF modeling of input power sweep curves and load/source-pull measurements can be attained. One of the important region of I-V to model for large signal performance if the knee region in the I-V region. This region is controlled mainly by the access region resistance parameters, and the smoothing parameters DELTA, MEXPACCS, and MEXPACCD.

5.2 Extraction of manufacturing variability

This section describes a methodology to use ASM-HEMT model to use model in Monte-Carlo (MC) simulations and model the variability in electrical device performance parameters. The fabrication process causes variability in device geometry parameters which include gate-length L, gate-width W, barrier thickness T_{bar}, source-gate access region length L_{sg}, and drain-gate access region length L_{dg}. The variability in device

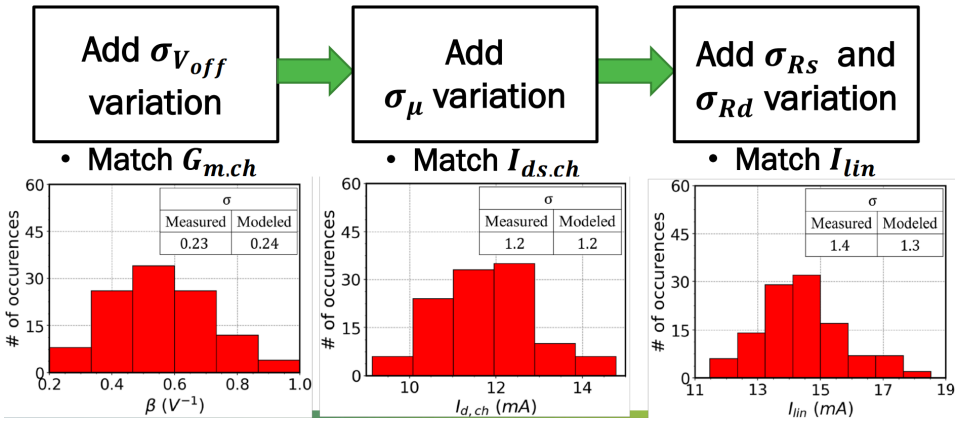

Figure 25: Process to extract model parameters systematically

geometry as measured by standard deviations of geometry parameters $\boldsymbol{\sigma_G}$ thus include,

$$\boldsymbol{\sigma_G} = (\sigma_L, \sigma_{Tbar}, \sigma_{Lsg}, \sigma_W, \sigma_{Ldg}). \tag{5.2.1}$$

$\boldsymbol{\sigma_G}$ are typically monitored in the foundry process. These variations can be directly set in the model with information on the foundry tolerances.

After setting $\boldsymbol{\sigma_G}$ MC simulations performed on a nominal device ASM-HEMT model can be used to observe the variations in electrical performance parameters such as transconductance G_m and compare it with measurements. Typically only geometry variability is not enough to represent the variability in electrical performance parameters. A systematic flow to extract variations in electrical model parameters is shown in Fig. 25. As shown in Fig. 25 the first step is to extract variability in $VOFF$ from current to transconductance ratio $\beta = \frac{I_ch}{G_{m,ch}}$. β should be measured from linear region transfer characteristics at intermediate gate-voltage where total current is not limited by the access region resistance. Then the variation in mobility can be extraction by modeling the variation in I_ch and then variations in access region resistances can be modeled by including the variations on series resistance parameters RS and RD. Refer to [35] for further details.

5.3 Access region resistance model for resistance modeling

The non-linear access region resistance model in ASM-HEMT can be applied to model the 2-DEG resistors in the foundry process. To set the model for such use case all the field-plates in the model should be turned off by setting FPMOD switches to 0. Gate-length should be set minimum value of 20e-9 and $VOFF$ set to -10V. Gate and source terminal need to be shorted for modeling the two terminal resistance. The total length of the resistance will be set by sum of LSG and LDG model parameters. The access region mobility and saturation velocity parameters can be used to model the non-linear behavior of the resistances.

5.4 Results of Benchmark Tests

Model has successfully passed Gummel symmetry, harmonic balance simulation, AC symmetry and reciprocity tests. Results of these tests' are given below.

5.4.1 Gummel Symmetry Test Results

The Gummel symmetry test is used to test the correctness of the model with respect to drain source symmetry. For GaN HEMTs, it is common to use different source and drain gate lengths, which make the full device asymmetric. The intrinsic device region is, however, still symmetric and the compact model for the intrinsic device should pass the Gummel symmetry test[36],[37].

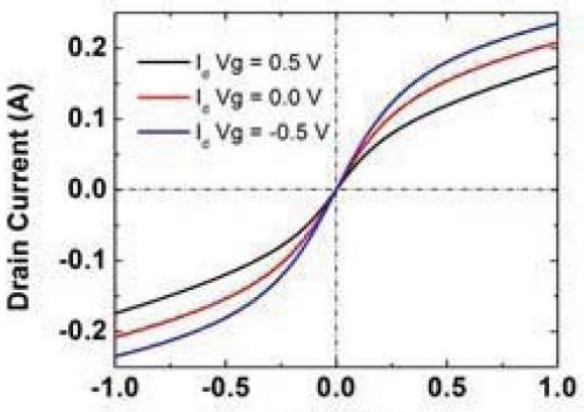

Figure 26: Drain current vs V_x

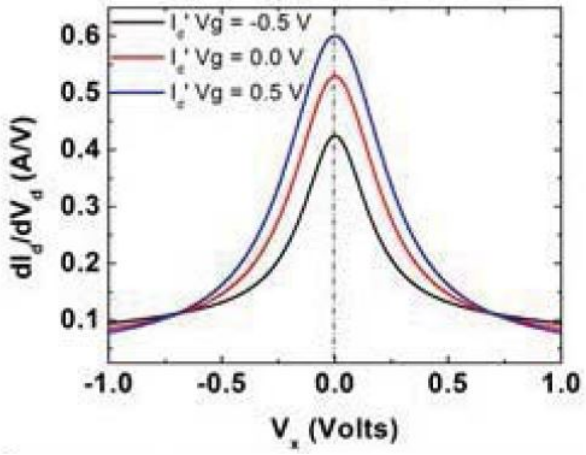

Figure 27: First derivative of I_d vs V_x

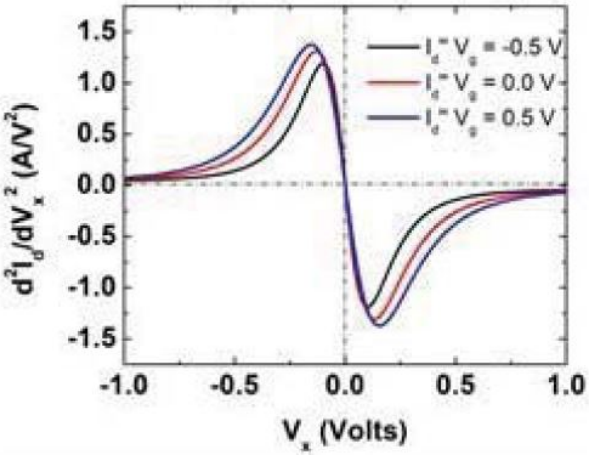

Figure 28: 2nd derivative of I_d vs V_x

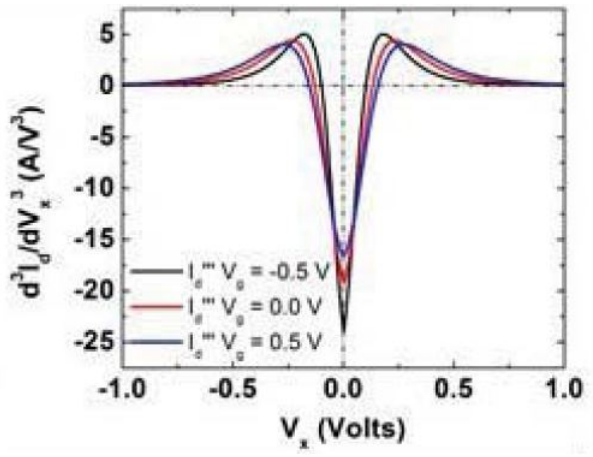

Figure 29: 3rd derivative of I_d vs V_x

Results are shown in 26,27,28 and 29.

5.4.2 Harmonic Balance Simulation Results

Distortion analysis is important for evaluation of RF circuit performance and correct model behavior for distortion analysis can be tested by the harmonic balance simulations[36],[37].

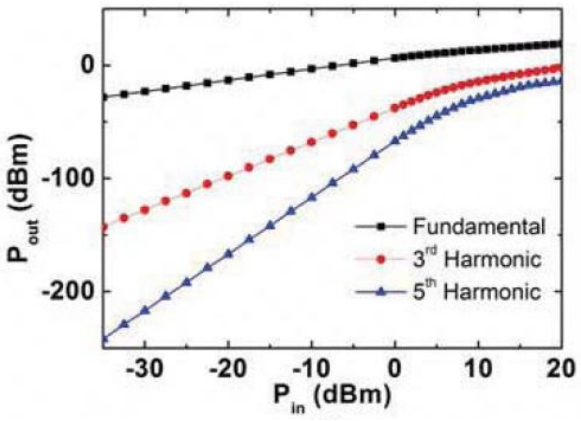

Figure 30: Single tone harmonic balance simulation result

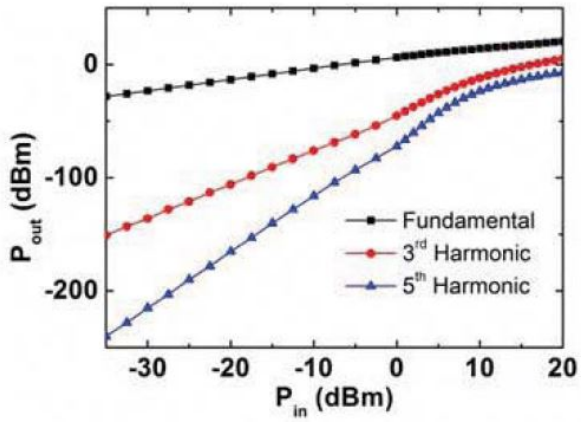

Figure 31: Two tone harmonic balance simulation result

Figures 30 and 31 show the results for harmonic balance simulation results for two harmonics.

5.4.3 AC Symmetry Test Results

In addition to the current expression, the charge and hence capacitance expressions in the model should also satisfy the symmetry condition. This is also known as AC symmetry test. It is tested using two expressions[36],[37].

$$\delta_{cg} = \frac{C_{GS} - C_{GD}}{C_{GS} + C_{GD}} \tag{5.4.1}$$

$$\delta_{csd} = \frac{C_{SS} - C_{DD}}{C_{SS} + C_{DD}} \tag{5.4.2}$$

These functions and their derivatives are shown in figures below.

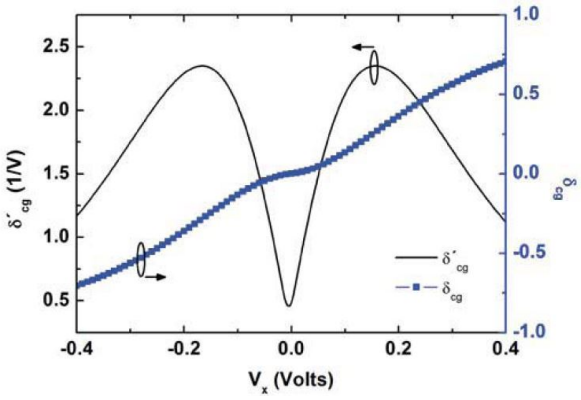

Figure 32: δ_{cg} and $\delta_{cg}^{'}$ vs V_x

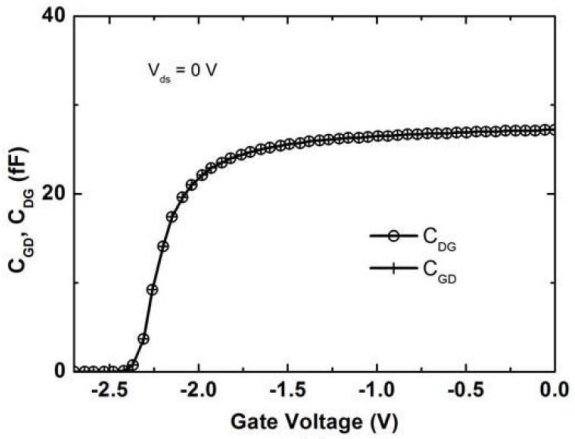

Figure 33: δ_{csd} and $\delta_{csd}^{'}$ vs V_x

5.4.4 Reciprocity Test Results

Another important test for the correct behavior of the capacitance model is the reciprocity of capacitances at zero drain– source voltage (V_{ds}). In general, the capacitance between the two nodes i and j of the device are nonreciprocal, i.e., $C_{ij} = C_{ji}$. However, $C_{ij} = C_{ji}$ at $V_{ds} = 0$ and the model should mimic this behavior[36],[37].

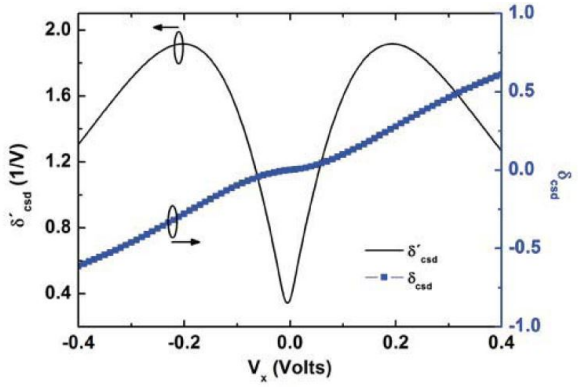

Figure 34: C_{GD}, C_{DG} vs Gate Voltage at $V_{DS} = 0$

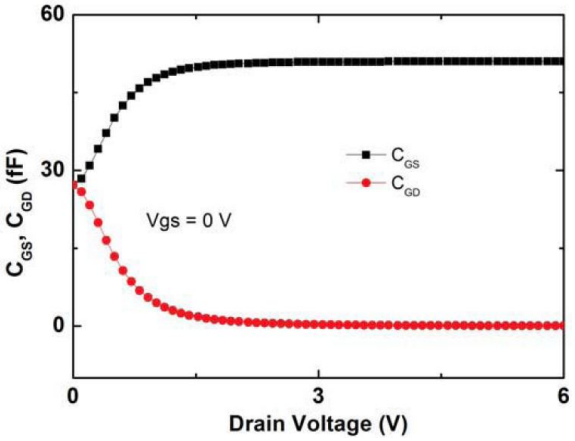

Figure 35: C_{GS} and C_{GD} vs Drain voltage at $V_{DS} = 0$

Test results are shown in 34 and 35.

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