

MIT Virtual Source GaN FET (MVSG) Compact Model Manual

MVSG_CMC Verilog-A Model: Version 4.0.0

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1 Introduction

Gallium Nitride (GaN) based field-effect transistors (FET) including high electron mobility transistors (HEMTs) are starting to be used in wireless communication and power conversion applications in industry [1]. This is because of the possibilities of higher switching voltage and switching frequency with GaN HEMTs in comparison to conventional Si-FETs, which enables delivery of high power levels at high frequencies (HF) for radio-frequency (RF) applications, as well as scaling of passive components in high-voltage (HV) circuits resulting in high efficiency and lower footprint of power conversion boards.

Compact models are necessary for designing such RF-circuits (e.g. power amplifiers) and HV-circuits (e.g. GaN-FET switching converters). Several compact models of GaN HEMTs have been developed for this purpose [2]. In this work the physics based compact model originated from Prof. Dimitri Antoniadis' group at MIT based on the virtual-source (VS) concept [3] for these GaN devices is discussed. Details of the Verilog-A model equations along with parameter extraction procedure are explained.

2 GaN HEMT: Working Principle

Gallium Nitride HEMT is an attractive candidate for HV and HF applications. This is due to superior and unique properties of the AlGaN/GaN system such as high electron density ($\sim 1 \times 10^{13} \text{ cm}^2$), high electron mobility in two dimensional electron gas (2DEG) ($\sim 1500 \text{ cm}^2/\text{Vs}$), good thermal conductivity ($\sim 1.5 \text{ WK/cm}$) and high breakdown field ($\sim 3.0 \text{ MV/cm}$). These properties are compared with other materials and summarized in Table 1.

Semiconductor		Si	AlGaAs/ InGaAs	InAlAs/ InGaAs	SiC	AlGaN/ GaN
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm^2/Vs	1500	8500	5400	700	1500-2200
Saturated (peak) electron velocity	$\times 10^7 \text{ cm/s}$	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0

Table 1: Table showing material properties. GaN shows a combination of high electron mobility, electron velocity and breakdown field [2]

The above-mentioned properties of GaN material systems results in superior switching figure-of-merit ($BV^2/R_{on}Q_G$) for GaN transistors used in 600-1200V applications. The plot of Breakdown voltage (BV) vs. On-resistance(R_{on}) of the three competing material systems for this voltage regime is shown in Fig. 1a. As can be seen, for a given BV , the R_{on} of GaN beats the Si and SiC limits; and it is this combination of good transport properties and high breakdown field that opens up the RF and HV application domains to GaN HEMTs.

GaN-based HEMTs, similar to other HEMTs, are field effect transistors (FETs) having a hetero-junction formed between two materials (in this case AlGaN and GaN) with different lattice constants. A schematic of the device structure is shown in Fig. 2a. The difference in electron affinity (χ) and band gap (E_g) results in the formation of a nearly triangular

potential well at the interface on the GaN side where electrons can be confined to form a 2DEG as shown in Fig. 2b. However, the cause for the 2DEG is different from other HEMT devices.

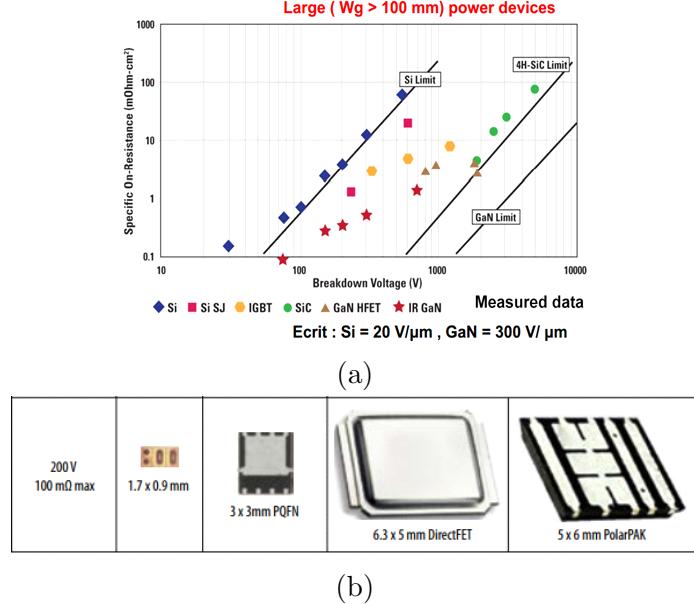


Figure 1: (a) BV vs. R_{on} of Si, SiC and GaN material system highlighting the superior DC-FoM of GaN HEMTs that makes (b) high frequency makes smaller circuit footprint possible [2].

The polar nature of the AlGaN/GaN system results in spontaneous polarization and in addition, the difference in lattice constants of the two layers results in piezoelectric polarization. In GaN HEMTs, the 2DEG is not induced by doping but instead by donor-like surface states on the AlGaN layer facilitated by spontaneous and piezoelectric electric field in AlGaN layer.

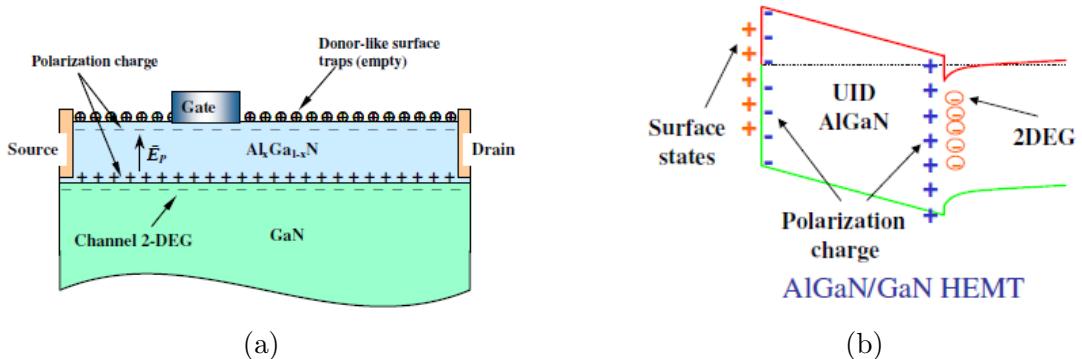


Figure 2: (a) Device structure schematic. (b) Band diagram of heterostructure showing different types of charges

Confinement of electrons in the quantum well and absence of dopants in the channel result in high mobility and peak velocity. Operation of the device requires a gate terminal

to modulate the 2DEG and hence drain to source current (I_{DS}). Since the 2DEG exists due to the heterostructure, a negative gate voltage is required to deplete it under the gate and prevent current flow. Therefore, GaN HEMTs without special gate stack engineering are normally-on (depletion-mode, D-mode) devices. Recent developments have introduced various structures and methods, such as recessed gate and p-type GaN gate to enable normally-off (enhancement-mode, E-mode) devices. Further details on the working principle can be found in [2]. With this basic understanding of device operation, we can look at the approach taken by the MIT Virtual Source GaN FET (MVSG) compact model to capture the device behavior under operating bias voltage.

3 MVSG Model

Typical device structure of GaN HEMT is shown in Fig. 3a. There are five distinct regions of the device requiring modeling attention, including intrinsic transistor region, field plate regions on the source and drain sides, and access regions on the source and drain. The intrinsic transistor region is the region under the gate, where the 2DEG is modulated by the gate voltage (V_G). The two regions next to the gate on the source and drain sides are the field plate regions which augment breakdown voltage capability of GaN HEMTs. MVSG supports up to four optional field plates on both the source and drain sides. The two access regions represent the ungated regions on the source and drain sides as these devices are not self-aligned. MVSG has the option to model the access regions (between source-gate and drain-gate) as non-linear implicit-gate transistors or linear resistances.

The MVSG model captures carrier transport in these different regions of the device with the help of a simplified sub-circuit model shown in Fig. 3b. More details of the model equations can be found in [2]. In this manual, the implementation of the model equations in Verilog-A code will be described in detail.

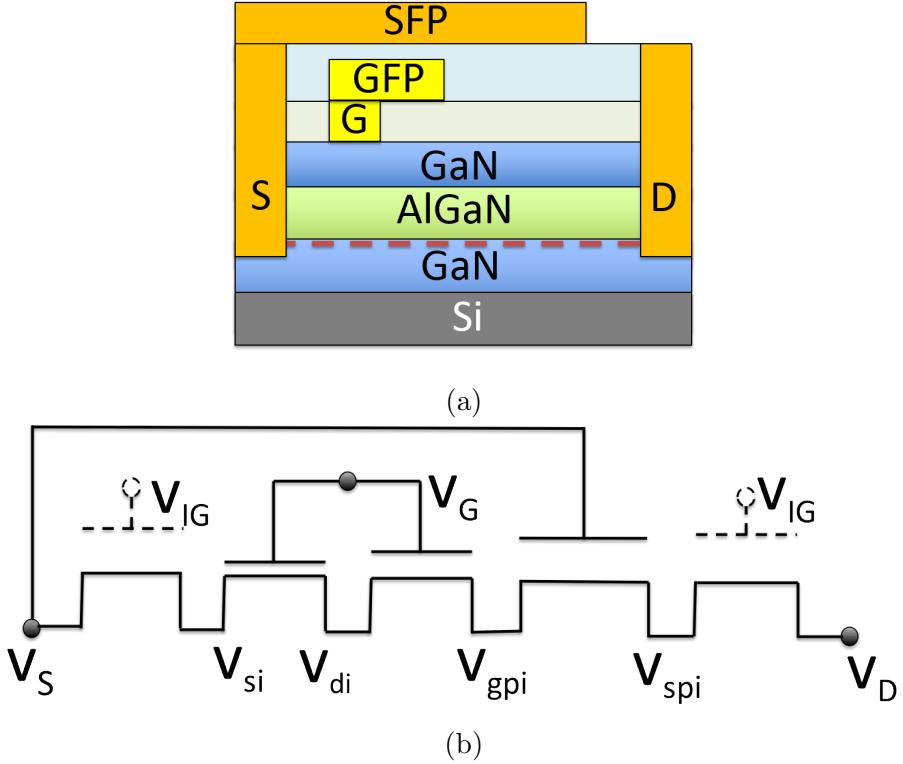


Figure 3: (a) Cross-sectional schematic of GaN HEMTs on Si. (b) The equivalent circuit for the model with intrinsic transistor, source-side gate-controlled-field-plate (GFP), drain-side source-controlled-field-plate (SFP) and implicit-gate access region transistors are shown.

The sub-circuit modeling approach shown above computes the voltage distribution in the device accurately under any bias condition and correctly captures depletion and other high voltage effects. The two field plate (FP) transistors, one as gate-controlled field plate (GFP) with its gate connected to the gate terminal and the other as source-controlled field plate (SFP) with its gate connected to the source terminal, have different threshold voltage (V_T) due to the dielectric used. The further the FP is from the gate edge, the more negative its V_T . This ensures that in the off-state, as V_{DS} is increased in the off-state, the field plates progressively deplete at different V_T , which prevents peak-fields from reaching the critical field and hence premature device breakdown.

4 Document Guidelines

In this manual, several formatting guidelines are followed in order to better aid the user in understanding the model. The first guideline is the use of voltage and current symbols.

- V_D, I_G : Uppercase represents a time-invariant DC bias
- v_d, i_g : Lowercase represents a time-varying signal
- v_D, i_G : Mixed case represents a total large signal where $v_D = V_D + v_d$
- V_t, I_{sat} : Mixed case (opposite) represents a physical parameter

The second guideline is the use of text styles to represent certain elements from the Verilog-A code.

- Node names (both extrinsic and intrinsic) are shown with a bold typeface such as **gi2p**
- Extrinsic parameters (model and instance values which can be modified by the user at the circuit level schematic) are shown by an italicized typeface such as *flagpgan*
- Internal variables (which cannot be directly modified by the user) are shown by a tele-type typeface such as **idshsat**
- Function names in the Verilog-A code are shown by a bold and italicized typeface such as ***calc_iq***

5 MVSG Model: Verilog-A Implementation

The following sections will first describe the MVSG model formulation and underlying physics, including the detailed Verilog-A implementation roughly in the order they appear in the Verilog-A code.

5.1 Terminal Voltage Definition

The first part of the Verilog-A implementation of the MVSG model involves the definition of terminal voltages for each sub-circuit element shown in Fig. 4.

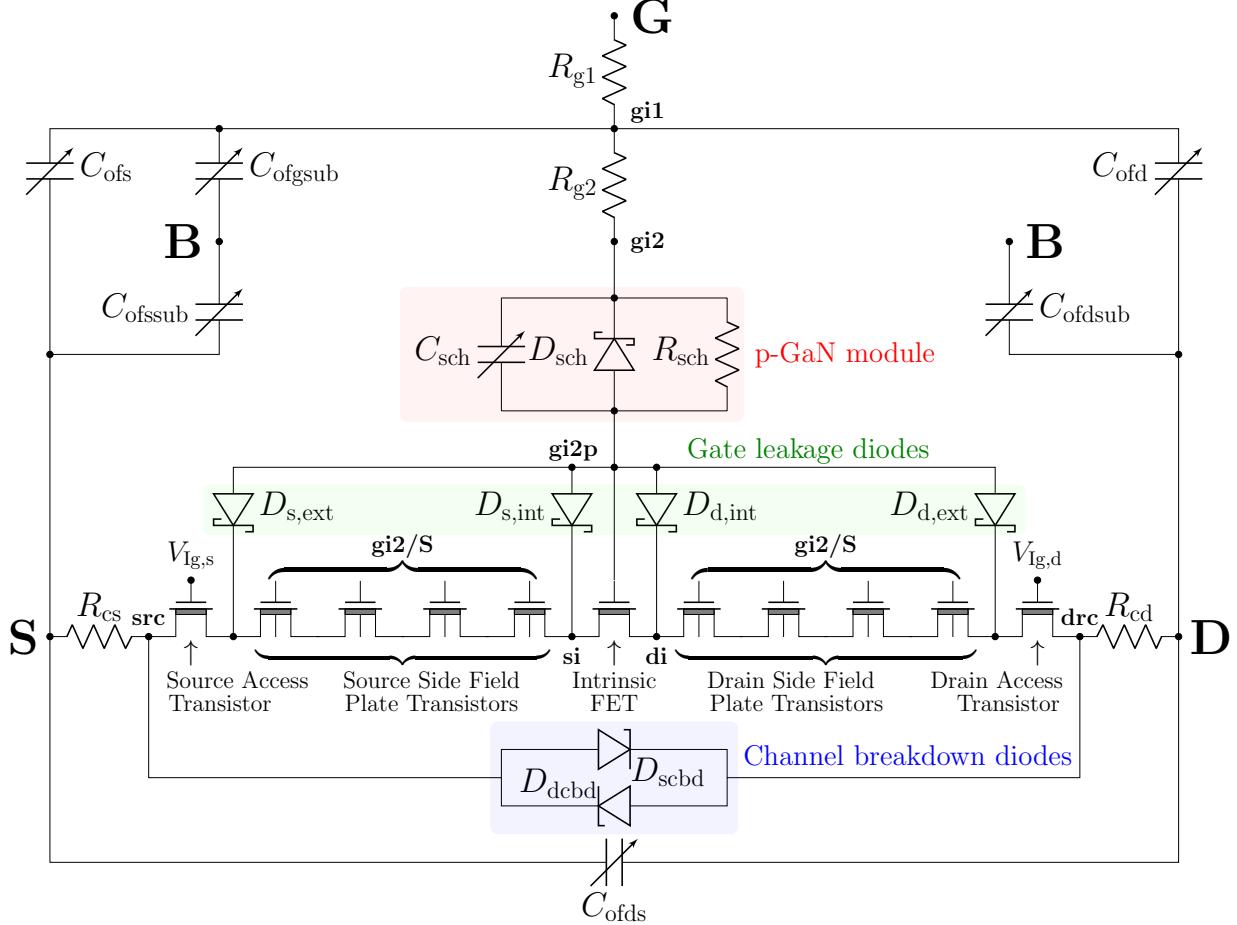


Figure 4: The equivalent circuit for the MVSG model showing all of the intrinsic and extrinsic nodes along with the intrinsic transistor, field plate region transistors, implicit-gate access region transistors, contact resistances (R_{cs} and R_{cd}), gate diodes, breakdown diodes, distributed gate resistance, p-GaN module elements, and bias-dependent fringing capacitances. The equivalent gate-source and gate-drain voltages of each transistor element is defined in the Verilog-A code. Thermal sub-circuit and trapping sub-circuits are not shown.

Fig. 4 shows the MVSG GaN HEMT schematic where external terminals are labeled as **D** (Drain), **G** (Gate), **S** (Source), and **B** (Body) (the thermal terminal in the equivalent circuit

schematic is part of the thermal sub-circuit and not part of the main schematic). Internal drain terminal of the intrinsic transistor is labeled as **di**, while internal source terminal is labeled as **si**. In addition, there are source and drain contact resistances which require additional intrinsic nodes: **src** and **drc**. **src** is the intrinsic source node of source-implicit-gate access transistor and **drc** is the intrinsic drain node of the drain-implicit-gate access transistor. To support the field plate (FP) transistors, from left to right, between **src** and **si**, unlabeled nodes are **fps4**, **fps3**, **fps2**, and **fps1**. Similarly, between **di** and **drc**, unlabeled nodes are **fp1**, **fp2**, **fp3**, and **fp4**. The model supports up to four FP transistors on each side of the intrinsic FET which are disabled by default (zero gate length). When a FP transistor is disabled, the source and drain nodes of that transistor are collapsed. See section 5.1.3 for how to activate and define their gate terminal voltages. The body of each FP transistor is charge coupled to the **B** (body) terminal and is represented by the body connection in the schematic.

5.1.1 Intrinsic Transistor

The intrinsic transistor voltage definition is done by the following lines, where **vdsi** and **vgsi** are the drain-source and gate-source voltages respectively.

```

1 // Determine drain-source and gate-source voltage for intrinsic transistor
2 vdsi = type * V(di , si );
3 vgsi = type * V(gi2p , si );
```

5.1.2 Source and Drain Implicit-Gate Access Transistors

The source and drain access regions do not have an actual gate terminal. The implicit gate terminal (denoted by $V_{ig,\{s/d\}}$ in Fig. 4) is non-existent and is only linked to the sheet resistance (rsh) and carrier mobility (μ_0) in these regions through an additional fitting parameter ($cgrs$ and $cgrd$). More details can be found in [2]. The terminal voltages for these implicit-transistors are defined in a way similar to that of the intrinsic transistor (**vdsr{s/d}** is the drain-source and **vgsr{s/d}** is the gate-source voltage) region as shown below. Note that for the drain implicit-gate transistor, an additional variable **drsht** is present to model charge trapping using the older module (*trapselect=1*). (see Section 5.7.1)

Source Implicit-Gate Access Transistor

```

1 // Determine drain-source and gate-source voltage for SAR transistor
2 if (flaggum == 0) begin
3     if (type * V(src , d) <= type * V(src , s)) begin
4         vsars = type * V(src , s);
5     end else begin
6         vsars = type * V(src , d);
7     end
8 end else begin
9     vsars = mmax(type * V(src , d) , type * V(src , s) , mmaxs);
10 end
11 vigs = vtors + 1.0 / (rsh * cgrs * mu0);
12 vdsrs = type * V(fps4 , src );
13 vgsrs = (vigs - vsars);
```

Drain Implicit-Gate Access Transistor

```

1 // Determine drain-source and gate-source voltage for DAR transistor
2 if (flaggum == 0) begin
3     if (type * V(fp4, d) <= type * V(fp4, s)) begin
4         vdars = type * V(fp4, s);
5     end else begin
6         vdars = type * V(fp4, d);
7     end
8 end else begin
9     vdars = mmax(type * V(fp4, d), type * V(fp4, s), mmaxs);
10 end
11 vigd = vtord + 1.0 / (drsht * rsh * cgrd * mu0);
12 vdsrd = type * V(drc, fp4);
13 vgsrd = (vigd - vdars);

```

When performing Gummel symmetry tests, it is best to set *flaggum*=1 to avoid discontinuities in the derivatives of *vsars* caused by the abrupt switching in the if-statement. When *flaggum*=1, the transition is smoothed using *mmax*. The comparison between *flaggum*=0 and *flaggum*=1 for the access regions can be seen in Fig. 5 up to the 5th derivative, where the IV curves with *flaggum*=1 have no discontinuities.

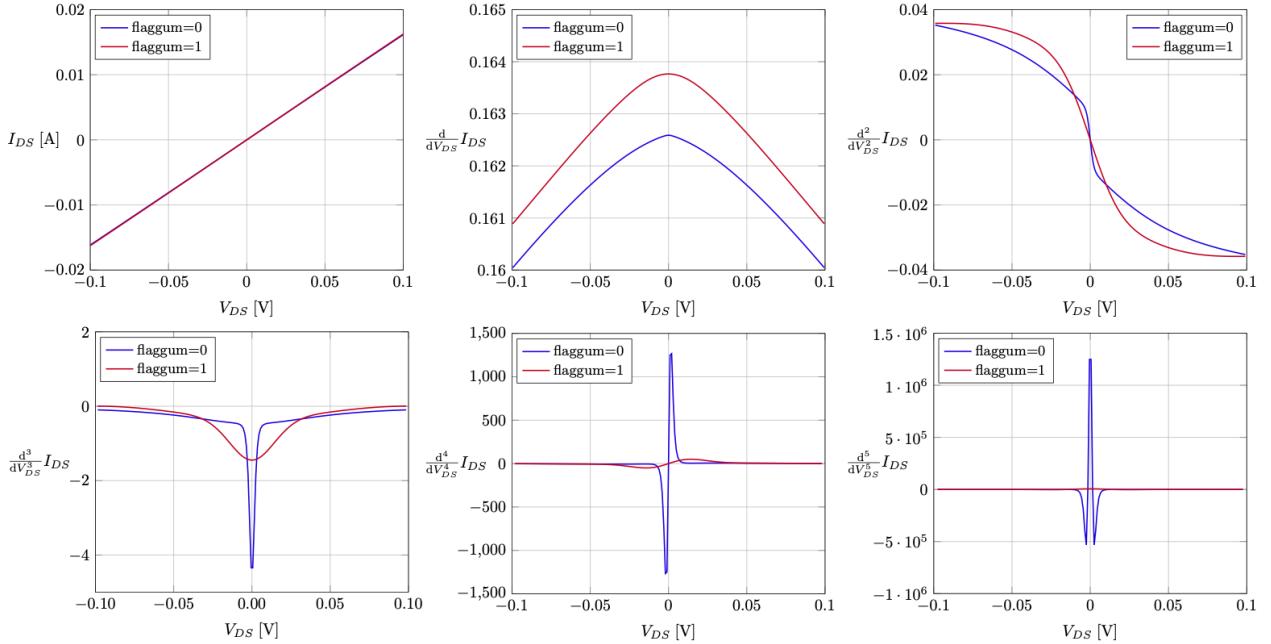


Figure 5: Derivatives of I-V plots for the SAR transistor with *flaggum*=0 and *flaggum*=1.

5.1.3 Field Plate Transistors

The field plate transistors are similar to the intrinsic FET and up to four are located on either side of the intrinsic FET. Each FP can be activated by using a non-zero gate length (more accurately, by setting it to be larger than the minimum length parameter *minl*). The gate of each FP can also be connected to either the **S** or **gi2** node with the *flagfp{*s1,s2,s3,s4,1,2,3,4*}* parameter under each FP parameter group. For example, setting

$flagfps1=1$ and $lgfps1 > minl$ activates a source-side GFP between **fps1** and **si**. A common mistake among users is thinking that the $flagfp\{s1,s2,s3,s4,1,2,3,4\}$ parameter turns the field plate on or off, which is not the case. This parameter controls if the gate terminal of the field plate is connected to **S** (set to 0) or **gi2** (set to 1). Unlike most modules (but similar to the access regions), the FPs are turned on by setting $lgfp\{s1,s2,s3,s4,1,2,3,4\}$ to be greater than (but not equal to) $minl$. If the length is set to $minl$ or smaller, then the source and drain nodes of the FP will be collapsed. A few examples are shown below.

- $lgfp1 = 0$: The (drain-side) field plate 1 is turned off, **di** & **fp1** are collapsed.
- $lgfps2 = minl$: The source-side field plate 2 is turned off, **fps2** & **fps1** are collapsed.
- $lgfp3 > minl \& flagfp3 = 0$: The (drain-side) field plate 3 is turned on and placed between **fp2** & **fp3** with the gate being connected to **S**.
- $lgfps4 > minl \& flagfps4 = 1$: The source-side field plate 4 is turned on and placed between **fps4** & **fps3** with the gate being connected to **gi2**.

Unlike the intrinsic FET, the FP transistors contain a charge coupled connection to **B** and additional parameters can be set to control cross coupled voltages. The voltage definition for the source-side FP1 (SFP1) is shown below. The other seven FPs are defined similarly.

```

1 // Determine gate-source , drain-source voltage and cross-coupled voltages for
2 if (flagfps1 == 1) begin
3   vgsfps1 = type * V(gi2 ,fps1 );
4   vcfps1 = type * V(s ,fps1 );
5 end else begin
6   vgsfps1 = type * V(s ,fps1 );
7   vcfps1 = type * V(gi2 ,fps1 );
8 end
9 vdsfps1 = type * V(si ,fps1 );
10 vbfps1 = type * V(b ,fps1 );

```

The field plates cause a shift in CV plots at the threshold voltage of each FP as shown in Fig. 6. This is due to each FP successively turning on as the channel depletes.

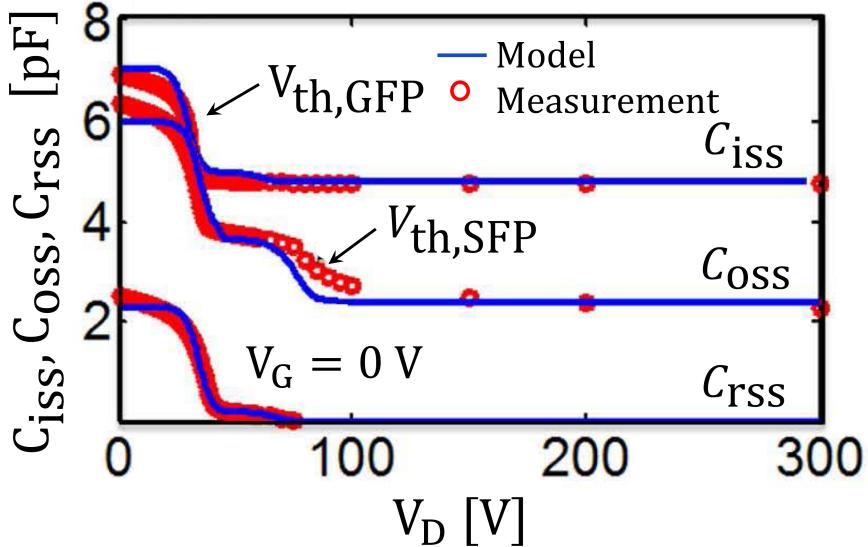


Figure 6: Two drain-side FPs are activated, with one gate connected (GFP) and one source connected (SFP). As the channel depletes, a shift in CV is shown at the threshold voltage of each FP.

5.1.4 Contact Resistances

The contact resistances (R_{cs} and R_{cd} in Fig. 4) are set through unit width parameters rcs and rcd [$\Omega \cdot m$]. By default, the contact resistances are only calculated from these parameters. However, if the parameter *flagres=1* is set, then the access region transistors are modeled as resistors, and their resistance is tagged onto the contact resistances for computation purposes. The computation is shown in the following code.

```

1 if (flagres==0) begin
2   rcs_w = rcs / w / ngf;
3   rcd_w = rcd / w / ngf;
4 end else begin
5   rcs_w = ( rcs / w + rsh * lgs / w ) / ngf;
6   rcd_w = ( rcd / w + rsh * lgd / w ) / ngf;
7 end

```

After rcs_w and rcd_w are obtained, they are temperature modulated as will be explained in Section 5.2, which will return rsi and rdi . Finally, the terminal voltages of these resistances are defined as seen in Fig. 4 through the following code.

```

1 if ((rcd_w >= minr) && (rcd_w > 0)) begin
2   I(d,drc) <+ V(d,drc) / rdi;
3 end else begin
4   V(d,drc) <+ 0;
5 end
6 if ((rcs_w >= minr) && (rcs_w > 0)) begin
7   I(src,s) <+ V(src,s) / rsi;
8 end else begin
9   V(src,s) <+ 0;
10 end

```

5.1.5 Other Elements

The terminal voltage definition for the bias-dependent fringing field capacitances (5.4.4), gate-diodes (5.5), p-GaN module elements (5.6), breakdown diodes (5.10), and distributed gate resistance (5.11) are defined where they are implemented in the code and will be explained in their respective sections. Modules not part of the equivalent circuit schematic in Fig. 4, including thermal self heating (5.2.1) and charge trapping (5.7) sub-circuits will also be explained in their respective sections.

5.2 Temperature Dependence

GaN HEMTs have high power dissipation due to high current densities (few A/mm) and poor thermal conductivity of the Si substrate in many cases. Therefore GaN compact models must incorporate temperature dependence on carrier transport parameters such as mobility and carrier velocity.

Three methods of device temperature deviation from ambient are available. The first is through the parameter *dtemp* which adds a fixed temperature offset from ambient. The second (5.2.1) is through self-heating which is captured in the model by employing a thermal node (**dt**) and a thermal sub-circuit. The third (5.2.2) is through the external **dt** node which is optionally connected to a current source (where power in W is represented by the current in A) in the circuit level schematic, to account for thermal coupling from adjacent environment.

The temperature modulated mobility (**muf**), velocity (**vx**), threshold voltage (**vt0f**), contact resistance (**rsi** and **rdi**) and subthreshold slope (**ss**, through **phit**) are captured by the following equations.

```

1 // Temperature dependence of voltage independent terms
2 gmin = $simparam("gmin",0);
3 tnomk = tnom + 'P_CELSIUS0;
4 tambk = $temperature;
5
6 // Make external thermal node dt optional
7 if ($port_connected(dt) == 0);
8
9 tsh = Temp(dt);
10 tdut = tambk + dtemp + tsh;
11 if (tdut < 'T_MIN + 'P_CELSIUS0) begin
12     tdut = 'T_MIN + 'P_CELSIUS0;
13 end else begin
14     if (tdut > 'T_MAX + 'P_CELSIUS0) begin
15         tdut = 'T_MAX + 'P_CELSIUS0;
16     end
17 end
18
19 rsi = 0;
20 rdi = 0;
21 if (flagres==0) begin
22     rcs_w = rcs / w / ngf;
23     rcd_w = rcd / w / ngf;
24 end else begin
25     rcs_w = ( rcs / w + rsh * lgs / w ) / ngf;

```

```

26     rcd_w = ( rcd / w + rsh * lgd / w ) / ngf;
27 end
28 if ((rcs_w >= minr) && (rcs_w > 0)) begin
29     rsi = ( rcs_w ) * ( 1.0 + rct1 * ( tdut - tnomk ) + rct2 * ( tdut -
30         tnomk ) * ( tdut - tnomk ) );
31     if ( rsi < 0.1 * rcs_w) begin
32         rsi = 0.1 * rcs_w;
33     end
34 end else begin
35     rsi           = 0;
36 end
37 if ((rcd_w >= minr) && (rcd_w > 0)) begin
38     rdi = ( rcd_w ) * ( 1.0 + rct1 * ( tdut - tnomk ) + rct2 * ( tdut -
39         tnomk ) * ( tdut - tnomk ) );
40     if ( rdi < 0.1 * rcd_w) begin
41         rdi = 0.1 * rcd_w;
42     end
43 end else begin
44     rdi = 0;
45 end
46 rg1 = ( rgsp / ngf / ngcon ) * ( lovg + agate * w / ngcon );
47 rg2 = ( rgsp / ngf / ngcon ) * ( (1.0 - agate) * w / ngcon );
48
49 // Tempcos on key transport and charge parameters
50 phit = 'P_KK * tdut / 'P_QQ;
51 ttrapfac = 1.0 + tempt * ( tdut - tnomk );
52 if (ttrapfac < 0.1) begin
53     ttrapfac = 0.1;
54 end
55 tfacdiode = pow( ( tdut / tnomk ) , 3.0 );
56
57 // The following lines are within the calc_iq function
58 tfacmobin = pow(( tambin / tnomin ), epsilon );
59 muf = mu0 / ( tfacmobin * ( 1.0 + mtheta * qinvv / cgin ) );
60 vx = vel0 * ( ( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin ) );
61 vtof = vto + vtzeta * ( tambin - tnomin );

```

The temperature rise can also impact the channel-charges, fringing-capacitances (both bias-dependent and -independent components), and FP-charges. These temperature effects are captured in terms of (a) the linear- and quadratic- dependence of these capacitance values and (b) threshold voltage (vto) dependence on temperature. A separate function call is made to calculate the temperature-dependent charge-terms using input temperature coefficients as shown below.

```

1 analog function real calc_capt;
2   input capin , tempcoin , tdutin , tnomkin ;
3   // IO
4   real capin , tempcoin , tdutin , tnomkin ;
5   // Local
6   real tcapfac ;
7
8 begin
9   tcapfac      = 1.0 + tempcoin * ( tdutin - tnomkin );
10  if (tcapfac < 0.01) begin
11    tcapfac     = 0.01;
12  end
13  calc_capt    = capin * tcapfac ;
14 end
15 endfunction

```

5.2.1 Self Heating Thermal Sub Circuit

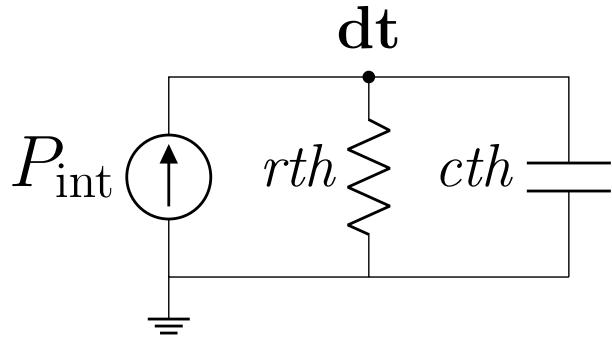


Figure 7: The thermal subcircuit in the model used to compute the temperature increase due to internal power dissipation.

The power dissipation (pdiss) in the device is captured as the sum of the product of voltage drop and current in each region of the device. pdiss (in W, calculated internally in the model) is passed to P_{int} (in A), which is the current source in Fig. 7. The temperature rise in the device from self-heating is captured using the RC network (rth and cth) connected to the thermal node as shown. Currently, the thermal network parameters are not scaled according to device size. The value of dt (in V) is used as tsh (self heating temperature change, in K) which is ultimately used to determine the device temperature (tdut) shown previously in 5.2.

5.2.2 External Thermal Node

The ability to model temperature rise due to adjacent heat sources is also incorporated in the model through an extension to the thermal sub-circuit. Temperature rise due to external factors is done at the netlist level by injecting current into the dt node shown in Fig. 8.

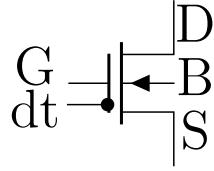


Figure 8: MVSG Symbol with additional optional thermal terminal (**dt**) for connecting external heat sources.

The elements inside the dashed box in Fig. 9 shows the thermal subcircuit for self heating as explained in Section 5.2.1. The external thermal node is represented by the terminals near the left edge of the dashed box where an external heat source (represented by P_{ext}) is optionally connected.

As the **dt** node is directly accessible at the netlist level, connecting a voltage source to **dt** will fix the temperature increase due to self heating (temperature rise in K will be set to the voltage in V) which is not entirely physical, and thus not recommended. To represent power flow (in W) into the device, a current source should be connected to **dt** (with the current in A set to the desired power in W). Device cooling can also be modeled by pulling current out of **dt**.

If self heating is turned off ($rth=0$), a non zero P_{ext} should not be connected, as **dt** is shorted to 0K through $rth=0$, which will conflict with a non-zero P_{ext} source.

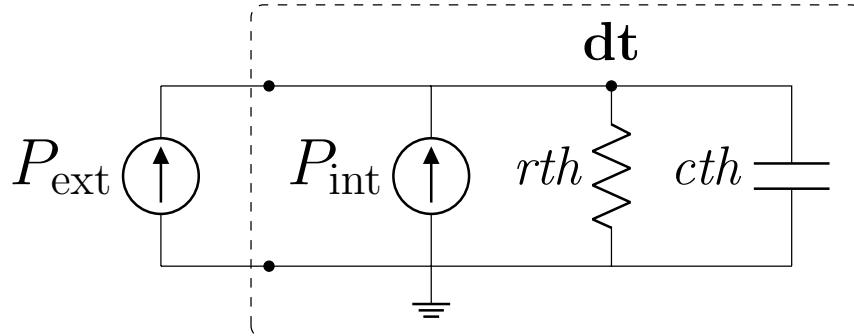


Figure 9: The thermal subcircuit in the model used to compute the temperature increase due to internal and external power dissipation. The elements inside the dashed box are built into the MVSG model. This is the augmented thermal sub circuit of Fig. 7, used if **dt** is connected at the circuit level schematic.

Some examples of different P_{ext} applied to the **dt** node are shown in Fig. 10 showing that the model is very versatile in external thermal influence.

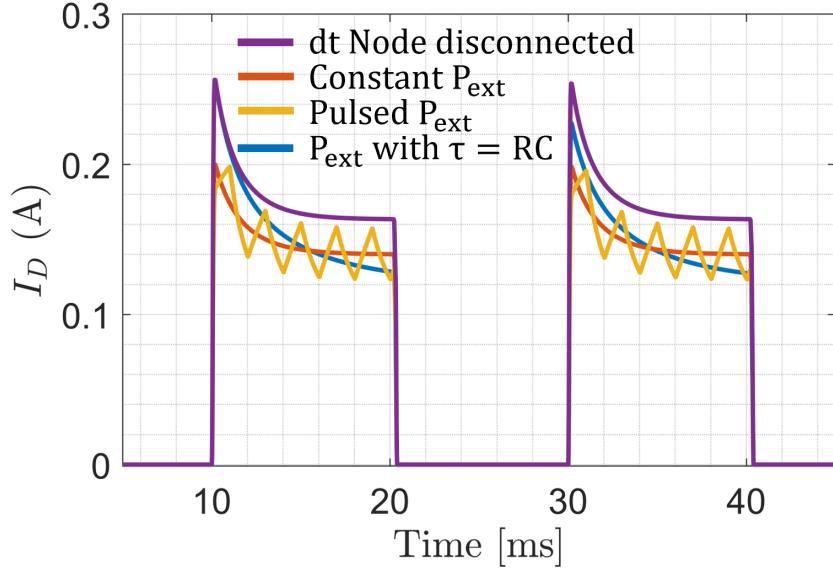


Figure 10: Some examples of various P_{ext} connected to **dt**. Internal self heating is on for all curves.

The implementation of thermal effects including self-heating (5.2.1) and optional thermal coupling from the external thermal node (5.2.2) is in the following code.

```

1 // power-dissipation calculations
2 pdiss = ( ids * V(di , si) + idsrd * V(drc , fp4) + idsrs * V(fps4 , src) + idsfps4
   * V(fps3 , fps4) + idsfps3 * V(fps2 , fps3) + idsfps2 * V(fps1 , fps2) + idsfps1
   * V(si , fps1) + idsfp1 * V(fp1 , di) + idsfp2 * V(fp2 , fp1) + idsfp3 * V(fp3 ,
   fp2) + idsfp4 * V(fp4 , fp3) );
3 if ((rcd_w >= minr) && (rcd_w > 0)) begin
4   pdiss = pdiss + ( V(drc , d) * V(drc , d) / rdi );
5 end
6 if ((rcs_w >= minr) && (rcs_w > 0)) begin
7   pdiss = pdiss + ( V(src , s) * V(src , s) / rsi );
8 end
9 // Self-heating
10 if (rth >0) begin
11   Pwr(dt) <+ ddt( cth * Temp(dt));
12   Pwr(dt) <+ - pdiss;
13   Pwr(dt) <+ Temp(dt) / rth;
14 end else begin
15   Temp(dt) <+ 0.0;
16 end

```

5.3 Transistor Drain Current Formulation

In the MVSG model, the intrinsic, access, and FP regions are assumed to be long enough (compared to electron mean free path in GaN) so that carrier transport is drift-diffusion (DD) based. Therefore, the implicit-gate model for these regions are essentially non-ballistic-

channel transistor models which are suitable for typical channel lengths longer than ~ 50 nm. The model equations described below are generic in nature and are applicable to each transistor region of the HEMT with their own parameters. For the implicit-gate transistors, gate overdrive voltage is linked to the sheet resistance as given in [4] and defined in section 5.1.2. The rest of the formulation is that of a conventional mobility-limited / saturation velocity-limited transport FET model. The DD channel model equations employed in MVSG model for these regions assume the band profile as shown in Fig. 11.

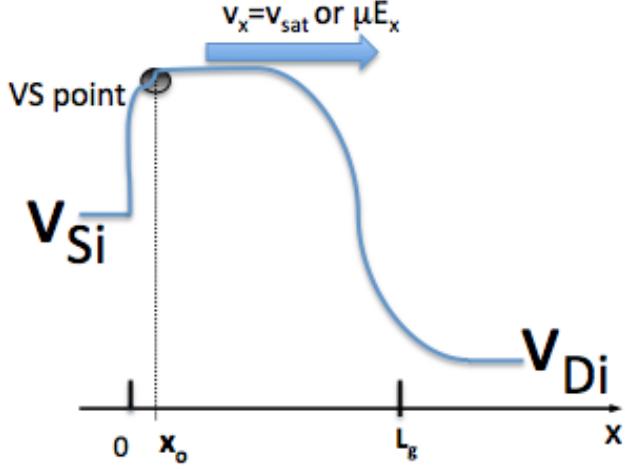


Figure 11: Conduction band profile assumed in DD channel transistor model under drain bias.

The current is given by the product of charge and velocity at the virtual source (VS) point (for that matter at any point in the channel, current is the product of local charge and velocity), but while the charge at the VS point is still the same as given by (2) in [5], the velocity at the VS point is no longer a simple, constant bias-independent quantity as in ballistic HEMTs. In long channels, transport is governed by drift/diffusion (DD) and the carrier velocity at any point in the channel is dependent on the local field as $v_x = \mu_{\text{eff}} E_x$. The current is evaluated using the following procedure.

The master equation for drift current is given by

$$\frac{I_D}{W} = Q_{ix} v_x = Q_{ix} \mu_{\text{eff}} E_x = Q_{ix} \mu_{\text{eff}} \frac{d\psi}{dx} \quad (1)$$

Here, ψ is the potential at location x . For the charge-based simplified all-region model, the channel layer charge is expressed as given in [6] and

$$\frac{dQ_{ix}}{d\psi} = C_{\text{inv}} \quad (2)$$

Using Caughey and Thomas model [7] for carrier velocity dependence on field, the effective mobility is given by

$$\mu_{\text{eff}} = \frac{\mu}{\left(1 + \left(\frac{\frac{d\psi}{dx}}{L_g \frac{v}{\mu}}\right)^\beta\right)^{\frac{1}{\beta}}} \quad (3)$$

This formulation assumes that the carrier velocity profile with field is similar to that of Si (i.e. carrier velocity increases with field and saturates at saturation velocity). It takes the form of drift velocity in strong accumulation and diffusion velocity in weak accumulation. In addition, in strong accumulation the velocity v includes GaN specific effects such as self-heating and scattering whose functions are multiplied to bias-independent saturation velocity (v_{sat0}). Using (2-3), (1) can be rewritten as

$$\frac{I_D}{W} = Q_{ix} \frac{\mu}{\left(1 + \left(\frac{\frac{dQ_{ix}}{dx}}{C_{\text{inv}} L_g \frac{v}{\mu}}\right)^\beta\right)^{\frac{1}{\beta}}} C_{\text{inv}} \frac{\frac{dQ_{ix}}{dx}}{C_{\text{inv}} L_g \frac{v}{\mu}} \quad (4)$$

Using current continuity and assuming $\frac{dQ_{ix}}{dx} = \frac{Q_{is} - Q_{id}}{L_g}$ in the denominator of (4), we can integrate the above expression from $x = 0$ to $x = L_G$ and from $Q_{ix} = Q_{is}$ to $Q_{ix} = Q_{id}$. The resulting current is given by

$$\frac{I_D}{W} = \frac{\mu}{2C_{\text{inv}} L_g} \frac{Q_{is}^2 - Q_{id}^2}{\left(1 + \left(\frac{Q_{is} - Q_{id}}{C_{\text{inv}} L_g \frac{v}{\mu}}\right)^\beta\right)^{\frac{1}{\beta}}} \quad (5)$$

Here, v is the carrier velocity combining strong and weak accumulation regimes, as discussed below. In order to make the current expression look similar to that of VS model expression in (4) in [5], the previous expression (5) can be reformulated as follows

$$\frac{I_D}{W} = v \frac{1}{2C_{\text{inv}} V_{\text{DSAT}}} \frac{Q_{is}^2 - Q_{id}^2}{\left(1 + \left(\frac{Q_{is} - Q_{id}}{C_{\text{inv}} V_{\text{DSAT}}}\right)^\beta\right)^{\frac{1}{\beta}}} = v \frac{Q_{is} + Q_{id}}{2} F_{\text{vsat}} \quad (6)$$

Where $F_{\text{vsat}} = \frac{\frac{Q_{is} - Q_{id}}{C_{\text{inv}} V_{\text{DSAT}}}}{\left(1 + \left(\frac{Q_{is} - Q_{id}}{C_{\text{inv}} V_{\text{DSAT}}}\right)^\beta\right)^{\frac{1}{\beta}}}$ and V_{DSAT} is similar to that in (5) from [5]. V_{DSAT} must account for both strong and weak accumulation regimes and so should v . To do this we follow a similar procedure as in (5) in [5] and is shown below.

$$V_{\text{DSAT}} = V_{\text{DSATS}} (1 - F_f) + 2n\varphi_t F_f \quad ; \quad \text{where } V_{\text{DSATS}} = \frac{v_{\text{sat}} L_g}{\mu} \quad (7a)$$

$$v = v_{\text{sat}} (1 - F_f) + 2\varphi_t \frac{\mu}{L_g} F_f \quad (7b)$$

v_{sat} is what we call the GaN ‘‘saturation velocity’’ which is similar to the saturation velocity in Si.

In the long channel limit, where transport is mobility limited, i.e. non-velocity saturation (NVsat), $V_{\text{DSAT}} \gg \frac{Q_{is} - Q_{id}}{C_{\text{inv}}}$ which means $F_{\text{vsat}} = \frac{Q_{is} - Q_{id}}{C_{\text{inv}} V_{\text{DSAT}}}$ and (6) reduces to

$$\frac{I_D}{W} = v \frac{Q_{is}^2 - Q_{id}^2}{2C_{\text{inv}} V_{\text{DSAT}}} \quad (8)$$

(8) has a form very similar to the EKV model used for long channel MOSFETs.

In shorter channel velocity saturation (Vsat) limit, $V_{\text{DSAT}} \ll \frac{Q_{is} - Q_{id}}{C_{\text{inv}}}$ and $F_{\text{vsat}} = 1$ which reduces 6 into a simple current expression

$$\frac{I_D}{W} = v \frac{Q_{is} + Q_{id}}{2} \quad (9)$$

This expression for current is of the same form as VS model expression of (4) in [5] except that the charge here is the average of source-end and drain-end charges while in the original VS Model it is just the charge at the VS point. The expression for charges at the source-end and drain-end is similar to that in (2) in [5] and are given by (10a, 10b)

$$Q_{is} = 2C_{\text{inv}} n \varphi_t \ln \left(1 + \exp \frac{V_{\text{GDi}} - V_{sx} - (V_T - (\text{flagsp})\alpha \varphi_t F_f)}{2n\varphi_t} \right) \quad (10a)$$

$$Q_{id} = 2C_{\text{inv}} n \varphi_t \ln \left(1 + \exp \frac{V_{\text{GSi}} - V_{dx} - (V_T - (\text{flagsp})\alpha \varphi_t F_f)}{2n\varphi_t} \right) \quad (10b)$$

Note that the charge-terms have a shift in their threshold voltage between strong-to-weak accumulation governed by $(\text{flagsp})\alpha \varphi_t F_f$. While the effect mimics surface-potential change with V_G in Si-devices and is kept here for backward compatibility, it is in general not relevant for GaN-devices (which have zero body-bias). So, this term is turned-off by default in the model by setting $\text{flagsp}=0$ and can be turned-on by setting $\text{flagsp}=1$. Further, the term α governs smoothness of transition from strong-to-weak accumulation. It is recommended to scale the value of α with the corresponding value of n for each transistor element of the model. Typically, $n \sim 1$ for $ss = 60 \text{ mV/dec}$ and $\alpha = 3.5$. However, for field-plate regions in GaN HEMTs, ss would reach few 10s of V/dec in some cases, and $n \sim 10 - 100$. Such ss would require α to be scaled to 35-350 accordingly for better computational smoothness. Here, complete S/D symmetry is achieved using the above charge formulation. The terms V_{sx} and V_{dx} are in turn required to include velocity-saturation effects that will be explained in the next section and are given here:

$$V_{sx} = \frac{-V_{\text{DSi}}}{\left(1 + \left(-\frac{V_{\text{DSi}}}{V_{\text{DSAT}}} \right)^{\beta} \right)^{\frac{1}{\beta}}} ; \quad V_{dx} = \frac{V_{\text{DSi}}}{\left(1 + \left(\frac{V_{\text{DSi}}}{V_{\text{DSAT}}} \right)^{\beta} \right)^{\frac{1}{\beta}}} \quad (11)$$

The charge expressions above are needed to model the subthreshold regime accurately. In the subthreshold regime the above expressions are reduced to

$$Q_{is} = 2C_{\text{inv}} n \varphi_t \exp \frac{V_{\text{GSi}} - (V_T - (\text{flagsp})\alpha \varphi_t)}{2n\varphi_t} \quad (12a)$$

$$Q_{id} = 2C_{\text{inv}} n \varphi_t \exp \frac{V_{\text{GDi}} - (V_T - (\text{flagsp})\alpha \varphi_t)}{2n\varphi_t} \quad (12b)$$

Substituting (7a), (7b) and (12) in (8), the current I_D in subthreshold regime, where diffusion current dominates, is

$$\begin{aligned} \frac{I_D}{W} &= v \frac{1}{2C_{\text{inv}}V_{\text{DSAT}}} \left(\frac{\left(2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GSi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{2n\varphi_t}\right)^2 - \left(2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GDi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{2n\varphi_t}\right)^2}{1 + \left(\frac{2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GSi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{2n\varphi_t} - 2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GDi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{2n\varphi_t}}{C_{\text{inv}}V_{\text{DSAT}}}\right)^{\frac{1}{\beta}}}\right) \\ &\approx 2\varphi_t \frac{\mu}{L_g} \frac{(2C_{\text{inv}}n\varphi_t)^2}{2C_{\text{inv}}2n\varphi_t} \left(\exp \frac{V_{\text{GSi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{n\varphi_t} - \exp \frac{V_{\text{GDi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{n\varphi_t} \right) \\ \frac{I_D}{W} &= \varphi_t \frac{\mu}{L_g} \left(2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GSi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{n\varphi_t} - 2C_{\text{inv}}n\varphi_t \exp \frac{V_{\text{GDi}} - (V_T - (\text{flagsp})\alpha\varphi_t)}{n\varphi_t} \right) \quad (13) \end{aligned}$$

This is similar to the well-known sub threshold MOSFET diffusion current.

5.3.1 Transition From Non-Saturation to Saturation Current

In order to facilitate smooth transition from linear to saturation regimes under applied V_{DS} we use similar function F_{sat} as in (4) in [5]. The charge expression at the source- and drain- ends is modified with V_{DS} as

$$Q_{i\{s/d\}} = 2C_{\text{inv}}n\varphi_t \ln \left(1 + \exp \frac{V_{G\{d/s\}i} \{-/+ \} V_{\text{DSAT}} F_{\text{sat}} - (V_T - (\text{flagsp})\alpha\varphi_t F_f)}{2n\varphi_t} \right) \quad (14)$$

Where $V_{\text{DSAT}} F_{\text{sat}}$ is given by

$$V_{\text{DSAT}} F_{\text{sat}} = V_{\text{DSAT}} \frac{\frac{V_{\text{DSi}}}{V_{\text{DSAT}}}}{\left(1 + \left(\frac{V_{\text{DSi}}}{V_{\text{DSAT}}}\right)^{\beta}\right)^{\frac{1}{\beta}}} = \frac{V_{\text{DSi}}}{\left(1 + \left(\frac{V_{\text{DSi}}}{V_{\text{DSAT}}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \quad (15)$$

Here V_{DSAT} is as given in (7a) and $V_{\text{DSi}} = V_{D_i} - V_{S_i}$ is the intrinsic drain to source voltage. In the linear regime (at low V_{DSi}), $V_{\text{DSAT}} F_{\text{sat}}$ approaches V_{DSi} and Q_{id} in (14) becomes comparable to Q_{is} . Thus, the current formulation of (5) reduces to

$$\frac{I_D}{W} = \frac{\mu}{2C_{\text{inv}}L_g} \frac{Q_{is}^2 - Q_{id}^2}{\left(1 + \left(\frac{Q_{is} - Q_{id}}{C_{\text{inv}}V_{\text{DSAT}}}\right)^{\beta}\right)^{\frac{1}{\beta}}} = \frac{\mu}{2C_{\text{inv}}L_g} (Q_{is}^2 - Q_{id}^2) \approx \frac{\mu Q_{is}}{C_{\text{inv}}L_g} (Q_{is} - Q_{id}) \quad (16)$$

Irrespective of V_{DSAT} , the denominator of the first expression in (16) tends to 1 as $Q_{is} - Q_{id} \ll C_{\text{inv}}V_{\text{DSAT}}$. Thus, transport regime (NVsat or Vsat) has no bearing on current in linear regime. More details of this model can be found in [2].

5.3.2 GaN Specific Effects

In GaN HEMTs, electron velocity decreases as charge density increases due to strong electron-optical phonon interaction (scattering) and this is modeled empirically using Q_{ixo} . Including this and the temperature dependence due to self-heating, v_{xo} is modeled as [4], [8]

$$v_{xo} = \frac{v_{\text{inj}}}{\left(1 + \theta_v \frac{Q_{\text{ixo}}}{C_{\text{inv}}}\right)} (1 - \eta_v I_D V_D) \quad (17)$$

where v_{inj} is the bias independent injection velocity at low channel charge. The term in the denominator accounts for carrier scattering and the last term in the numerator accounts for velocity reduction due to self-heating. θ_v and η_v are fitting parameters. Carrier mobility also decreases due to scattering and self-heating and is modeled as [8], [9]:

$$\mu = \frac{\mu_0}{\left(1 + \theta_\mu \frac{Q_{\text{ixo}}}{C_{\text{inv}}}\right) \left(1 + \frac{\eta_\mu I_D V_D}{T_o}\right)^\varepsilon} \quad (18)$$

Here θ_μ , η_μ and ε are fitting parameters and T_o is reference temperature. The detailed procedure for the extraction of these parameters is provided at the end of this manual. Section 5.3.3 shows the Verilog-A file implementation of the core-equations of the transistor drain current described in this section.

5.3.3 Analog Function: `calc_iq` (Current Formulation)

The above-mentioned drain current model formulation is implemented using a function call of `calc_iq`. Note that `calc_iq` is repeatedly used for calculating channel current and charge of the intrinsic transistor, field-plate transistors, and access-region implicit gate transistors. The current-related Verilog-A codes are as below. The details of the charge-related part is explained in 5.4

Function I/O definition

```
1 analog function real calc_iq;
2   output idsout ,qgsout ,qgdout ,qcout ,qbout ,qsout ,vtdibl ,vdsat1 ;
3   input vgsin ,vdsin ,qcbflag ,vcin ,vbin ,qgsflag ,tamin ,tnomin ,phitin ,w,lin ,
4     cgin ,cs ,cc ,cb ,vto ,ss ;
5   input delta1 ,delta2 ,nd ,alpha ,vel0 ,mu0 ,beta ,mtheta ,vtheta ;
6   input vtzeta ,dibsat ,epsilon ,vzeta ,lambda ,ngf ,type , trapfracdl ;
7
8 // IO
9   real  idsout ,qgsout ,qgdout ,qcout ,qbout ,qsout ,vtdibl ,vdsat1 ,vgsin ,vdsin ,
10    qcbflag ,vcin ,vbin ,qgsflag ;
11   real  tambin ,tnomin ,phitin ,w,lin ,cgin ,cs ,cc ,cb ,vto ,ss ,delta1 ,delta2 ,nd ,
12    alpha ,vel0 ,mu0 ,beta ,mtheta ,vtheta ;
13   real  vtzeta ,dibsat ,epsilon ,vzeta ,lambda ,ngf ,type , trapfracdl ;
14
15 // Local
16   real  alpha_phit , delta , n , vtof , vsatdibl , ffs , two_n_phit , qref , etas ,
17     qinvs , muf , vx , vxf ;
18   real  n0 , ffs0 , two_n_phit0 , qref0 , etas0 , qinvs0 , muf0 , vx0 , tfacmobin ;
19   real  ff , eta , qinvv ;
20   real  ff0 , eta0 , qinvv0 ;
21   real  vdsats , vdsats1 , vdsat , fsd , vdx , fds , vsx , ffd , etad , qinvd , vdsc ,
22     fsat , vel ;
23   real  vdsats0 , vdsats10 , vdsat10 , fsd0 , vdx0 , fds0 , vsx0 , ffd0 , etad0 ,
24     qinvd0 ;
25   real  qs2 , qs3 , qd2 , qd3 , qsqd , qinvdd , qd1 , qs , qd , etac , etab , etags ;
26   real  exparg , myarg , absvdsin , vgdin ;
27   real  exparg0 , myarg0 ;
```

Current formulation

```

1 begin
2     absvdsin      = absfunc( vdsin , mmaxs );
3     vgdin         = vgsin - vdsin ;
4     alpha_phit    = alpha * phitin ;
5     n             = ss / ( 'M_LN10 * phitin ) + nd * absvdsin ;
6     vtof          = vto + vtzeta * ( tambin - tnomin );
7     tfacmobin    = pow(( tambin / tnomin ), epsilon );
8     if (dibsat != 0) begin
9         vsatdibl = absvdsin / ( pow(( 1.0 + pow( absvdsin / dibsat , beta )
10        ),( 1.0/beta )) );
11     end else begin
12         vsatdibl = 0;
13     end
14     delta          = ( delta1 - vsatdibl * delta2 ) * absvdsin ;
15     vtdibl        = vtof - delta ;
16     two_n_phit   = 2.0 * n * phitin ;
17     qref          = cgin * two_n_phit ;
18     // Qinvv
19     myarg          = vtdibl - flagsp * alpha_phit / 2.0;
20     exparg         = (( mmax( vgsin ,vgdin ,mmaxs ) - myarg ) / ( alpha_phit )
21 );
22     if (exparg > 'MMAXEXP) begin
23         ff          = 0.0;
24     end else if (exparg < -'MMAXEXP) begin
25         ff          = 1.0;
26     end else begin
27         ff          = 1.0 / ( 1.0 + exp( exparg ) );
28     end
29     eta            = ( mmax( vgsin ,vgdin ,mmaxs ) - ( vtdibl - flagsp * 0.1 *
30     alpha_phit * ff )) / two_n_phit ;
31     if (eta > 'MMAXEXP) begin
32         qinvv       = qref * eta;
33     end else if (eta < -'MMAXEXP) begin
34         qinvv       = qref * exp( eta );
35     end else begin
36         qinvv       = qref * ln( 1.0 + exp( eta ) );
37     end
38     // velocity
39     muf           = mu0 / ( tfacmobin * ( 1.0 + mtheta * qinvv /cgin ) );
40     vx            = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta *
41     tambin )) * ( 1.0 + lambda * absvdsin /lin ) / ( 1.0 + vtheta * qinvv/ cgin
42     );
43     vxf           = 2.0 * ff * phitin * muf / lin + ( 1.0 - ff ) * vx;
44     vdsats        = vx * lin / muf;
45     vdsats1       = vdsats * sqrt( 1.0 + 2.0 * qinvv / cgin / vdsats ) -
46     vdsats;
47     vdsat         = vdsats * ( 1.0 - ff ) + two_n_phit * ff;
48     vdsat1        = vdsats1 * ( 1.0 - ff ) + two_n_phit * ff;
49     fsd           = 1.0 / pow( 1.0 + pow( mmax( 0,( vdsin / vdsat1 ),mmaxs )
50     ,beta ),1.0 / beta );
51     vdx           = vdsin * fsd;
52     fds           = 1.0 / pow( 1.0 + pow( mmax( 0,( -vdsin / vdsat1 ),mmaxs
53     ),beta ),1.0 / beta );
54     vsx           = -vdsin * fds;

```

Source charge formulation

```

1 // Qinvs
2 exparg      = ( vgsin - myarg ) / ( alpha_phit );
3 if (exparg > 'M_MAXEXP) begin
4     ffs      = 0.0;
5 end else if (exparg < -'M_MAXEXP) begin
6     ffs      = 1.0;
7 end else begin
8     ffs      = 1.0 / ( 1.0 + exp( exparg ) );
9 end
10 etas       = ( vgdin - vsx - ( vtdibl - flagsp * 0.1 * alpha_phit *
11 ffs )) / two_n_phit;
12 if (etas > 'M_MAXEXP) begin
13     qinvs   = qref * etas;
14 end else if (etas < -'M_MAXEXP) begin
15     qinvs   = qref * exp( etas );
16 end else begin
17     qinvs   = qref * ln( 1.0 + exp( etas ) );

```

Drain charge formulation

```

1 // Qinvd
2 exparg      = ( vgdin - myarg ) / ( alpha_phit );
3 if (exparg > 'M_MAXEXP) begin
4     ffd      = 0.0;
5 end else if (exparg < -'M_MAXEXP) begin
6     ffd      = 1.0;
7 end else begin
8     ffd      = 1.0 / ( 1.0 + exp( exparg ) );
9 end
10 etad       = ( vgsin - vdx - ( vtdibl - flagsp * 0.1 * alpha_phit *
11 ffd )) / two_n_phit;
12 if (etad > 'M_MAXEXP) begin
13     qinvd   = qref * etad;
14 end else if (etad < -'M_MAXEXP) begin
15     qinvd   = qref * exp( etad );
16 end else begin
17     qinvd   = qref * ln( 1.0 + exp( etad ) );

```

Drain current formulation

```

1 // Current
2 vdsc       = ( qinvs - qinvd ) / cgin;
3 myarg      = vdsc / vdsat;
4 fsat       = myarg / ( pow( 1.0 + pow( absfunc( myarg, mmaxs ), beta )
5 , 1.0 / beta ) );
6 vel        = vxf * fsat;
7 idsout    = type * w * ngf * 0.5 * ( qinvs + qinvd ) * vel *
trapfracdl;

```

This completes the Verilog-A code for modeling drain current in GaN HEMTs. The model is fully symmetric with regard to S/D and satisfies the Gummel symmetry tests. In

addition to currents, charges associated with the device are to be modeled to enable dynamic device applications. This is explained in the following section.

5.4 Transistor Channel Charge Formulation

Any compact model in addition to models for terminal currents must also include descriptions for terminal charges. Models for charges (and hence capacitances) are essential to reproduce dynamic behavior of devices for circuit simulation purposes. MVSG has model for all terminal charges. In addition to gate-charge of intrinsic transistor, the charges associated with all FPs are modeled in a distributed fashion based on internal node voltages. The gate charge in each transistor element is partitioned into gate-source charge (Q_{GSi}) and gate-drain charge (Q_{GDi}) using the well known Ward-Dutton charge partitioning. A simple single moment partition method is used to get analytical closed form expressions for Q_{GSi} and Q_{GDi} .

$$Q_{GSi} = \int_0^{L_g} \left(1 - \frac{x}{L_g}\right) Q_{Gi}(x) dx \quad (19a)$$

$$Q_{GDi} = \int_0^{L_g} \left(\frac{x}{L_g}\right) Q_{Gi}(x) dx \quad (19b)$$

Here $Q_{Gi}(x)$ is the areal charge density at any point x in the channel. $Q_{Gi}(x)$ and its dependence on bias depends on the mode of transport of carriers in the channel. The model for charge partitioning based on quasi-ballistic transport and NVsat formulation is described in detail in [5]. Here a fully continuous, derivable and fully symmetric charge partitioning model based on DD transport including pinch-off and velocity saturation effects will be discussed. The model satisfies the charge symmetry tests (McAndrew tests) akin to Gummel symmetry for currents. Firstly, model for gate charge in longer channel GaN HEMTs where transport is drift-diffusion (DD) based, either in velocity saturation or mobility-limited regime will be discussed (5.4.1). The section is then followed by charges associated with field plates and cross-coupled charges and body-charges (5.4.2).

5.4.1 Gate Charge In Drift Diffusion Regime

To model gate charge in DD regime, the approach adopted by Yannis Tsividis is closely followed. The derivation procedure for gate charge in this regime is similar to that found in their book (section 6.4.2, chapter 6) [6] and is extended to include Vsat regime. The source and drain partitioned charges are based on Q_{invs0} and Q_{invd0} terms used for current formulation (DIBL effect is removed from these terms to avoid negative capacitances) and is therefore self-consistent with transport. The details of the model are discussed in [6] and only brief description of the expressions are given here:

$$Q_{inv} = \frac{2}{3} WL_g \left[\frac{Q_{invs0}^2 + Q_{invd0}^2 + Q_{invs0}Q_{invd0}}{Q_{invs0} + Q_{invd0}} \right] \quad (20)$$

$$Q_s = \frac{2}{15} WL_g \left[\frac{2Q_{invs0}^3 + 3Q_{invd0}^3 + 4Q_{invs0}^2Q_{invd0} + 6Q_{invd0}^2Q_{invs0}}{Q_{invs0}^2 + Q_{invd0}^2 + 2Q_{invs0}Q_{invd0}} \right] \quad (21)$$

$$Q_d = Q_{\text{inv}} - Q_s \quad (22)$$

These definitions of Q_s and Q_d bring in self-consistency with transport model. Since expressions for Q_{invs} and Q_{invd} remain the same as that in model for current and (20-22) are arrived at based on physics (please refer [5] for more details), charge model is self-consistent with current model.

5.4.2 Field Plate Charges

The channel charge of the FPs is partitioned to their corresponding source and drain internal nodes using the expressions (20-22) Q_{invs} and Q_{invd} corresponding to the FPs. This is done via the function call to ***calc_iq*** (5.4.3) with the corresponding FP parameters. However, in addition to the channel charges, cross-coupled charges are associated with each FP due to fringing fields. That is, for each FP connected to {gate, source} there is a capacitance associated with between drain and the other terminal: {source, gate}. So when $\text{flagfp}\{i\}=0$ an additional C_{GDX} component is present and for $\text{flagfp}\{i\}=1$ an additional C_{SDX} component is present. This cross-coupled capacitance has threshold voltage $V_{T,\text{FP}\{i\}}$ corresponding to that FP ($vtofp\{i\}$) and fringing capacitance per unit width ($ccfp\{i\}$) extractable from CV measurements in off state. A detailed extraction procedure of these parameters is given Section 8. Here the formulation equations are given in (23).

$$Q_{C,\text{FP}\{i\}} = CC_{\text{FP}\{i\}} W n_{\text{FP}\{i\}} \varphi_t \ln \left(1 + \exp \frac{V_{G\{s/d\}i\text{FP}\{i\}} - (V_{T,\text{FP}\{i\}} - \alpha \varphi_t F_f)}{n_{\text{FP}\{i\}} \varphi_t} \right) \quad (23)$$

The body capacitance associated with each FP is computed in the same way as in (23)

$$Q_{B,\text{FP}\{i\}} = CB_{\text{FP}\{i\}} W n_{\text{FP}\{i\}} \varphi_t \ln \left(1 + \exp \frac{V_{\text{BDiFP}\{i\}} - (V_{T,\text{FP}\{i\}} - \alpha \varphi_t F_f)}{n_{\text{FP}\{i\}} \varphi_t} \right) \quad (24)$$

Finally, the capacitance associated with the gate field plate extension on the source-side is computed using similar method (instead of adding additional transistors for ease of computation). The capacitance is implemented only if $\text{flagfp}\{i\}s=1$.

$$Q_{S,\text{FP}\{i\}} = CS_{\text{FP}\{i\}} W n_{\text{FP}\{i\}} \varphi_t \ln \left(1 + \exp \frac{V_{\text{GsiFP}\{i\}} - (V_{T,\text{FP}\{i\}} - \alpha \varphi_t F_f)}{n_{\text{FP}\{i\}} \varphi_t} \right) \quad (25)$$

Section 5.4.3 shows the Verilog-A implementation of the core-equations of the charge model described above.

5.4.3 Analog Function: ***calc_iq*** (Charge Formulation)

The Verilog-A codes associated with the charge model in ***calc_iq*** are as follows.

Source and drain charge formulation with DIBL removed

```

1 // charge calc
2 n0      = ss / ( 'M_LN10 * phitin );
3 two_n_phito = 2.0 * n0 * phitin;

```

```

4      qref0      = cgin * two_n_phit0;
5      // Qinvv0
6      myarg0     = vtov - flagsp * alpha_phit / 2.0;
7      exparg0    = (( mmax( vgsin ,vgdin ,mmaxs ) - myarg0 )/( alpha_phit ))
8      ;
9      if (exparg0 > 'M_MAXEXP) begin
10         ff0      = 0.0;
11     end else if (exparg0 < -'M_MAXEXP) begin
12         ff0      = 1.0;
13     end else begin
14         ff0      = 1.0 / ( 1.0 + exp( exparg0 ) );
15     end
16     eta0      = ( mmax( vgsin ,vgdin ,mmaxs ) - ( vtov - flagsp * 0.1 *
alpha_phit * ff0 )) / two_n_phit0;
17     if (eta0 > 'M_MAXEXP) begin
18         qinvv0   = qref0 * eta0;
19     end else if (eta0 < -'M_MAXEXP) begin
20         qinvv0   = qref0 * exp( eta0 );
21     end else begin
22         qinvv0   = qref0 * ln( 1.0 + exp( eta0 ) );
23     end
24     // velocity0
25     muf0      = mu0 / tfacmobin;
26     vx0       = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta *
tambin ));
27     vdsats0   = vx0 * lin / muf0;
28     vdsats10  = vdsats0 * sqrt( 1.0 + 2.0 * qinvv0 / cgin / vdsats0 ) -
vdsats0;
29     vdsat10   = vdsats10 * ( 1.0 - ff0 ) + two_n_phit0 * ff0;
30     fsd0      = 1.0 / pow( 1.0 + pow( mmax(0,( vdsin / vdsat10 ),mmaxs )
,beta ),1.0 / beta );
31     vdx0      = vdsin * fsd0;
32     fds0      = 1.0 / pow( 1.0 + pow( mmax(0,( -vdsin / vdsat10 ),mmaxs )
,beta ),1.0 / beta );
33     vsx0      = -vdsin * fds0;
34     exparg0   = ( vgsin - myarg0 ) / ( alpha_phit );
35     if (exparg0 > 'M_MAXEXP) begin
36         ffs0      = 0.0;
37     end else if (exparg0 < -'M_MAXEXP) begin
38         ffs0      = 1.0;
39     end else begin
40         ffs0      = 1.0 / ( 1.0 + exp( exparg0 ) );
41     end
42     etas0      = ( vgdin - vsx0 - ( vtov - flagsp * 0.1 * alpha_phit *
ffs0 )) / two_n_phit0;
43     if (etas0 > 'M_MAXEXP) begin
44         qinvs0   = qref0 * etas0;
45     end else if (etas0 < -'M_MAXEXP) begin
46         qinvs0   = qref0 * exp( etas0 );
47     end else begin
48         qinvs0   = qref0 * ln( 1.0 + exp( etas0 ) );
49     end
50     exparg0   = ( vgdin - myarg0 ) / ( alpha_phit );
51     if (exparg0 > 'M_MAXEXP) begin

```

```

51      ffd0      = 0.0;
52  end else if (exparg0 < -M_MAXEXP) begin
53      ffd0      = 1.0;
54  end else begin
55      ffd0      = 1.0 / ( 1.0 + exp( exparg0 ) );
56  end
57      etad0      = ( vgsin - vdx0 - ( vtof - flagsp * 0.1 * alpha_phit *
58      ffd0 )) / two_n_phit0;
59  if (etad0 > M_MAXEXP) begin
60      qinvd0      = qref0 * etad0;
61  end else if (etad0 < -M_MAXEXP) begin
62      qinvd0      = qref0 * exp( etad0 );
63  end else begin
64      qinvd0      = qref0 * ln( 1.0 + exp( etad0 ) );

```

DD-channel charge partitioning

```

1      qs2      = qinvs0 * qinvs0 + 1e-38;
2      qs3      = qs2 * qinvs0 + 1e-57;
3      qd2      = qinvd0 * qinvd0 + 1e-38;
4      qd3      = qd2 * qinvd0 + 1e-57;
5      qsqd     = qinvs0 * qinvd0 + 1e-38;
6      qinvdd   = 2.0 / 3.0 * ( qs2 + qd2 + qsqd ) / ( qinvs0 + qinvd0 +
7      2e-19 );
8      qd1      = 2.0 * ( 2.0 * qs3 + 3.0 * qd3 + 4.0 * qs2 * qinvd0 +
9      6.0 * qd2 * qinvs0 ) / ( 15.0 * ( qs2 + qd2 + 2.0 * qsqd ) );
10     qs       = qinvdd - qd1;
11     qd       = qd1;
12     qgsout   = w * ngf * lin * type * qs * trapfracd1;
13     qgdout   = w * ngf * lin * type * qd * trapfracd1;

```

FP cross-coupled and body charge formulation

```

1      if ( qcbflag==1) begin
2          etac      = ( vcin - ( vtov - flagsp * 0.5 * alpha_phit )) /
two_n_phit0;
3          if (etac > 'M_MAXEXP) begin
4              exparg = etac;
5          end else if (etac < -'M_MAXEXP) begin
6              exparg = exp( etac );
7          end else begin
8              exparg = ln( 1.0 + exp( etac ) );
9          end
10         qcout     = w * ngf * type * cc * two_n_phit0 * exparg *
trapfracdl;
11         etab      = ( vbin - ( vtov - flagsp * 0.5 * alpha_phit )) /
two_n_phit0;
12         if (etab > 'M_MAXEXP) begin
13             exparg = etab;
14         end else if (etab < -'M_MAXEXP) begin
15             exparg = exp( etab );
16         end else begin
17             exparg = ln( 1.0 + exp( etab ) );
18         end
19         qbout    = w * ngf * type * cb * two_n_phit0 * exparg *
trapfracdl;
20         end else begin
21             qcout    = 0;
22             qbout    = 0;
23         end

```

FP source side charge formulation

```

1      if (qgsflag==1) begin
2          etags     = ( vgsin - ( vtov - flagsp * 0.5 * alpha_phit )) /
two_n_phit0;
3          if (etags > 'M_MAXEXP) begin
4              exparg = etags;
5          end else if (etags < -'M_MAXEXP) begin
6              exparg = exp( etags );
7          end else begin
8              exparg = ln( 1.0 + exp( etags ) );
9          end
10         qsout    = w * ngf * type * cs * two_n_phit0 * exparg *
trapfracdl;
11         end else begin
12             qsout    = 0;
13         end
14         calc_iq   = idsout;
15     end
16 endfunction

```

Along with the code presented in section 5.3.3, this fully completes the *calc_iq* function.

5.4.4 Model for Fringing Field Capacitances

The fringing capacitance between any pair of the four device terminals is computed using both a bias-independent ($Cof\{i\}m0$) and bias-dependent ($Cof\{i\}m$) parameter, where $i = s, d, ds, dsub, ssub$, or $gsub$. First, these parameters are temperature modulated via `calc_capt` in section 5.2 to produce the variables `Cof{i}mt0` and `Cof{i}mt`. These are then used in (26) to obtain the charge between each terminal pair which contributes to dynamic behavior. [10] The location of these capacitances are shown in Fig. 4.

$$Q_{of\{s,d,ds,dsub,ssub,gsub\}} = Wn_{gf} \left(C_{of\{s,d,ds,dsub,ssub,gsub\}mt0} V + C_{of\{s,d,ds,dsub,ssub,gsub\}mt} n_{Frin} \ln \left(1 + \exp \frac{V - V_{TFrin}}{n_{Frin}} \right) \right) \quad (26)$$

The first term determined by the variable `Cof{i}mt0` is the bias-independent capacitance and the second term determined by the variable `Cof{i}mt` governs the long bias dependent “tail” in the measured CV-characteristics shown in Fig. 12. The earlier non-physical approach (prior to **V2.1.0**) to capture this tail using a “dummy” field-plate in the model should be avoided.

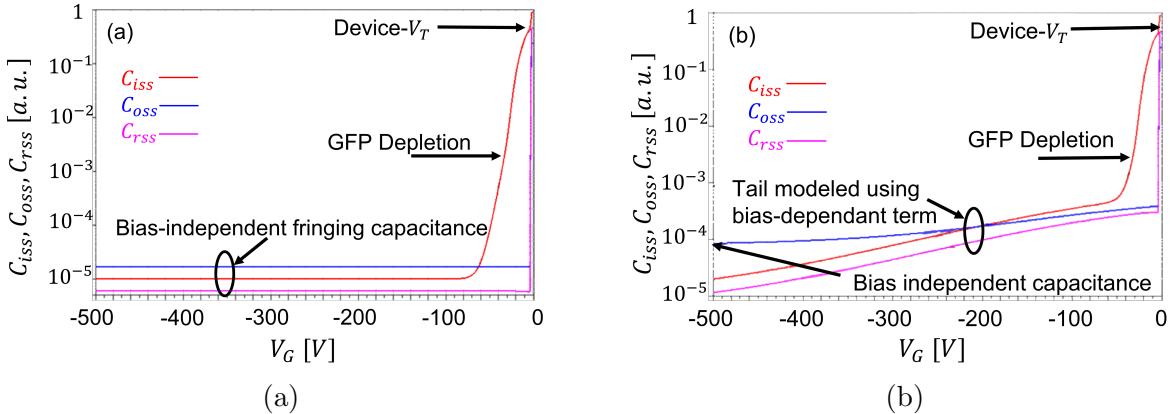


Figure 12: (a) Previous CV-behavior in the MVSG model vs. (b) current CV-behavior. The tail-beyond the last FP-depletion is modeled using the bias-dependent term. The final constant capacitance value that the CV “settles to” is the original bias-independent term of the **V2.1.0** model.

The following lines of code execute these capacitances.

```

1 // Fringing capacitances
2 if (((V(gi1,s) - vtfrin) / nfrin) > 'M_MAXEXP) begin
3     qofs          = w * ngf * (cofsmt0 * V(gi1,s) + cofsmt * (V(gi1,s) -
4         vtfrin));
5 end else if (((V(gi1,s) - vtfrin) / nfrin) < -'M_MAXEXP) begin
6     qofs          = w * ngf * (cofsmt0 * V(gi1,s) + cofsmt * nfrin * exp( (V(
7         gi1,s) - vtfrin) / nfrin));
8 end else begin

```

```

7      qofs      = w * ngf * (cofsmt0 * V(gi1,s) + cofsm * nfrin * ln( 1.0
8      + exp( (V(gi1,s) - vtfrin) / nfrin)));
9 end
10 I(gi1,s)      <+ ddt(qofs);
11 if (((V(gi1,d) - vtfrin) / nfrin) > 'M_MAXEXP) begin
12   qofd      = w * ngf * (cofdmt0 * V(gi1,d) + cofdm * (V(gi1,d) -
13   vtfrin));
14 end else if (((V(gi1,d) - vtfrin) / nfrin) < -'M_MAXEXP) begin
15   qofd      = w * ngf * (cofdmt0 * V(gi1,d) + cofdm * nfrin * exp( (V
16   (gi1,d) - vtfrin) / nfrin));
17 end else begin
18   qofd      = w * ngf * (cofdmt0 * V(gi1,d) + cofdm * nfrin * ln( 1.0
19   + exp( (V(gi1,d) - vtfrin) / nfrin)));
20 end
21 I(gi1,d)      <+ ddt(qofd);
22
23 if (((V(s,d) - vtfrin) / nfrin) > 'M_MAXEXP) begin
24   qofds     = w * ngf * (cofdsmt0 * V(s,d) + cofdsmt * (V(s,d) -
25   vtfrin));
26 end else if (((V(s,d) - vtfrin) / nfrin) < -'M_MAXEXP) begin
27   qofds     = w * ngf * (cofdsmt0 * V(s,d) + cofdsmt * nfrin * exp( (V
28   (s,d) - vtfrin) / nfrin));
29 end else begin
30   qofds     = w * ngf * (cofdsmt0 * V(s,d) + cofdsmt * nfrin * ln( 1.0
31   + exp( (V(s,d) - vtfrin) / nfrin)));
32 end
33 I(s,d)      <+ ddt(qofds);
34
35 if (((V(b,s) - vtfrin) / nfrin) > 'M_MAXEXP) begin
36   qofssub   = w * ngf * (cofssubmt0 * V(b,s) + cofssubmt * (V(b,s) -
37   vtfrin));
38 end else if (((V(b,s) - vtfrin) / nfrin) < -'M_MAXEXP) begin
39   qofssub   = w * ngf * (cofssubmt0 * V(b,s) + cofssubmt * nfrin * exp
40   ( (V(b,s) - vtfrin) / nfrin));
41 end else begin
42   qofssub   = w * ngf * (cofssubmt0 * V(b,s) + cofssubmt * nfrin * ln(
43   1.0 + exp( (V(b,s) - vtfrin) / nfrin)));
44 end
45 I(b,s)      <+ ddt(qofssub);
46
47 if (((V(b,d) - vtfrin) / nfrin) > 'M_MAXEXP) begin
48   qofdsub   = w * ngf * (cofdsubmt0 * V(b,d) + cofdsubmt * (V(b,d) -
49   vtfrin));
50 end else if (((V(b,d) - vtfrin) / nfrin) < -'M_MAXEXP) begin
51   qofdsub   = w * ngf * (cofdsubmt0 * V(b,d) + cofdsubmt * nfrin * exp
52   ( (V(b,d) - vtfrin) / nfrin));
53 end else begin
54   qofdsub   = w * ngf * (cofdsubmt0 * V(b,d) + cofdsubmt * nfrin * ln(
55   1.0 + exp( (V(b,d) - vtfrin) / nfrin)));
56 end
57 I(b,d)      <+ ddt(qofdsub);
58
59 if (((V(gi1,b) - vtfrin) / nfrin) > 'M_MAXEXP) begin

```

```

48 qofgsub           = w * ngf * (cofgsubmt0 * V(gi1,b) + cofgsubmt * (V(gi1,b)
- vtfrin));
49 end else if (((V(gi1,b) - vtfrin) / nfrin) < -M.MAXEXP) begin
50   qofgsub           = w * ngf * (cofgsubmt0 * V(gi1,b) + cofgsubmt * nfrin *
exp( (V(gi1,b) - vtfrin) / nfrin));
51 end else begin
52   qofgsub           = w * ngf * (cofgsubmt0 * V(gi1,b) + cofgsubmt * nfrin *
ln( 1.0 + exp( (V(gi1,b) - vtfrin) / nfrin)));
53 end
54 I(gi1,b)          <+ ddt(qofgsub);

```

5.5 Gate Current Formulation

Gate current formulation for Schottky gated GaN HEMTs (typically in RF-GaN HEMTs) includes two Schottky diodes between gate-source and gate-drain terminals. The model is identical for the two diodes but the parameters can be independently set. By default, MVSG places gate diodes between **gi2p** and **fps4/fp4** nodes, but a fraction may also be placed between **gi2p** and **si/di** nodes for backward compatibility purposes by adjusting *fracig* (5.5.3).

The gate current is computed using the function ***calc_ig*** (5.5.4) which computes the forward (5.5.1) and reverse recombination(5.5.2) currents separately and returns the sum. It also includes the ability to incorporate temperature dependence, high injection effect (in forward), saturation (in reverse), and breakdown.

In summary, the total current through each gate diode is the sum of $I_{Fg\{s/d\}i}$ (5.5.1) and $I_{Rg\{s/d\}i}$ (5.5.2), and then multiplied by the appropriate value determined by *fracig* (5.5.3).

5.5.1 Forward-Gate Current Model

The forward diode current when high injection is off ($frac\{s/d\}=1$) is given by the expression

$$I_{Fg\{s/d\}i} = W n_{gf} i_{j\{s/d\}} \left(\frac{T}{T_0} \right)^{egate} \left(\exp \left(\frac{p_{g,param\{s/d\}} V_{g\{s/d\}i}}{\varphi_t} - \frac{p_{g,param1} V_{jg}}{\varphi_t} \right) - (k_{bdgate\{s/d\}}) i_{g\{s/d\},bd} - \exp \left(\frac{-p_{g,param1} V_{jg}}{\varphi_t} \right) \right) \quad (27)$$

which includes the temperature dependence of the unit-width reverse saturation current $i_{j\{s,d\}}$, bandgap dependence (through V_{jg}) and ideality factor dependence through $p_{g,param\{s/d\}}$. $V_{g\{s/d\}i}$ represents the forward voltage across the diode and it's value depends on the location it is placed in the equivalent circuit model (5.5.3). The subscript name in the manual was chosen as only internal gate diodes were present historically. T is the device temperature, T_0 is the reference temperature (value of *t_{nom}* in K), while *egate* is the diode temperature coefficient, which is 3.0 in the model.

When high injection is on ($frac\{s/d\}<1$), $I_{Fg\{s/d\}i}$ must be computed in a different method. In physical diodes, prior to the onset of high injection (given by the parameter

$vgsat\{s/d\}$), the forward current remains the same. After about $V_{g\{s/d\}i} > vgsat\{s/d\}$, the slope of the forward current curve (in log scale) decreases by $frac\{s/d\}$. To compute the current when high injection is on, start by computing the no high injection current, which takes on the exact same form as (27), and is shown in (28). The only difference is that the value is assigned to a different variable name.

$$I_{Fg\{s/d\}i,nohinv} = Wn_{gf} i_{j\{s/d\}} \left(\frac{T}{T_0} \right)^{egate} \left(\exp \left(\frac{p_{g,param\{s/d\}} V_{g\{s/d\}i}}{\varphi_t} - \frac{p_{g,param1} V_{jg}}{\varphi_t} \right) - (kbgate\{s/d\}) i_{g\{s/d\},bd} - \exp \left(\frac{-p_{g,param1} V_{jg}}{\varphi_t} \right) \right) \quad (28)$$

Next, the unshifted high injection current is computed and is given in (29). The only difference is that $p_{g,param\{s/d\}}$ is multiplied by $frac\{s/d\}$ which represents the smaller inverse ideality factor resulting from high injection.

$$I_{Fg\{s/d\}i,hinj,un} = Wn_{gf} i_{j\{s/d\}} \left(\frac{T}{T_0} \right)^{egate} \left(\exp \left(\frac{(frac\{s/d\}) p_{g,param\{s/d\}} V_{g\{s/d\}i}}{\varphi_t} - \frac{p_{g,param1} V_{jg}}{\varphi_t} \right) - (kbgate\{s/d\}) i_{g\{s/d\},bd} - \exp \left(\frac{-p_{g,param1} V_{jg}}{\varphi_t} \right) \right) \quad (29)$$

With these two equations, (28) represents the forward current with $V_{g\{s/d\}i} < vgsat\{s/d\}$, and (29) represents the forward current with $V_{g\{s/d\}i} > vgsat\{s/d\}$, although shifted down (in the log scale). In order to make these two curves intersect at $vgsat\{s/d\}$, (29) must be shifted up. Shifting simply requires division by the right side current value at $vgsat\{s/d\}$ and multiplication by the left side current value at the same voltage. Performing this and assigning in the final high injection equation for $V_{g\{s/d\}i} > vgsat\{s/d\}$ gives (30).

$$I_{Fg\{s/d\}i,hinj} = \begin{cases} I_{Fg\{s/d\}i,hinj,un} \times \frac{I_{Fg\{s/d\}i,nohinv}(V_{gsat\{s/d\}})}{I_{Fg\{s/d\}i,hinj,un}(V_{gsat\{s/d\}})} & \text{if } frac\{s/d\} > 0 \\ I_{Fg\{s/d\}i,nohinv}(V_{gsat\{s/d\}}) & \text{if } frac\{s/d\} = 0 \end{cases} \quad (30)$$

Note that if $frac\{s/d\}=0$, then (29) is not calculated, and the high injection current is taken to be a constant value shown in (30). This is necessary as (29) returns zero and would result in a divide by zero condition. The final step is to combine (28) and (30), such that there is some smoothing between the two curves at $vgsat\{s/d\}$. The Fermi function shown in (31) is employed to smooth the forward gate current when high injection is on.

$$F_{f,vg} = \frac{1}{1 + \exp \frac{V_{g\{s/d\}i} - [V_{gsat\{s/d\}} - \frac{1}{2} \alpha_{g\{s/d\}}^2 \varphi_t]}{\alpha_{g\{s/d\}}^2 \varphi_t}} \quad (31)$$

The final current is then given by (32) which combines (28) and (30) with (31).

$$I_{Fg\{s/d\}i} = F_{f,vg} I_{Fg\{s/d\}i,nohinv} + (1.0 - F_{f,vg}) I_{Fg\{s/d\}i,hinj} \quad (32)$$

The parameter $\text{alphag}\{s/d\}$ controls the level of smoothing at the onset of high injection. A graphic showing the functionality is shown in Fig. 13.

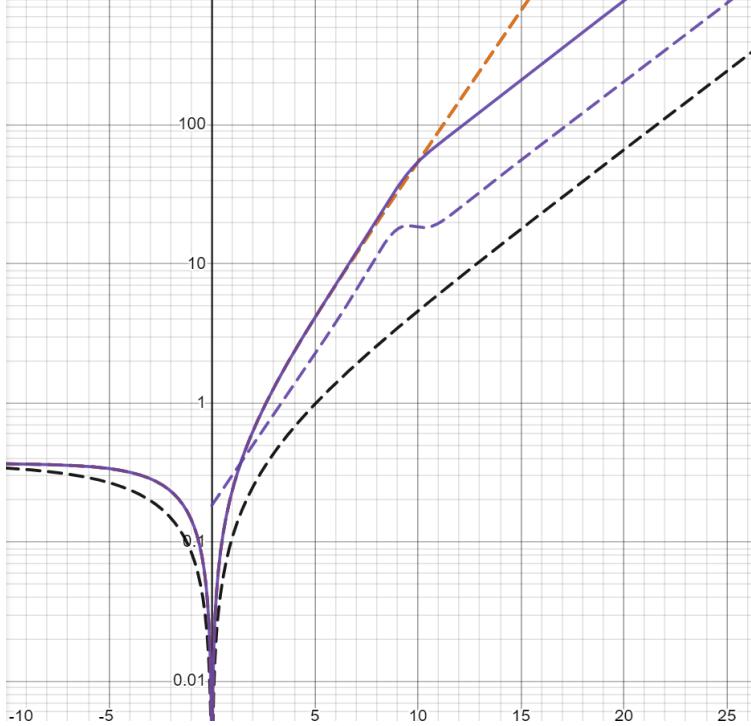


Figure 13: A representation of the formulation of high injection current in MVSG `calc_ig`. The upper black dashed curve shows the no high injection current (28), while the lower black dashed curve shows the reduced inverse ideality factor current (29). This is then shifted up to give the orange dashed curve (30). Finally, the solid purple curve shows the combination of the upper black dashed curve and the orange dashed curve using the Fermi function (32). The purple dashed curve shows the derivative of the solid purple curve, showing that forward gate current with high injection is monotonic (derivative is always positive).

The middle term in (27) accounts for gate-breakdown, where the coefficient $\text{kbdgate}\{s/d\}$ is a parameter, and the term multiplied to it is given by

$$i_{g\{s/d\},bd} = \exp\left(-p_{bdg\{s/d\}}(V_{g\{s/d\}i} + V_{bdg\{s/d\}}) - \frac{p_{g,param1}V_{jg}}{\varphi_t}\right) - \exp\left(-p_{bdg\{s/d\}}V_{bdg\{s/d\}} - \frac{p_{g,param1}V_{jg}}{\varphi_t}\right) \quad (33)$$

The parameter $vbdg\{s/d\}$ controls the reverse voltage at which breakdown occurs (resulting in an exponential rise in current) with an inverse ideality factor determined by the parameter $pbdg\{s/d\}$. If $\text{kbdgate}\{s/d\}=0$ (by default), breakdown is turned off, (27) reduces to (34)

and adopts a more familiar, simpler diode equation.

$$I_{Fg\{s/d\}i} = W n_{gf} i_{j\{s/d\}} \left(\frac{T}{T_0} \right)^{egate} \exp \left(-\frac{p_{g,param1} V_{jg}}{\varphi_t} \right) \left(\exp \left(\frac{p_{g,param\{s/d\}} V_{g\{s/d\}i}}{\varphi_t} \right) - 1 \right) \quad (34)$$

If high injection is on, (28) & (29) may be simplified in the exact same way.

5.5.2 Reverse Recombination-Gate Current Model

In addition to forward current, the reverse GIDL and recombination currents are captured through empirical diode equations to account for drain voltage dependence on reverse-leakage gate currents. The reverse current formulation is given by

$$I_{Rg\{s/d\}i} = -W n_{gf} i_{rec\{s/d\}} \left(\frac{T}{T_0} \right)^{egate} \left(\exp \frac{p_{gs,rec\{s/d\}} F_{recg\{s/d\}}}{\varphi_t} - 1 \right) \quad (35)$$

where $F_{recg\{s/d\}}$ is the reverse voltage across the diode accounting for saturation and is given by

$$F_{recg\{s/d\}} = \frac{-V_{g\{s/d\}i}}{\left(1 + \left| \frac{V_{g\{s/d\}i}}{V_{gsatq\{s/d\}}} \right|^{\beta_{rec\{s/d\}}} \right)^{\frac{1}{\beta_{rec\{s/d\}}}}} \quad (36)$$

Additionally, a second recombination current component (for $V_{GD} < 0$ regimes) can be invoked by calling the same recombination module (35, 36) with a different parameter set by setting *igrecmod*=1. The recombination current regimes in GaN HEMTs show the “double-saturation” behavior which can be effectively captured with this dual-recombination semi-empirical approach.

5.5.3 Gate-Current De-Biasing and Node-Assignment

To account for CV-discontinuities associated with FP-turn on/off and associated gate-current transitions (that can be interpreted as discontinuities in their derivatives, see Fig. 14), gate-diodes are re-assigned to connect between internal gate (**gi2p**) and source/drain nodes of last FP (**fps4,fp4**) since **V3.0.0**. This ensures that the gate-currents do not change with FP-depletion on source/drain access regions as they are only de-biased through access transistors and contact-resistances. Measurements seem to indicate the validity of this approach as they do not show significant discontinuities in gate currents at FP threshold voltages (**vtوفp{i}**). However, the older assignment to internal source/drain nodes (**si,di**) is retained via a parameter *fracig* for backward compatibility and ease-of-use (*fracig*=0 to turn off the branches to the internal source/drain nodes by default). Fig. 15 shows a partial MVSG schematic of the old and new arrangement of gate diodes. [10]

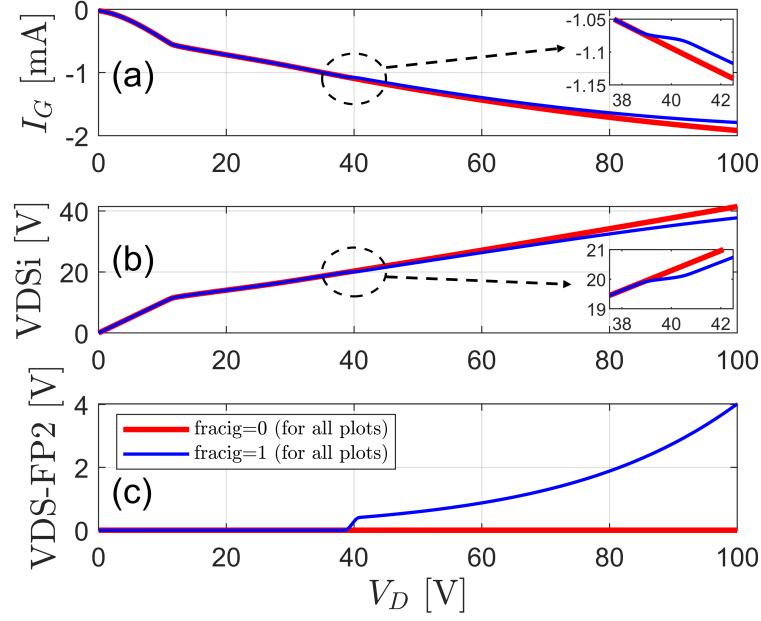


Figure 14: Behavior of **(a)** I_G , **(b)** intrinsic transistor voltage drop (V_{DSi}), and **(c)** field plate voltage drop (V_{DS-FP2}) in a V_{DS} sweep. In blue is $fracig=1$ which uses the internal gate diodes found in **V2.1.0**, and in red is $fracig=0$ which uses the external gate diodes added in **V3.0.0**. At the FP threshold voltage $V_D = |V_{T0,FP2}| = 40$ V, $fracig=1$ shows abrupt depletion of the FP which causes saturation in I_G and V_{DSi} . This causes discontinuities in derivatives of I_G and gate-charge which show up in I_G plots. $fracig=0$ eliminates this issue as gate current no longer flows through the FP transistors.

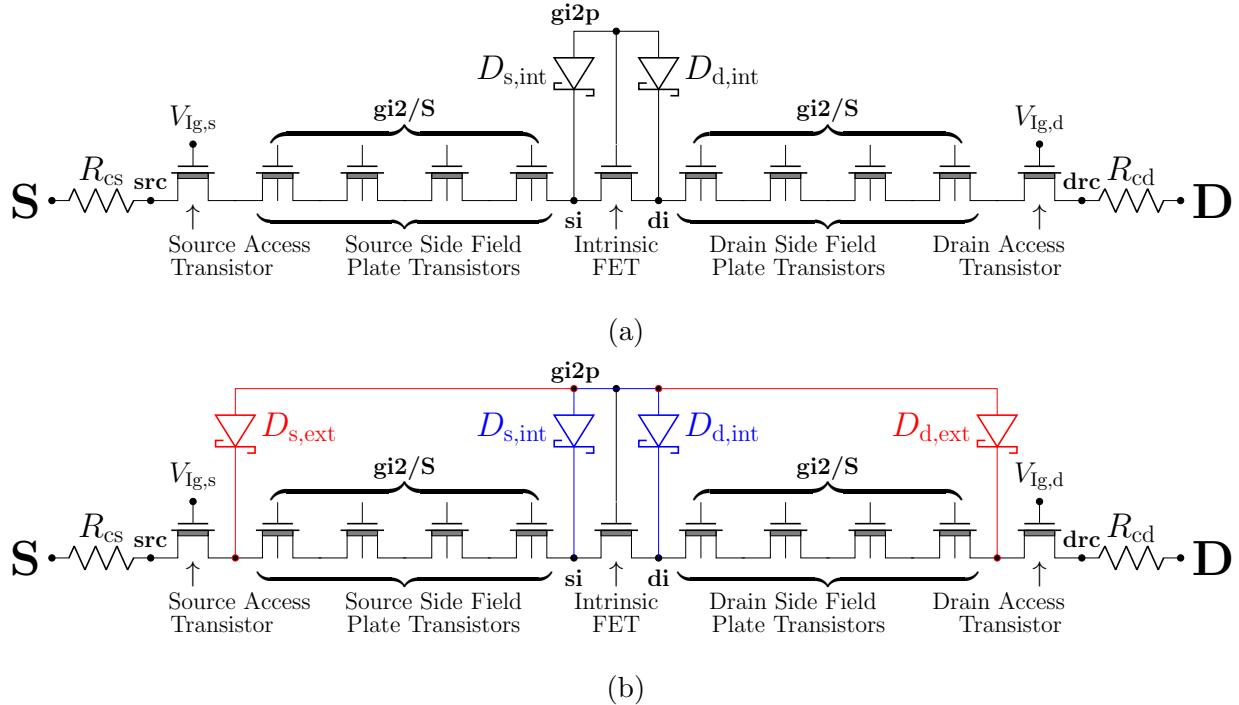


Figure 15: **(a)** Partial MVSG schematic from **V2.1.0** which shows that gates diodes are connected between the internal gate node (**gi2p**) and the intrinsic transistor source/drain nodes (**si,di**) (Note that the **gi2p** node was renamed in **V3.2.0** from **gi2**). The diodes were de-biased through FP and access transistors. **(b)** Following **V3.0.0**, the diodes are split into two branches (one to original **si,di** nodes (blue) and another to last FP-node **fps4,fp4** (red)). These external gate diodes are de-biased only through access transistors and contact resistances.

5.5.4 Analog Function: *calc_ig*

Function I/O definition

```

1 analog function real calc_ig;
2   output isdiodeout, isrecout;
3   input vgin, phitin;
4   input vgsatin, alphagin, fracin, pg-paramin, pbdgin, vbdgin, tfacdiodein;
5   input w, ngf, ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin,
6   pg-param1, vjg, type;
7   // IO
8   real isdiodeout, isrecout;
9   real vgin, phitin;
10  real vgsatin, alphagin, fracin, pg-paramin, pbdgin, vbdgin, tfacdiodein;
11  real w, ngf, ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin,
12  pg-param1, vjg, type;
13  // Local
14  real igout, alpha2_phit, t0, ffvgin, iginbd, igindiode;
15  real frecgin, iginrec;
16  real expbdarg1, expbdarg2, expbd1, expbd2, expphib, expffvarg, expiforarg,
17  expifor, expirevarg, expirev;
18  real pg-paramin_hinj, expbdarg1_vgsat, expbd1_vgsat, iginbd_vgsat;
19  real expiforarg_nohinj_vgsat, expifor_nohinj_vgsat, igindiode_nohinj_vgsat
20 , igindiode_nohinj;
21  real expiforarg_hinj_vgsat, expifor_hinj_vgsat, igindiode_hinj_vgsat;
22  real expiforarg_hinj, expifor_hinj, igindiode_hinj-pre, igindiode_hinj;
```

Current formulation

```

1 begin
2   expphib      = pg-param1 / phitin * (- vjg);
3   t0           = explim( expphib );
4
5   expbdarg1    = pbdgin * ( -vgin - vbdgin ) + expphib;
6   expbdarg2    = -pbdgin * vbdgin + expphib;
7   expbd1       = explim( expbdarg1 );
8   expbd2       = explim( expbdarg2 );
9   iginbd       = ( expbd1 - expbd2 );
10
11  isdiodeout   = type * w * ngf * ijin * tfacdiodein;
12  expiforarg   = pg-paramin / phitin * vgin + expphib;
13  expifor      = explim( expiforarg );
14  if (fracin == 1) begin
15    igindiode = isdiodeout * ( expifor - ( kbdgatein * iginbd ) - t0 )
16  ;
17  end else begin
18    expbdarg1_vgsat = pbdgin * ( -vgsatin - vbdgin ) + expphib;
19    expbd1_vgsat   = explim( expbdarg1_vgsat );
20    iginbd_vgsat   = ( expbd1_vgsat - expbd2 );
21
22    expiforarg_nohinj_vgsat = pg-paramin / phitin * vgsatin + expphib;
23    expifor_nohinj_vgsat   = explim( expiforarg_nohinj_vgsat );
24    igindiode_nohinj_vgsat = ( expifor_nohinj_vgsat - ( kbdgatein *
25     iginbd_vgsat ) - t0 );
```

```

25      igindiode_nohinj = isdiodeout * ( expifor - ( kbdgatein * iginbd )
26      - t0 );
27      if (fracin > 0) begin
28          pg-paramin_hinj = fracin * pg-paramin;
29
30          expiforarg_hinj_vgsat = pg-paramin_hinj / phitin * vgsatin +
31          expphib;
32          expifor_hinj_vgsat = explim( expiforarg_hinj_vgsat );
33          igindiode_hinj_vgsat = ( expifor_hinj_vgsat - ( kbdgatein *
34          iginbd_vgsat ) - t0 );
35
36          expiforarg_hinj = pg-paramin_hinj / phitin * vgin + expphib
37          ;
38          expifor_hinj = explim( expiforarg_hinj );
39          igindiode_hinj_pre = isdiodeout * igindiode_nohinj_vgsat /
40          igindiode_hinj_vgsat;
41          igindiode_hinj = igindiode_hinj_pre * ( expifor_hinj - (
42          kbdgatein * iginbd ) - t0 );
43          end else begin
44              igindiode_hinj = isdiodeout * igindiode_nohinj_vgsat;
45          end
46          alpha2_phit = alphagin * alphagin * phitin;
47          expffvarg = ( vgin - ( vgsatin - alpha2_phit / 2.0 ))/
48          alpha2_phit;
49          if (expffvarg > 'M_MAXEXP) begin
50              ffvgin = 0.0;
51          end else if (expffvarg < -'M_MAXEXP) begin
52              ffvgin = 1.0;
53          end else begin
54              ffvgin = 1.0 / ( 1.0 + exp( expffvarg ) );
55          end
56          igindiode = ffvgin * igindiode_nohinj + ( 1.0 - ffvgin ) *
57          igindiode_hinj;
58      end
59
60      frecgin = -vgin / pow(( 1.0 + pow( absfunc( vgin / vgsatqin,
61      mmaxs ), betarecin )), 1.0 / betarecin );
62      isrecout = -type * w * ngf * irecin * tfacdiodein * 1.0;
63      expirevarg = pgsrecin / phitin * frecgin;
64      expirev = explim( expirevarg );
65      iginrec = isrecout * ( expirev - 1.0 );
66
67      igout = igindiode + iginrec;
68      calc_ig = igout;
69  end
70 endfunction

```

Function calls to forward, first, and second reverse recombination current components

```

1 if (igmod == 1) begin
2     igs1           = calc_ig(igssdio , igsrec , type * V(gi2p ,  fps4) , phit , vgsats
3     , alphags , fracs , pg_params , pbdgs , vbdgs , tfacdiode , w , ngf ,(1.0 - fracig) * ijs ,
4     kbdgates , vgsatqs , betarecs ,(1.0 - fracig) * irecs , pgsrems , pg_param1 , vjg ,
5     type );
6     igd1           = calc_ig(igdsdio , igdrec , type * V(gi2p ,  fp4) , phit , vgsatd ,
7     alphagd , fracd , pg_paramd , pbdgd , vbdgd , tfacdiode , w , ngf ,(1.0 - fracig) * ijd ,
8     kbdgated , vgsatqd , betarecd ,(1.0 - fracig) * irecd , pgsrecd , pg_param1 , vjg ,
9     type );
10    I(gi2p ,  fps4) <+ igs1 + gmin * V(gi2p ,  fps4);
11    I(gi2p ,  fp4) <+ igd1 + gmin * V(gi2p ,  fp4);
12    if (igrecmod == 1) begin
13        igs12          = calc_ig(igssdio2 , igsrec2 , type * V(gi2p ,  fps4) , phit ,
14        vgsats , alphags , 1.0 , pg_params , pbdgs , vbdgs , tfacdiode , w , ngf , 0.0 , 0.0 , vgsatqs2 ,
15        betarecs2 ,(1.0 - fracig) * irecs2 , pgsrems2 , pg_param1 , vjg , type );
16        igd12          = calc_ig(igdsdio2 , igdrec2 , type * V(gi2p ,  fp4) , phit ,
17        vgsatd , alphagd , 1.0 , pg_paramd , pbdgd , vbdgd , tfacdiode , w , ngf , 0.0 , 0.0 , vgsatqd2 ,
18        betarecd2 ,(1.0 - fracig) * irecd2 , pgsrecd2 , pg_param1 , vjg , type );
19        I(gi2p ,  fps4) <+ igs12 + gmin * V(gi2p ,  fps4);
20        I(gi2p ,  fp4) <+ igd12 + gmin * V(gi2p ,  fp4);
21    end
22    if (fracig != 0) begin
23        igsidb         = calc_ig(igssdiadb , igsrecdb , type * V(gi2p ,  si) , phit ,
24        vgsats , alphags , fracs , pg_params , pbdgs , vbdgs , tfacdiode , w , ngf , fracig * ijs ,
25        kbdgates , vgsatqs , betarecs , fracig * irecs , pgsrems , pg_param1 , vjg , type );
26        igdidb         = calc_ig(igdsdiadb , igdrecdb , type * V(gi2p ,  di) , phit ,
27        vgsatd , alphagd , fracd , pg_paramd , pbdgd , vbdgd , tfacdiode , w , ngf , fracig * ijd ,
28        kbdgated , vgsatqd , betarecd , fracig * irecd , pgsrecd , pg_param1 , vjg , type );
29        I(gi2p ,  si) <+ igsidb + gmin * V(gi2p ,  si);
30        I(gi2p ,  di) <+ igdidb + gmin * V(gi2p ,  di);
31        if (igrecmod == 1) begin
32            igs12db        = calc_ig(igssdio2db , igsrec2db , type * V(gi2p ,  si) , phit ,
33            vgsats , alphags , 1.0 , pg_params , pbdgs , vbdgs , tfacdiode , w , ngf , 0.0 , 0.0 , vgsatqs2 ,
34            betarecs2 , fracig * irecs2 , pgsrems2 , pg_param1 , vjg , type );
35            igd12db        = calc_ig(igdsdio2db , igdrec2db , type * V(gi2p ,  di) , phit ,
36            vgsatd , alphagd , 1.0 , pg_paramd , pbdgd , vbdgd , tfacdiode , w , ngf , 0.0 , 0.0 , vgsatqd2 ,
37            betarecd2 , fracig * irecd2 , pgsrecd2 , pg_param1 , vjg , type );
38            I(gi2p ,  si) <+ igs12db + gmin * V(gi2p ,  si);
39            I(gi2p ,  di) <+ igd12db + gmin * V(gi2p ,  di);
40        end
41    end
42 end

```

5.6 Schottky p-GaN Module

The p-GaN module is an addition in **V3.2.0 official release** with major improvements in **V4.0.0 official release**. Schottky-type p-GaN gate is widely employed to achieve low-leakage enhancement mode ($V_{t0} > 0$) GaN HEMT power devices. The physical structure of p-GaN gate stack is fundamental to device construction and has prominent impacts on both

static DCIV and transient switching behavior. [11]

An illustration of the charge storage behavior of p-doped GaN layer is shown in Fig. 16 which shows a cross section of a p-GaN HEMT in both off and on states. During the off state, electrons are able to move from the metal gate to the p-doped GaN through the forward current of the Schottky barrier. However, during the on state, these electrons are unable to move back to the metal gate, which effectively reduces the gate overdrive voltage and reduces p-GaN HEMT turn on and thus channel current. After some time, these electrons are able to leak through the Schottky barriers, however for fast switching in power converters, there is insufficient time for this to occur.

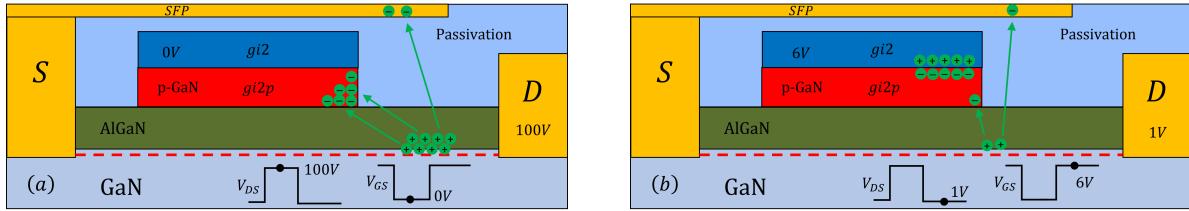


Figure 16: Illustration of charge distribution for p-GaN HEMT during off (a) and on (b) conditions. The p-GaN region acts like a floating node where electrons are trapped by the Schottky barrier on either side. As a result, during dynamic switching operation, the effective threshold voltage shifts.

As the p-doped GaN gate is present, the channel is no longer directly controlled by the metal gate terminal, but is controlled by the voltage on the p-doped GaN layer. At steady state, the voltage on the p-GaN layer is not equal to the metal gate, but is determined by the voltage division between the gate and other terminals of the device. This results in a threshold voltage shift. Additionally, as there is a junction capacitance between the metal gate and p-doped GaN, dynamic effects are also present, including dynamic threshold voltage shifts.

5.6.1 Module Implementation

The p-doped GaN (**gi2p** node) will form a Schottky junction with the gate metal which is modeled as D_{sch} in Figure 17. Dynamic effects are modeled by a voltage dependent junction capacitance (C_{sch}). [12] Hybrid/Ohmic p-GaN which is proposed to improve static/dynamic behavior can be modeled with a resistor (R_{sch}) with the parameters $rsch0$ & $ohmicratio$.

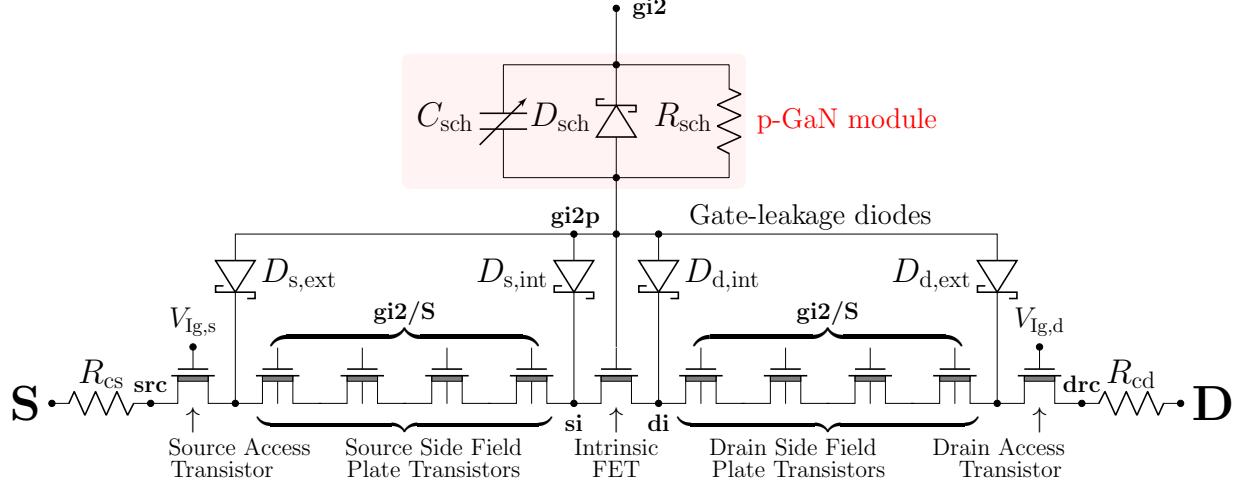


Figure 17: Partial MVSG Schematic showing the p-GaN module in red inserted between the distributed gate resistance (above **gi2**) and internal gate node (**gi2p**). When the p-GaN module is disabled (*flagpgan*=0), **gi2** and **gi2p** are collapsed.

By default, for depletion-mode and/or high frequency devices, *flagpgan*=0, which turns off the p-GaN Module and collapses the **gi2** and **gi2p** nodes. Gate FPs always connect to the outer **gi2** node, as the p-GaN gate stack only applies to the intrinsic FET.

The junction diode D_{sch} uses the same ***calc_ig*** (5.5.4) function that the gate diodes use, with most of the features including forward mode current with high injection effects, primary and secondary reverse recombination with voltage saturation. Breakdown and bandgap dependence is omitted.

The equations for D_{sch} are shown in (37, 38). Just like the gate diodes (5.5), the total D_{sch} current is the sum of the forward and reverse components. The high injection formulation is not shown for the p-GaN diode, but operates the exact same way as the gate diodes in (28–32). A secondary reverse reverse recombination current with the same formulation as (38, 39) but with a different parameter set can be enabled by setting *pganrecmod*=1. $i_{j,\text{pgan}}$ and $i_{\text{rec},\text{pgan}}$ are the forward and reverse mode saturation currents respectively. $p_{g,\text{param},\text{pgan}}$ and $p_{g,\text{rec},\text{pgan}}$ are the inverse ideality factors. T is the device temperature, T_0 is the nominal temperature (value of *t_{nom}* parameter in K), *egate* is the diode temperature factor which has a value of 3.0. φ_t is the thermal voltage. The voltage across the diode is given by $V_{\text{gi2p,gi2}}$. When high injection is activated, *vgsat_pg* controls the onset of high injection, *frac_pg* controls the fractional change in the inverse ideality factor, and *alphag_pg* controls the smoothing. *vgsatq_pg* and *betarec_pg* are parameters used to control the reverse recombination voltage saturation, identical to (36) in the gate current.

$$I_{F,\text{dsch}} = W(1.0 - (\text{ohmicratio}))n_{\text{gf}} i_{j,\text{pgan}} \left(\frac{T}{T_0}\right)^{\text{egate}} \left(\exp\left(\frac{p_{g,\text{param},\text{pgan}} V_{\text{gi2p,gi2}}}{\varphi_t}\right) - 1\right) \quad (37)$$

$$I_{R,\text{dsch}} = -W(1.0 - (\text{ohmicratio}))n_{\text{gf}} i_{\text{rec},\text{pgan}} \left(\frac{T}{T_0}\right)^{\text{egate}} \left(\exp\left(\frac{p_{g,\text{rec},\text{pgan}} F_{\text{rec},\text{pgan}}}{\varphi_t}\right) - 1\right) \quad (38)$$

where $F_{\text{rec,pgan}}$ is the reverse voltage across the D_{sch} diode accounting for saturation and is given by

$$F_{\text{rec,pgan}} = \frac{-V_{\text{gi2p,gi2}}}{\left(1 + \left|\frac{V_{\text{gi2p,gi2}}}{V_{\text{gsatq,pgan}}}\right|^{\beta_{\text{rec,pgan}}}\right)^{\frac{1}{\beta_{\text{rec,pgan}}}}} \quad (39)$$

The charge stored on the junction capacitor C_{sch} is not linear with respect to bias, and is given by (40). The capacitance of C_{sch} can be determined by taking the derivative of the charge with respect to the voltage across it and is given by (41). This equation shows that C_{sch} follows a typical Schottky junction capacitance equation, where the capacitance follows a inverse square root relationship as the D_{sch} diode becomes further reverse biased. $csh0$ is the zero bias Schottky junction capacitance & $vcsh0$ is the built in potential of the Schottky junction.

$$Q_{\text{sch}} = 2.0C_{\text{sh0}}W(1.0 - (\text{ohmicratio}))n_{\text{gf}}V_{\text{csh0}} \left(1.0 - \sqrt{1.0 - \frac{V_{\text{gi2p,gi2}}}{V_{\text{csh0}}}}\right) \quad (40)$$

$$C_{\text{sch}} = \frac{\partial Q_{\text{sch}}}{\partial V_{\text{gi2p,gi2}}} = C_{\text{sh0}}W(1.0 - (\text{ohmicratio}))n_{\text{gf}} \frac{1}{\sqrt{1.0 - \frac{V_{\text{gi2p,gi2}}}{V_{\text{csh0}}}}} \quad (41)$$

It is important to note that (40) becomes undefined when the voltage across D_{sch} (and hence C_{sch}) exceeds the built in potential. When this happens, the depletion width approaches zero, and the capacitance predicted by (41) approaches infinity. To prevent this, two parameters, fc & $pgancshorder$ are used to correct this. fc controls the fractional change in voltage across p-GaN between 0 and $vcsh0$ before a Taylor series is used to represent the charge which can be set within $[0, 1]$. $pgancshorder$ is used to control the order of the Taylor series which can be set to an integer between 0 and 5. Since $pgancshorder$ control the Taylor series order for the charge, it is recommended to set it to at least 2, so the capacitance is linear and differentiable once. The formulation for Schottky junction capacitor C_{sch} including the Taylor series expansion is shown in (42). The full expansion of the Taylor series can be inferred from the code.

$$Q_{\text{sch}}^{\dagger} = \begin{cases} Q_{\text{sch}} & \text{if } V_{\text{gi2p,gi2}} \leq fc * vcsh0 \\ \sum_{n=0}^{(\text{pgancshorder})} \frac{Q_{\text{sch}}^{(n)}(fc * vcsh0)}{n!} (V_{\text{gi2p,gi2}} - fc * vcsh0)^n & \text{if } V_{\text{gi2p,gi2}} > fc * vcsh0 \end{cases} \quad (42)$$

The p-GaN junction may be intentionally leaked with an ohmic junction to yield a hybrid device in order to exhibit better channel control, while having minimal effect on gate leakage. The p-GaN module supports this through the parameters $rsch0$ & $ohmicratio$. $rsch0$ is the unit width resistance, and $ohmicratio$ is the fraction of the gate stack that is ohmic. If $ohmicratio$ is increased beyond its default value of 0, the effective width of D_{sch} & C_{sch} are reduced as shown in (37,38,40,41). The behavior is implemented with resistor R_{sch} shown in Fig. 17 with the mathematical model in (43).

$$R_{\text{sch}} = \begin{cases} \frac{r_{\text{sch0}}}{W(\text{ohmicratio})n_{\text{gf}}} & \text{if } r_{\text{sch0}} > 0 \\ \infty & \text{if } r_{\text{sch0}} = 0 \end{cases} \quad (43)$$

The implementation of the p-GaN module in the Verilog-A code is shown below.

Schottky p-GaN Module Implementation including function call to *calc_ig*

```

1 if (flagpgan == 1) begin
2     vsch          = type * V(gi2p, gi2);
3     idsch         = calc_ig(idschsat, idschrec, vsch, phit, vgsat_pgan,
4                               alphag_pgan, frac_pgan, pg_param_pgan, 4.0, 600.0, tfacdiode, w * (1.0-
5                               ohmicratio), ngf, ij_pgan, 0.0, vgsatq_pgan, betarec_pgan, irec_pgan, pgsrec_pgan
6                               , 0.0, 0.0, type);
7     I(gi2p, gi2) <+ idsch + gmin * V(gi2p, gi2);
8     if (pganrecmod == 1) begin
9         idsch2       = calc_ig(idschsat2, idschrec2, vsch, phit
10                           , 1.0, 10.0, 1.0, 0.0, 4.0, 600.0, tfacdiode, w * (1.0-ohmicratio), ngf, 0.0, 0.0,
11                           vgsatq_pgan2, betarec_pgan2, irec_pgan2, pgsrec_pgan2, 0.0, 0.0, type);
12         I(gi2p, gi2) <+ idsch2 + gmin * V(gi2p, gi2);
13     end
14     if (vsch <= fc * vcsh0) begin
15         qsch          = type * 2.0 * csh0 * w * (1.0-ohmicratio) * ngf * vcsh0 *
16         ( 1.0 - sqrt( 1.0 - vsch/vcsh0 ) );
17     end else begin
18         qsch0        = 1.0 - sqrt( 1.0 - fc );
19         if (pgancshorder >= 1) begin
20             qsch1c      = 1.0 / ( 2.0 * vcsh0 * sqrt(1.0-fc) );
21             vschfc1    = vsch - fc * vcsh0;
22             qsch1      = qsch1c * vschfc1;
23             if (pgancshorder >= 2) begin
24                 qsch2c      = qsch1c / ( 4.0 * vcsh0 * (1.0-fc) );
25                 vschfc2    = vschfc1 * vschfc1;
26                 qsch2      = qsch2c * vschfc2;
27                 if (pgancshorder >= 3) begin
28                     qsch3c      = qsch2c / ( 2.0 * vcsh0 * (1.0-fc) );
29                     vschfc3    = vschfc2 * vschfc1;
30                     qsch3      = qsch3c * vschfc3;
31                     if (pgancshorder >= 4) begin
32                         qsch4c      = 5.0 * qsch3c / ( 8.0 * vcsh0 * (1.0-fc) );
33                         vschfc4    = vschfc3 * vschfc1;
34                         qsch4      = qsch4c * vschfc4;
35                         if (pgancshorder >= 5) begin
36                             qsch5c      = 7.0 * qsch4c / ( 10.0 * vcsh0 * (1.0-fc
37                             ) );
38                             vschfc5    = vschfc4 * vschfc1;
39                             qsch5      = qsch5c * vschfc5;
40                         end else begin
41                             qsch5c      = 0;
42                         end
43                     end else begin
44                         qsch4c      = 0;
45                     end
46                 end else begin
47                     qsch3c      = 0;
48                 end
49             end else begin
50                 qsch2c      = 0;
51             end
52         end else begin
53             qsch2c      = 0;
54         end
55     end
56 
```

```

45      end else begin
46          qsch1c = 0;
47      end
48      qsch      = type * 2.0 * csh0 * w * (1.0-ohmicratio) * ngf * vcsch0 *
49      ( qsch0 + qsch1 + qsch2 + qsch3 + qsch4 + qsch5 );
50  end
51  I(gi2p,gi2) <+ ddt(qsch);
52  if (rsch0 !=0 && ohmicratio != 0) begin
53      rsch      = rsch0 / ( w * ohmicratio * ngf );
54      I(gi2p,gi2) <+ V(gi2p,gi2) / rsch;
55  end
56 end else begin
57     V(gi2,gi2p) <+ 0;

```

5.6.2 p-GaN Module Simulation Results

Several simulations were performed using the p-GaN module to benchmark performance metrics. In Fig. 18, terminal currents and the internal p-GaN voltage ($V_{\text{gi}2p}$) both with and without the p-GaN module (by setting *flagpgan* to 1 and 0) are shown. With the p-GaN module disabled, the internal p-GaN voltage follows the gate voltage V_G exactly, and the drain current is high. With the p-GaN module enabled, the internal p-GaN voltage follows the gate voltage until the gate diodes ($D_{s,\{\text{int,ext}\}}$ and $D_{d,\{\text{int,ext}\}}$ in Fig. 17) reaches their knee voltage and become highly conductive. As the junction diode D_{SH} is still in reverse mode and highly resistive, the p-GaN voltage is hindered from following the gate voltage closely. The corresponding drain current I_D is also lowered significantly as channel turn on is reduced. The gate current is also reduced as it is limited by the reverse mode current of the p-GaN diode (D_{sch}).

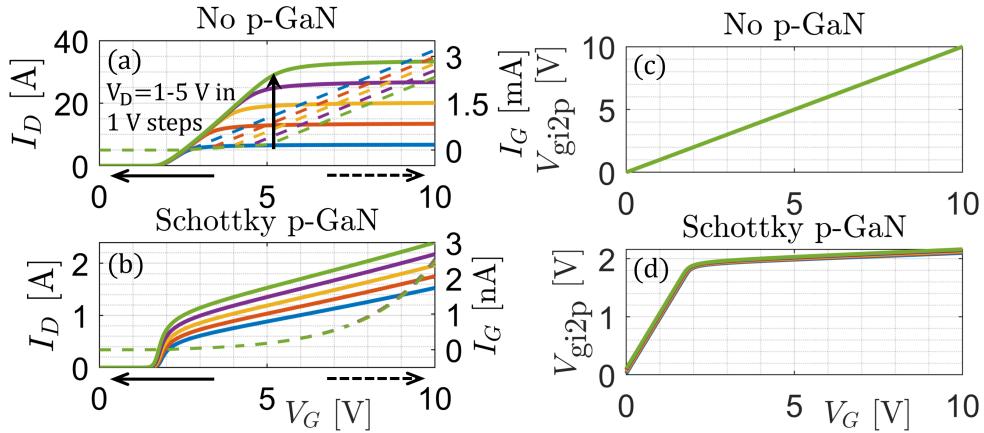


Figure 18: Drain current (I_D), Gate current (I_G), and p-GaN voltage ($V_{\text{gi}2p}$) simulations with and without the p-GaN module.

A single pulse test is shown in Fig. 19, where V_D switches from 0 V to 1 V, while V_G switches from 0 V to various $V_{G,\text{final}}$ values. The dynamic effect due to the gate and junction

capacitances is captured, where a significant amount of time is needed for $V_{\text{gi}2\text{p}}$ and I_D to settle to DC values determined by the gate and junction diodes. This transient data is used to produce transfer curves at different t_{ext} values, showing the transition of device turn on being capacitance-dominated to diode-dominated.

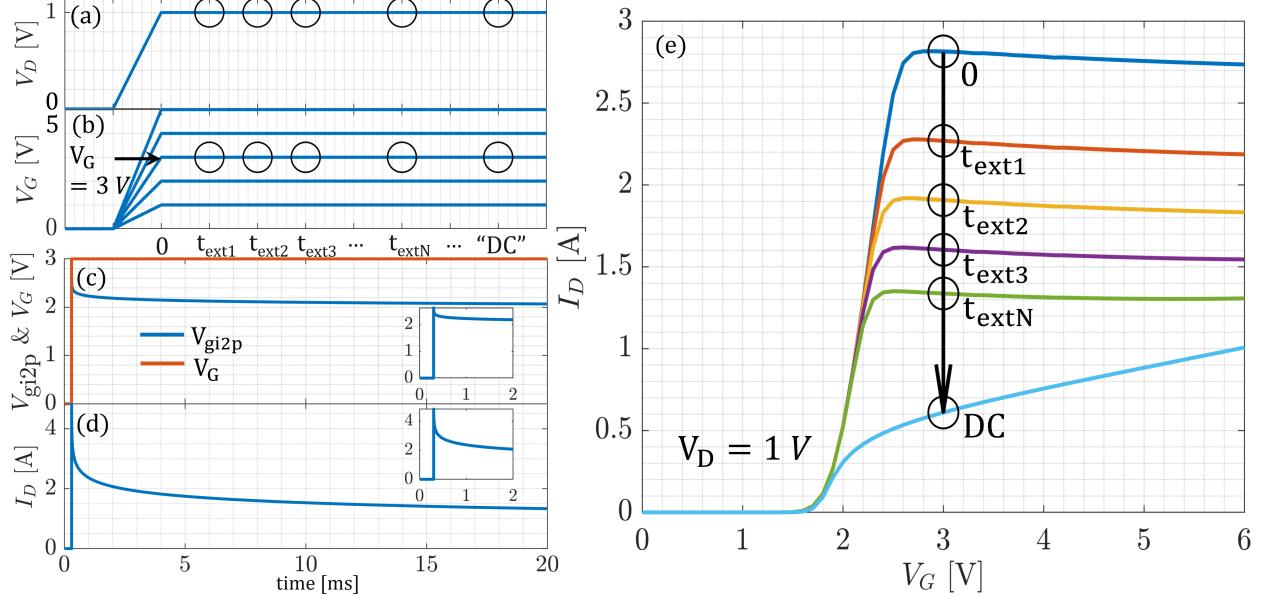


Figure 19: (a,b) Single pulse test setup. (c,d) Transient response of $V_{G,\text{final}} = 3$ V. (e) Transfer (I_D - V_G) curves at various t_{ext} values. Transient simulation with $V_{G,\text{final}} = 3$ V is annotated for illustrative purpose.

5.7 Charge Trapping Effects

Earlier versions of MVSG had a simple trapping module to mimic the effect of $R_{\text{DS},\text{On}}$ (on-resistance) increase (knee walkout) with charge-trapping: the drain access-region resistance was increased under switching scenarios. The extent of $R_{\text{DS},\text{On}}$ shift was determined by bias (V_{DG}) and frequency dependence was achieved via a simple RC-subcircuit (with only one time constant for both trapping and de-trapping). Details of this implementation are highlighted in Fig. 20. This model (5.7.1) is selectable by *trapselect*=1 in order to maintain backward compatibility.

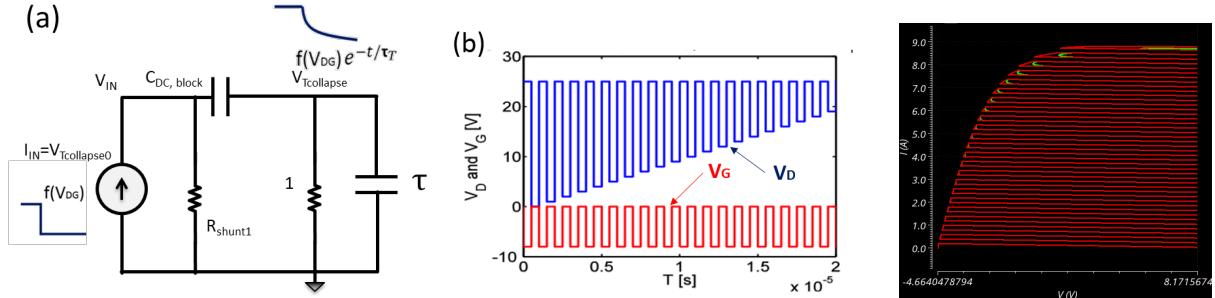


Figure 20: (a) The RC-time constant that models the charge de-trapping time-constant (τ_T) and whose input function ($f(V_{DG})$) is a temperature and field-dependent step-function as shown and output is a decaying function that can increase the sheet resistance (R_{sh}) of the drain access region (b) Typical gate- and drain-switching waveforms that mimic the Auriga-pulsed-IV setup. The drain is switched from high-value in quiescent-state to low-value in non-quiescent-state. The gate is switched correspondingly from off-quiescent-state to on-state as shown. Resulting pulsed output curves show increased $R_{DS,On}$ in trapped-IV (green) compared to nominal IV (red).

The current trapping module (5.7.2, selected with *trapselect=2*) is reworked to include realistic drain-lag and gate-lag effects observed in measurements. Both observed drain-voltage and gate-voltage dependence are included via separate sub-circuits. Both capture and emission time constants are considered via diode-R-C based implementations. Temperature dependence is added as well.

In summary, selection between different trapping models can be done through a flag: *trapselect*. By default, *trapselect=0* which turns off trapping module. Setting *trapselect=1* selects the $R_{DS,On}$ increase model (older trapping model) and setting *trapselect=2* selects the latest drain-/gate-lag model implemented in V.3.1.0.

5.7.1 Trapping Model Modulating $R_{DS,On}$ (*trapselect=1*)

The dynamic current collapse effect in GaN HEMTs resulting in higher knee voltage, lower on-currents under switching conditions is well known [2]. The knee-walk out effect is accounted for in MVSG by increasing the sheet resistance/threshold voltage of drain-side access region dynamically through a trap-time constant. A single RC trap time constant is chosen for fitting frequency dependence in specific industry measurement data as trapping and de-trapping time constants cannot be separated from this set of available data.

$$V_{tcollapse0} = (\text{trapfac}) \times \left(\alpha_{t1} V_{DG} + \left(\exp \frac{V_{DG} - (\text{vttrap}) - \alpha_{t3} V_{IN}}{\alpha_{t2}} \right) \right) \quad (44)$$

This is the source function for charge trapping which has the requisite bias and temperature dependence. Beyond *vttrap*, the trapping effect is exponential as seen from the measurement data. This is fed into the RC network with time constant (τ_t). The resulting $V_{tcollapse}$ function from the RC network is fed to the sheet resistance (R_{sh}) of the drain access region which increases the knee-voltage and lowers the on-currents only under switching conditions when $V_{tcollapse}$ is non-zero.

The shunt-resistance ($R_{\text{shunt}1}$) of large-value is to avoid build-up on V_{IN} and associated convergence issues in DC-simulations. Further, in order to avoid the exponential function in (44) from blowing-up, a feedback term ($\alpha_{t3}V_{IN}$) is added in the exponent. This requires an additional parameter (α_{t3}) but saturates the effect of trapping for large $V_{DG} \gg vttrap$. The default model-parameter set in the Verilog-A code converges in DC and transient switching simulations.

Older trapping module (modulating $R_{DS,On}$) implementation in Verilog-A code ($trapselect=1$)

```

1 if ( trapselect == 1) begin
2   V(dtrapin)      <+0;
3   V(dtrapin2)     <+0;
4   V(dtrapin3)     <+0;
5   V(gtrapin)      <+0;
6   V(gtrapin2)     <+0;
7   V(gtrapin3)     <+0;
8   // Rsh degradation with trapping
9   vtcollapse0 = alphat1 * abs(V(d,g)) + explim( (V(d,g) - vttrap - V(tr1)
10 ) * alphat3) / alphat2 );
11   I(tr1)          <+ -vtcollapse0 ;
12   I(tr1)          <+ V(tr1)/rintrap1 ;
13   I(tr1,tr)        <+ ddt(ctrap * V(tr1,tr));
14   I(tr)            <+ ddt(taut * V(tr));
15   I(tr)            <+ V(tr);
16   vtcollapse       = V(tr);
17   drsht           = 1.0 + ( vtcollapse ) * ttrapfac ;

```

5.7.2 Gate-lag/drain-lag Trapping Model ($trapselect=2$)

Pulsed IV-measurements typically done on RF-GaN devices pulse both V_D and V_G from their quiescent bias-conditions to non-quiescent stress values. Typical pulsed IV curves appear as shown in Fig. 21 (Measurements shared by Raytheon Inc.). While the devices do not show significant threshold voltage shifts, we see both a degradation in $R_{DS,On}$, $V_{D,SAT}$ (Knee voltage) and $I_{D,SAT}$ (saturation current) values. To better describing these effects, a second trapping model was implemented in **V3.1.0** accounting for both gate-lag and drain-lag processes, with separate time constants for emission/capture and temperature coefficients up to the second order.

It is well known that the trap-states in the buffer/heterostructure cause an overall reduction in 2DEG charge post-stress and it takes a finite time after the voltage stress removal to re-gain the 2DEG charge. Representative time-domain plots of I_D in a switching transition is shown in Fig. 22 which show this effect clearly as a function of both drain-pulsing and gate-pulsing. The emission time-scales are in general different from capture time-scales and are accounted in MVSG model.

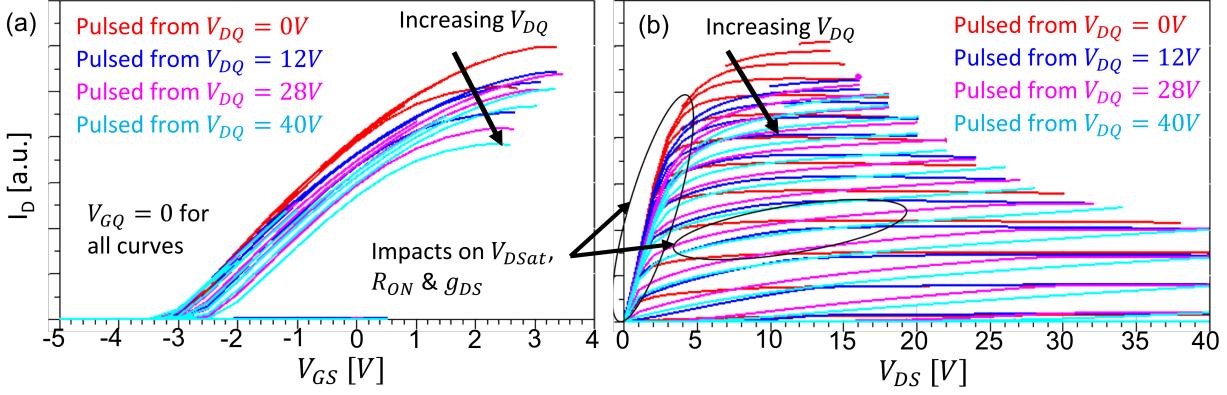


Figure 21: (a) $I_D - V_G$ and (b) $I_D - V_D$ pulsed IV plots showing bias-dependence on $I_{D,SAT}$, V_{DSAT} , $R_{DS,On}$ and threshold voltage shifts associated with trapping in a typical GaN-HEMT. MVSG model captures this effect by modulating the intrinsic transistor channel-charge as a function of dynamic switching voltages, including their temperature and time-dependence. Courtesy: Raytheon Inc.

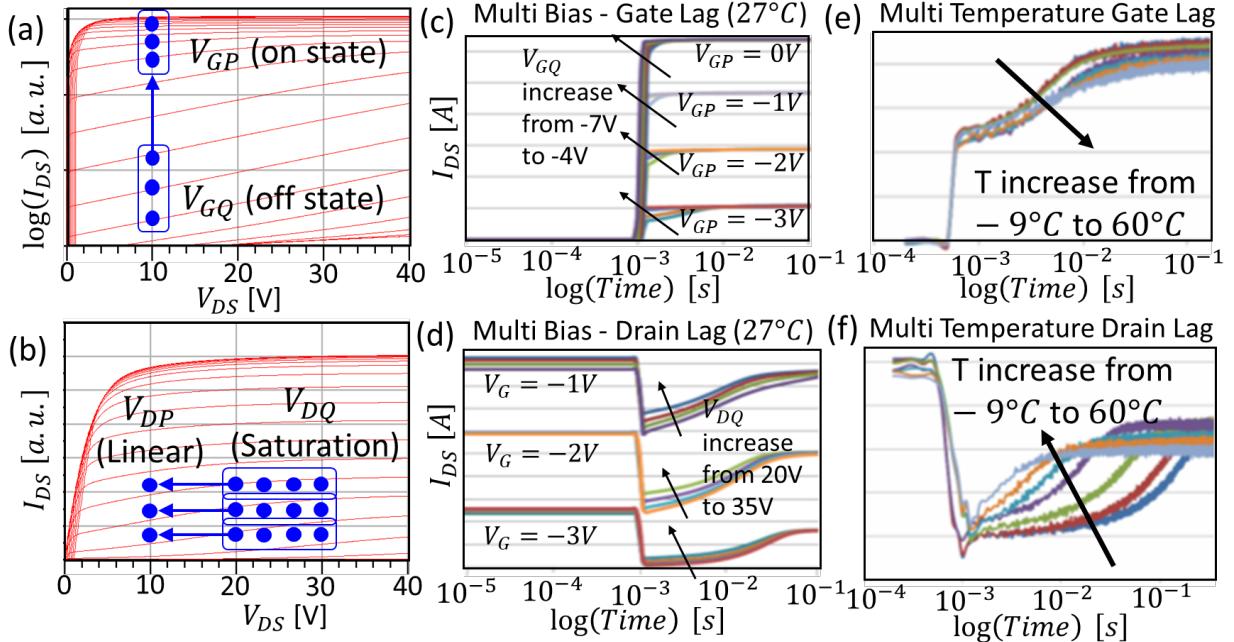
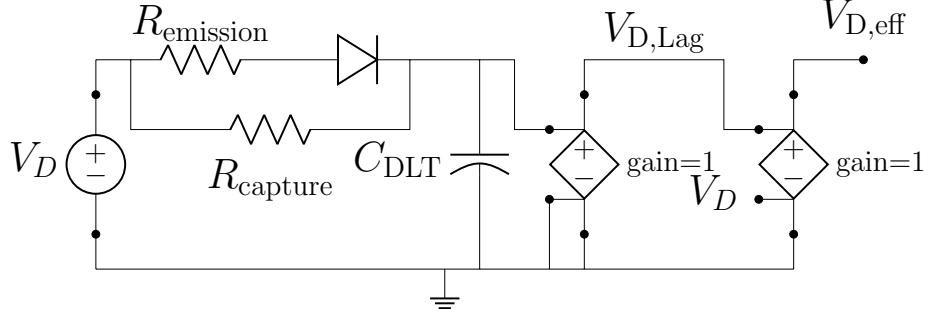


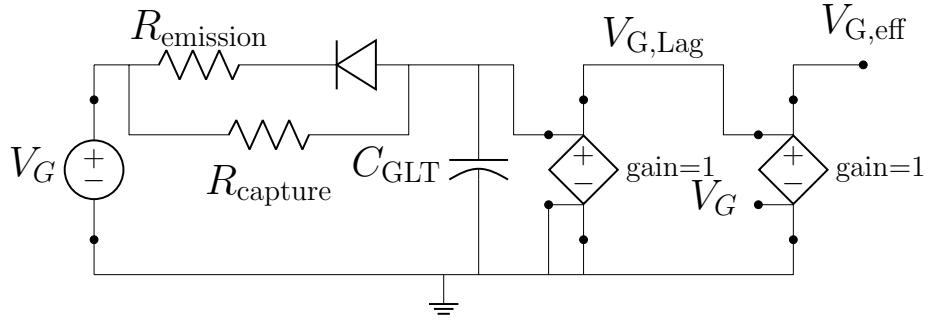
Figure 22: (a) Gate-lag pulsing and (b) Drain-lag pulsing conditions and resulting time-domain waveforms vs. bias and temperature are shown. Slow-recovery in I_D post off-state stress is associated with charge-trapping effects. Temperature dependence of I_D recovery is also shown. It seems that the emission time-constant reduces with temperature for gate-pulsing while it increases with temperature for drain-lag. Latest MVSG trapping module is able to re-create the observed behavior in large-signal switching simulations. Courtesy: Raytheon Inc.

The sub-circuits for drain-lag and gate-lag implemented within Verilog-A MVSG model

are shown in Fig. 23. V_D and V_G are inputs to each sub-circuit and are modified with a delay to mimic the trapping “stress-functions” $V_{D,\text{Lag}}$ and $V_{G,\text{Lag}}$ as shown. These act as bias-dependent stress functions that modulate the channel charge under switching conditions to mimic charge-trapping effect.



(a) Drain-lag sub-circuit schematic incorporated within the Verilog-A MVSG model



(b) Gate-lag sub-circuit schematic incorporated within the Verilog-A MVSG model

Figure 23: The sub-circuits have (a) Drain-voltage and (b) Gate-voltage inputs respectively. The RC elements cause a delay that is determined by the switching polarity of the input pulse to yield different time-constants for device stressing and de-stressing. The output voltage is used to module the channel-currents and charges to mimic trapping effects.

Further, each sub-circuit yields two time-constants: Emission time-constant (τ_{emission}) and capture time-constant (τ_{capture}) implemented through two parallel resistor branches in an RC network as shown in the figure. Directionality is introduced by adding an ideal series diode on one of the resistance branches. The saturation current of these diodes is controlled by the parameter $isat$.

The input-voltage for the {drain/gate}-lag sub-circuit is $\{V_D/V_G\}$. Input-voltage transition from low-to-high on V_{DS} or high-to-low on V_{GS} corresponds to stressing the device, while the opposite is de-stressing. The diode is forward-biased in the stressing scenario yielding RC time constant $\tau_{\text{emission}} \approx (R_{\text{emission}}||R_{\text{capture}})C_{\{D/G\}\text{LT}} \approx R_{\text{emission}}C_{\{D/G\}\text{LT}}$. For device de-stressing, the diode is reverse-biased in this transition yielding RC time constant $\tau_{\text{capture}} \approx R_{\text{capture}}C_{\{D/G\}\text{LT}}$. The output voltage of these sub-circuits are $V_{D,\text{eff}}$ and $V_{G,\text{eff}}$, which are inputs to (45) of trapping module. [10]

It is recommended to set the capacitance values in these trapping sub-circuits in the pF to μF range as larger values tend to cause convergence issues. Typically, τ_{capture} is in the 100 μs range, while τ_{emission} is faster, in the ns range. For nomenclature considerations, it

should be noted that capture and emission are referring to positively charged holes, rather than electrons.

$$Q_{\text{frac},d} = \frac{|V_{D,\text{eff}}|}{V_{\text{DLtrapth}}} \quad , \quad Q_{\text{frac},g} = \frac{|V_{G,\text{eff}}|}{V_{\text{GLtrapth}}} \quad (45)$$

Here, V_{DLtrapth} and V_{GLtrapth} are input parameters which capture the threshold drain-/gate-stress voltage values. Trapping is significant when switching stress exceeds these threshold voltages. The values from (45) reduce channel charge by a factor (Q_{frac}) given by:

$$Q_{\text{frac}} = \frac{1}{1 + Q_{\text{frac},d} + Q_{\text{frac},g}} \quad (46)$$

The intrinsic transistor current and gate-charges are then modulated by this factor as:

$$I_{\text{DSi}} = Q_{\text{frac}} I_{\text{DSi}0} \quad , \quad Q_{\{\text{GSi}, \text{GDi}, \text{GSUBi}\}} = Q_{\text{frac}} Q_{\{\text{GSi}0, \text{GDi}0, \text{GSUBi}0\}} \quad (47)$$

Where the currents and charges on the right of (47) with a subscript (0) are unstressed values that get reduced by Q_{frac} .

Temperature dependence of the charge trapping module is explained in Section 5.7.3.

Latest trapping module implementation in Verilog-A code (*trapselect=2*)

```

1 end else if ( trapselect == 2 ) begin
2   V(tr1)           <+0;
3   V(tr)            <+0;
4   // Drain-lag block
5   V(dtrapin)      <+ type * V(d,s);
6   vdlinput        = V(dtrapin);
7   vdloutput       = V(dtrapin2);
8   I(dtrapin3, dtrapin2)<+ isat * ( explim(V(dtrapin3, dtrapin2)/phit) - 1.0
9   );
10  I(dtrapin, dtrapin3) <+ V(dtrapin, dtrapin3) / remission;
11  I(dtrapin, dtrapin2) <+ V(dtrapin, dtrapin2) / rcapture;
12  I(dtrapin2)        <+ cdglag * ddt(vdloutput) * ( 1.0 + rct1dl * ( tdut -
13    tnomk ) + rct2dl * ( tdut - tnomk ) * ( tdut - tnomk ) );
14  chargefracd       = abs(vdloutput - vdlinput) / vdltrapth;
15  // Gate-lag block
16  V(gtrapin)        <+ type * V(g,s);
17  vglinput         = V(gtrapin);
18  vgloutput        = V(gtrapin2);
19  I(gtrapin2, gtrapin3)<+ isat * ( explim(V(gtrapin2, gtrapin3)/phit) - 1.0
20   );
21  I(gtrapin, gtrapin3) <+ V(gtrapin, gtrapin3) / remission;
22  I(gtrapin, gtrapin2) <+ V(gtrapin, gtrapin2) / rcapture;
23  I(gtrapin2)        <+ cdglag * ddt(vgloutput) * ( 1.0 + rct1gl * ( tdut -
24    tnomk ) + rct2gl * ( tdut - tnomk ) * ( tdut - tnomk ) );
25  chargefracg       = abs(vgloutput - vglinput) / vgltrapth;
26  chargefrac        = 1.0 / (1.0 + chargefracd + chargefracg);
27
28 //Function call to include trapping in intrinsic-TX current and charges
29 ids = calc_iq(ids, qgs, qgd, qc, qb, qs, vtdibli, vdsat1i, vgsi, vdsi, 0, 0, 0, 0, 0, tdut,
30   tnomk, phit, w, l, cgt, 0, 0, 0, vto, ss, delta1, delta2, nd, alpha, vx0, mu0, beta, mtheta,
31   vtheta, vtzeta, dibsat, epsilon, vzeta, lambda, ngf, type, chargefrac);

```

It should be noted that the charge-trapping module is activated only for intrinsic transistor. The same trapping module can also be engaged with field-plated and access-transistor regions in future MVSG model releases. The function calls to currents and charges (`calc_iq`) for these additional transistors have Q_{frac} set to 1 (no charge-trapping induced current/charge reduction) but can be changed to a value set by the trapping function by modifying the Verilog-A code.

5.7.3 Switching Simulation Results ($\text{trapselect}=2$)

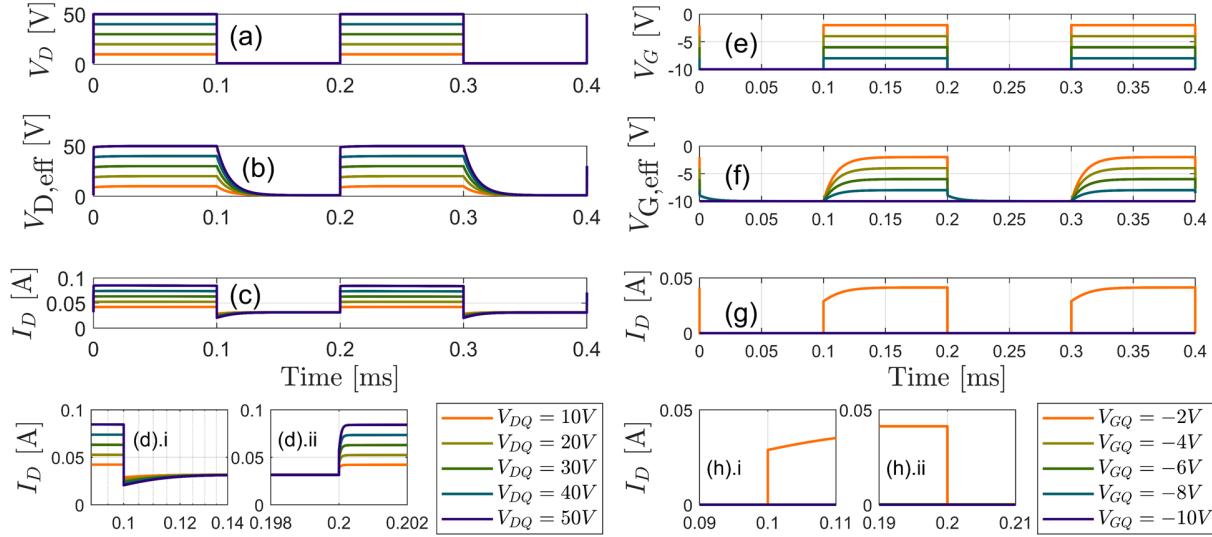


Figure 24: Transient simulation results of MVSG model of (a-d) Drain-pulsing and (e-h) Gate-pulsing with $\text{trapselect}=2$. The gate-/drain-stress functions and resulting current profiles show slow recovery during de-stressing. I_D recovery mimics the behavior observed in measurements of Fig. 22.

Transient drain and gate pulsing simulations are shown in Fig. 24. Drain-pulsing simulations in Fig. 24(a-d) with the device switched from various off state V_{DQ} (10 V to 50 V), to the same on state V_{DP} (10 V), shows I_D lower than the DC value once the device is turned back on. Gate-pulsing from various off state V_{GQ} (-2 V to -10 V) values to the same on state V_{GP} (-10 V) are shown in Fig. 24(e-h), revealing the bias-dependency on I_D trapping and recovery. It takes time (τ_{capture}) for the current to recover to its DC-value. Setting $\text{trapselect}=0$ will show I_D following V_D pulses without any delay. Note that the simulations have R_{th} set to 0 (which is why $I_D(V_D = 50 \text{ V}) > I_D(V_D = 10 \text{ V})$).

Linear ($rct1\{d/g\}l$) and quadratic ($rct2\{d/g\}l$) temperature coefficients are added to the capacitance element of the RC sub-circuits of Fig. 23 as in (48). A simulation showing temperature dependence is presented in Fig. 25. In this particular simulation, there is negative temperature coefficient for drain-lag and positive temperature coefficient for gate-lag. MVSG is able to handle positive and negative linear and quadratic temperature coefficients for both drain and gate lag.

$$C_{\text{DLT}} = C_{\text{dglag}} \left(1.0 + (\text{rct1dl})(T_{\text{DUT}} - T_{\text{NOM}}) + (\text{rct2dl})(T_{\text{DUT}} - T_{\text{NOM}})^2 \right) \quad (48\text{a})$$

$$C_{\text{GLT}} = C_{\text{dglag}} \left(1.0 + (\text{rct1gl})(T_{\text{DUT}} - T_{\text{NOM}}) + (\text{rct2gl})(T_{\text{DUT}} - T_{\text{NOM}})^2 \right) \quad (48\text{b})$$

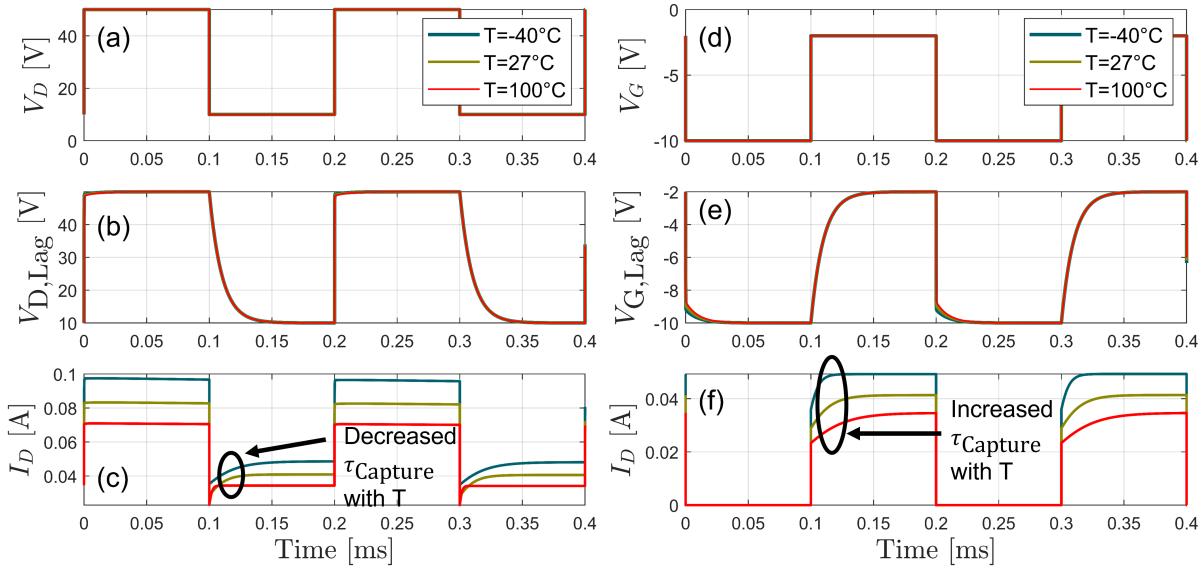


Figure 25: Temperature-dependence is added to the trapping and de-trapping time constants and are shown in switching simulations at -40°C , 27°C , & 100°C . In this simulation, τ_{capture} for drain-lag shows negative temperature coefficient while it shows positive temperature coefficient for gate-lag.

5.8 Device-Noise: RF and Phase Noise Model

Device-noise in GaN-HEMTs impact the noise-figure of amplifiers built using these devices which are especially critical for the design of low noise amplifiers (LNA) at the receiver stage and the low frequency noise of the device impacts the phase-noise and skirting characteristics of the oscillators built in this technology for the VCOs also at the receiver-stage. The noise sources are hence of two variants: The RF-white noise associated with the device-level-noise sources and low-frequency noise sources associated with charge-states in the device, both of which are explained in this section along with the MVSG modeling approach to capture them.

5.8.1 RF-Device Noise

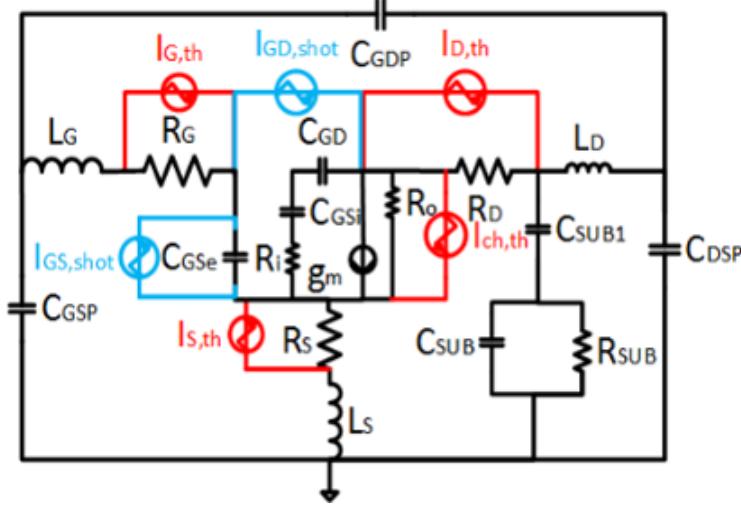


Figure 26: The full-equivalent-circuit of GaN-HEMTs that includes the various RF-noise sources that contribute to the device-noise-figure and are part of the MVSG-model

The white-noise sources present in GaN-HEMTs are highlighted in the small-signal equivalent circuit of Fig. 26 and are of two types, namely: the thermal-noise linked with various resistive elements of the device and the shot-noise sources linked to the Schottky-barriers of gate-source and gate-drain junctions. The noise-power-spectral-density linked to the parasitic-resistances are given by the Johnson-Nyquist thermal noise formulation:

$$I_{S,th}^2 = \frac{4kT}{R_S} \quad ; \quad I_{D,th}^2 = \frac{4kT}{R_D} \quad ; \quad I_{G,th}^2 = \frac{4kT}{R_G} \quad (49)$$

where k is the Boltzmann constant and the resistances are extracted from S-parameter measurements. Unlike the resistive thermal-noise, the thermal-noise linked to the device-channel is bias-dependent and is a modified-formulation of the device-channel-noise given in [13] as follows:

$$I_{ch,th}^2 = 4kTg_m\Gamma \quad (50)$$

where g_m is the small-signal-transconductance and output-conductance which are bias-dependent, and Γ is given by:

$$\Gamma = \frac{Q_G}{Wn_{gf}LC_{inv}} \quad (51)$$

with $Q_G = Q_{inv}$ given by (20). Γ transforms from 1 in the linear-regime to the factor of 2/3 in saturation as required by conventional channel-thermal noise models. Moreover, this approach enables the channel-thermal-noise in the linear-regime to be caused by the channel-resistance at and in saturation. It is to be noted that none of the thermal-noise sources in the model need additional parameters since they are based on DC, AC and small-signal model-parameters which are already described in previous sections. The second category of

white-noise sources are the shot-noise sources associated with gate Schottky diodes and are modeled as follows (with current saturation values from 5.5.1 and 5.5.2):

$$I_{GS,\text{shot}}^2 = 2q(\text{shs}) \left| \left(I_{GS} + 2 \left(Wn_{\text{gf}} I_{\text{Fg}\{\text{s/d}\}} e^{-\frac{\varphi_B}{\eta\varphi_T}} - Wn_{\text{gf}} I_{\text{Rg}\{\text{s/d}\}} \right) \right) \right| \quad (52)$$

$$I_{GD,\text{shot}}^2 = 2q(\text{shd}) \left| \left(I_{GD} + 2 \left(Wn_{\text{gf}} I_{\text{Fg}\{\text{d/s}\}} e^{-\frac{\varphi_B}{\eta\varphi_T}} - Wn_{\text{gf}} I_{\text{Rg}\{\text{d/s}\}} \right) \right) \right| \quad (53)$$

This formalism is consistent with the approach taken in [13] and reduces to the conventional $2qI$ limit in forward-active mode where I is the gate-source (I_{GS}) or gate-drain (I_{GD}) current. The second terms in the parentheses in the above equations are the reverse-saturation currents ($I_{\text{Fg}\{\text{s/d}\}}^2$) of the diodes. At large-reverse-bias, the model formulation reduces to $2qI_{\text{Fg}\{\text{s/d}\}}$. At zero-voltage across the diodes, the Nyquist-limit of the shot-noise-source is $4kTg$ where $g = dI/dV$ is the diode-conductance which is given by $g = I_{\text{Fg}\{\text{s/d}\}}/\varphi_T$ and the noise-source at zero voltage therefore reduces to which is correctly modeled in the above expressions. Once again, the shot-noise-modeling in MVSG-approach does not need additional parameters once the gate-current model is calibrated. Both thermal- and shot-noise sources account for the RF-device noise that is relevant to the design of RF-LNAs on the receiver-side of a transceiver system and a detailed procedure to device-level noise-figure measurements and model validation is provided in Fig. 27.

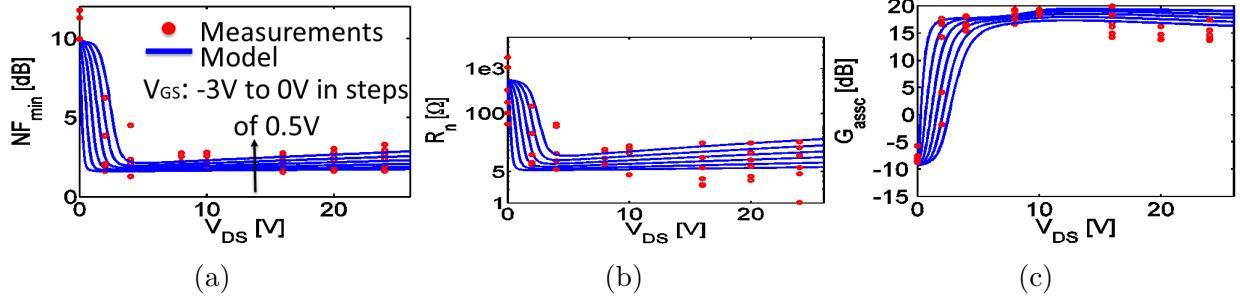


Figure 27: MVSG models RF device noise by adding thermal noise sources to parasitic and channel resistances and shot noise sources to the gate heterostructure diodes. Typical device-level minimum noise figure, associated gain and noise resistance fits comparing the model results with measurements are shown. The noise model depends only on small signal gain terms and DC terminal currents and requires no additional parameters. In this example, at $V_{DS} = 12$ V and $V_{GS} = V_{t0} + 0.15$ V, $NF_{\min} = 2$ dB and $G_{assc} = 15$ dB which is correctly predicted by the model. [14]

5.8.2 Device-Phase Noise

The second category of device-noise sources are low-frequency flicker-noise sources associated with the various charge capture and release processes in the device. The well-known Leeson's phase-noise model is adopted in the MVSG approach to capture the phase-noise in GaN-HEMTs and is given by [13]:

$$I_{1/f}^2 = K_f \frac{Wn_{\text{gf}}}{L} \frac{\left(\frac{|I_{DS}|}{Wn_{\text{gf}}} \right)^{\text{af}}}{f^{\text{ffe}}} \quad (54)$$

where the parameters K_f , af and ffe are flicker-noise fitting parameters. The I_{DS} used in the above formulation captures the bias-dependence of the flicker-noise in the device. The width-dependency adopted in the MVSG-model makes it geometry-scalable and is based on the approach given in [13]. The code accounts for polarity-change of flicker noise between forward ($V_{DS} > 0$) and reverse-modes ($V_{DS} < 0$).

Noise model implementation in Verilog-A code

```

1 if (noisemod == 1) begin
2   I(gi2p, si)      <+ white_noise(shs * 'P_QQ * abs(igsidb + 2.0 * (igssdiadb
3     + igsrecdb)), "g-s shot int");
4   I(gi2p, di)      <+ white_noise(shd * 'P_QQ * abs(igdidb + 2.0 * (igdsdiadb
5     + igdrecdb)), "g-d shot int");
6
7   I(gi2p, fps4)    <+ white_noise(shs * 'P_QQ * abs(igsip + 2.0 * (igssdio +
8     igsrec)), "g-s shot ext");
9   I(gi2p, fp4)    <+ white_noise(shd * 'P_QQ * abs(igdip + 2.0 * (igdsdio +
10    igdrec)), "g-d shot ext");
11
12   fpwr            = kf * ( w * ngf / 1 ) * pow( ( abs(ids) / ( w * ngf ) ), af );
13   if (ids <0) begin
14     fpwr           = -fpwr;
15   end
16   I(di, si)       <+ flicker_noise(fpwr, ffe, "flicker");
17
18   gm               = ddx(ids, V(gi2p));
19   svc              = 4.0 * 'P_KK * tdut * gm * ( qgs + qgd ) / ( w * ngf * 1
20     * type * cg );
21   I(di, si)       <+ white_noise(svc, "channel");
22
23   if (lgfps1>(minl) && rsh!=0) begin
24     I(si, fps1)    <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfps1 / ( w *
25       ngf )), "rfps1");
26   end
27   if (lgfps2>(minl) && rsh!=0) begin
28     I(fps1, fps2)  <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfps2 / ( w *
29       ngf )), "rfps2");
30   end
31   if (lgfps3>(minl) && rsh!=0) begin
32     I(fps2, fps3)  <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfps3 / ( w *
33       ngf )), "rfps3");
34   end
35   if (lgfps4>(minl) && rsh!=0) begin
36     I(fps3, fps4)  <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfps4 / ( w *
37       ngf )), "rfps4");
38   end
39   if (lgfp1>(minl) && rsh!=0) begin
40     I(fp1, di)     <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfp1 / ( w *
41       ngf )), "rfp1");
42   end
43   if (lgfp2>(minl) && rsh!=0) begin
44     I(fp2, fp1)    <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfp2 / ( w *
45       ngf )), "rfp2");

```

```

35
36     end
37     if (lgfp3 >(minl) && rsh!=0) begin
38         I(fp3 ,fp2) <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfp3 / ( w *
39         ngf )) , "rfp3");
40     end
41     if (lgfp4 >(minl) && rsh!=0) begin
42         I(fp4 ,fp3) <+ white_noise(4.0 * 'P_KK * tdut / (rsh * lgfp4 / ( w *
43         ngf )) , "rfp4");
44     end
45     if ((rcs_w >= minr) && (rcs_w > 0)) begin
46         I(src ,s) <+ white_noise(4.0 * 'P_KK * tdut / rsi , "rcs");
47     end
48     if ((rcd_w >= minr) && (rcd_w > 0)) begin
49         I(d,drc) <+ white_noise(4.0 * 'P_KK * tdut / rdi , "rcd");
50     end
51 end

```

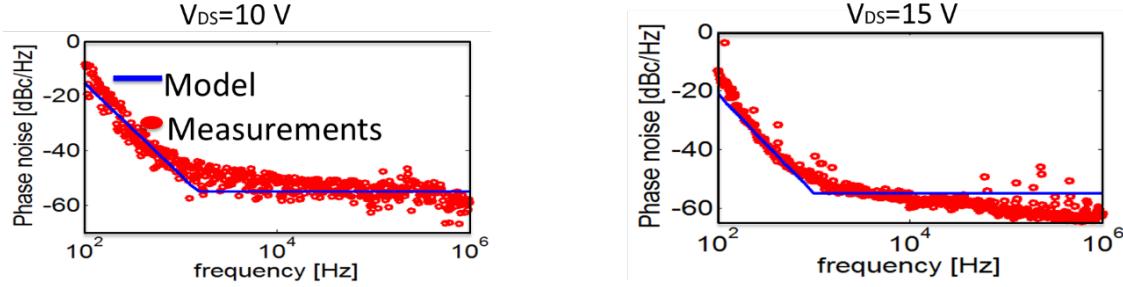


Figure 28: Measured low frequency phase noise spectrum compared against simulation using the MVSG model. [14]

5.9 Channel RF- g_m Dispersion

The channel current in GaN HEMTs may not respond instantaneously to the applied V_{GS} at high-frequency RF-circuit operation. This time-lag or the transit-time of carriers manifests as the phase-lag in frequency domain in the device g_m characteristics. This is captured in MVSG model using the approach proposed in [15]. The channel current at low frequency I_{DS} is passed through a second-order transfer function to obtain the channel current $I_{DS,RF}$ that incorporates the NQS effect as shown below:

$$I_{DS,RF} = \frac{I_{DS}}{\left(1 + s\tau_{gmrf} + \frac{s^2\tau_{gmrf}^2}{3}\right)} \quad (55)$$

Here τ_{gmrf} is the transit-time constant in the channel of RF-GaN HEMT.

Channel NQS-transport model implementation in Verilog-A code

```

1 // channel-gm-dispersion calculations
2 idsrf = V(xt2);
3 if (gmdisp==0) begin
4     V(xt1) <+ 0;
5     V(xt2) <+ 0;
6     I(di, si) <+ ids + gmin * V(di, si);
7 end else begin
8     I(xt1) <+ ids - V(xt2) - ddt(taugmrf * V(xt1));
9     I(xt2) <+ V(xt1) - V(xt2) - ddt((taugmrf/3.0) * V(xt2));
10    I(di, si) <+ idsrf + gmin * V(di, si);
11 end
12 I(gi2p, si) <+ ddt(qgs) + ddt(minc * V(gi2p, si));
13 I(gi2p, di) <+ ddt(qgd) + ddt(minc * V(gi2p, di));

```

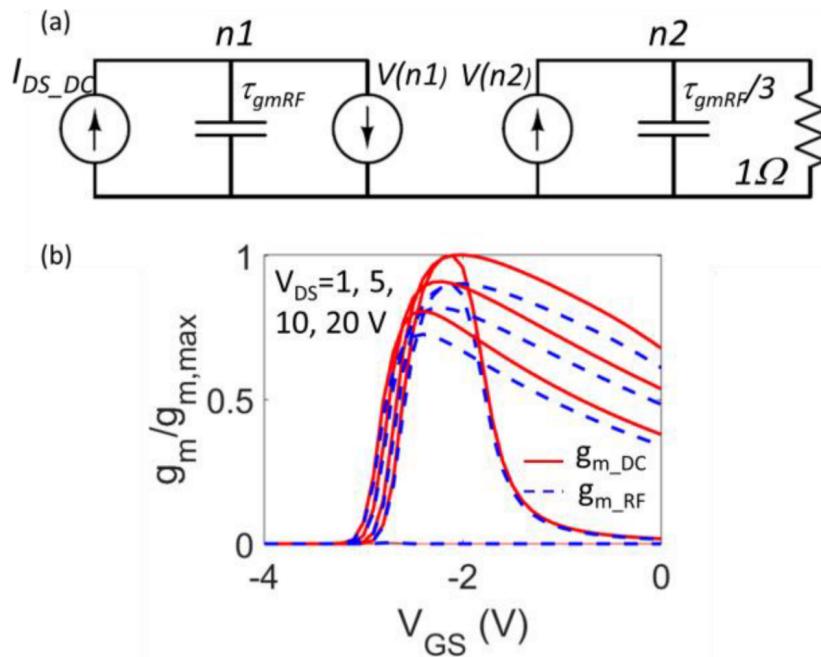


Figure 29: (a) Equivalent circuit to account for RF- g_m dispersion by following modified Weil–McNamee excess phase to introduce excess phase in channel-current. (b) MVSG simulation results with and without RF- g_m dispersion, by setting flag parameter $gmdisp$ to 1 and 0, respectively. [16]

5.10 Channel Breakdown Model

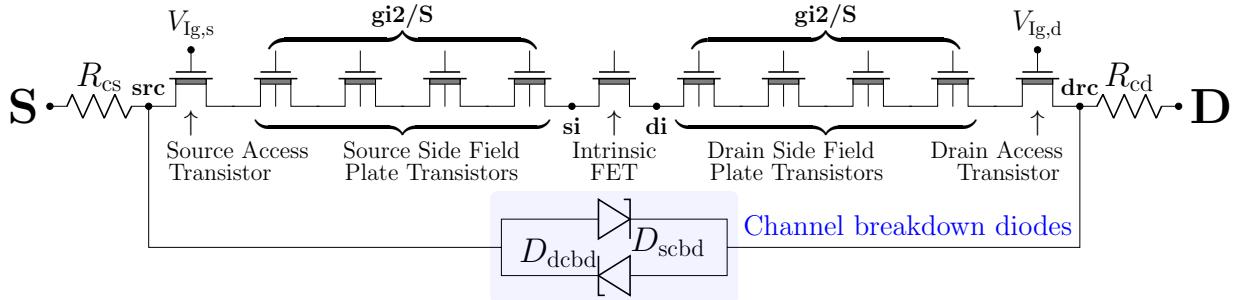


Figure 30: Partial MVSG schematic of channel-breakdown model that shows the two back-to-back breakdown diodes that are de-biased through the source/drain contact resistances.

The primary breakdown characteristics of well-designed GaN HEMTs with robust back-end passivation and metallization are due to gate-drain and gate-source diode breakdown and/or the channel-breakdown. The MVSG model captures these breakdown characteristics with function calls to a single model formulation given by [16]

$$I_{G\{S/D\}} = I_{R,BD} K_{BD} (\exp(-\phi_{BD} V_{BD}) - \exp(-\phi_{BD} (V_{G\{S/D\}} - V_{BD}))) \quad (56)$$

$$I_{CH,F} = I_{R,CHBD} K_{CHBD} (\exp(-\phi_{BD} V_{BD}) - \exp(-\phi_{BD} (V_{DS} + V_{DG} - V_{BD}))) \quad (57)$$

$$I_{CH,R} = I_{R,CHBD} K_{CHBD} (\exp(-\phi_{BD} V_{BD}) - \exp(-\phi_{BD} (V_{SD} + V_{SG} - V_{BD}))) \quad (58)$$

Here $I_{G\{S/D\}}$ is the gate- $\{$ source/drain $\}$ diode-breakdown current, $I_{CH,F}$ is the channel-breakdown current in forward-mode and $I_{CH,R}$ in reverse-mode. ϕ_{BD} is the ideality-factor that determines the turn-on rate, V_{BD} is the voltage of onset of breakdown and I_R is the reverse saturation current parameter of each of the breakdown diode. The models can be activated by user-defined flags: K_{CHBD} and K_{BD} . Example turn-on behavior of channel-breakdown in forward and reverse modes along with its bias-dependence is shown in Fig. 31. The channel-current increase once V_{DS} exceeds V_{BD} can be observed from Fig. 31(a). The V_{DG} -term in equations above causes the breakdown voltage to have V_G -dependence wherein the breakdown sets in earlier at higher- V_{GS} . The back-to-back diode implementation also captures the breakdown in symmetric switch FETs where $|V_{SD}|$ exceeds V_{BD} as shown in Fig. 31(b). The FET-breakdown characteristics are different in reverse-mode and can be observed in Fig. 31(c) which shows a lower breakdown voltage. Equivalent figures when contact-resistance de-biasing of the breakdown currents are shown in Figs. 31(d)-(f). This option is activated by setting the flag $cbddmod=1$. The figure also demonstrates that the implementation satisfies Gummel symmetry; a requirement for all standard compact models. While thermal dependence of breakdown voltage is not activated in this example, linear temperature coefficient is added to V_{BD} to shift the onset of channel and gate-breakdown and the slope of turn-on current is controlled by the temperature co-efficient of ϕ_{BD} . The breakdown of individual FP-transistors can also be modeled as internal back-to-back diodes using the same approach but this will result in several function calls to the breakdown module implementing the equations. Only terminal breakdown characteristics are adopted in CMC-standard version of MVSG model.

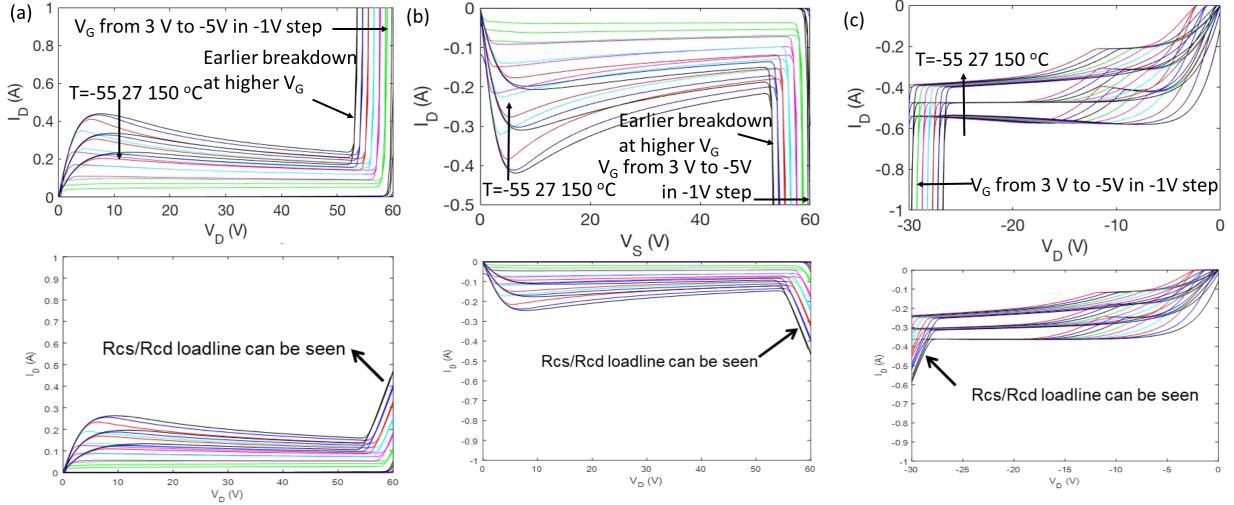


Figure 31: **(a)** Channel-breakdown model in the forward mode which shows the increase in turn-on voltage as V_G is reduced. **(b)** The symmetric breakdown behavior in a switch-FET with negative V_{DS} applied. **(c)** Reverse-mode breakdown behavior shown in the third-quadrant. Equivalent results are also shown with de-biasing of breakdown currents through source/drain contact resistances (R_{cs}/R_{cd}) that clearly demonstrate the load-line effects after the onset of breakdown-currents.

Channel breakdown model implementation in Verilog-A code

```

1 // channel-breakdown current calculations
2 if (icbdmod == 1) begin
3     if (cbddbmod == 0) begin
4         vinscbd      = type * ( V(s,d) + V(s,gi2p) );
5         vindcbd      = type * ( V(d,s) + V(d,gi2p) );
6     end else begin
7         vinscbd      = type * ( V(src,drc) + V(src,gi2p) );
8         vindcbd      = type * ( V(drc,src) + V(drc,gi2p) );
9     end
10    igscbd        = calc_ig(igscbddio,igsrecbd,vinscbd,phit,vgsats,alphags,
11                           fracs,0,pchbdgs,vchbdgs,tfacdiode,w,ngf,ijscbd,1.0,vgsatqs,betarecs,0,
12                           pgsreecs,0,vjg,type);
13    igdcbd        = calc_ig(igdcbddio,igdrecbd,vindcbd,phit,vgsatd,alphagd,
14                           fracd,0,pchbdgd,vchbdgd,tfacdiode,w,ngf,ijdcbd,1.0,vgsatqd,betarecd,0,
15                           pgsrecd,0,vjg,type);
16    if (cbddbmod == 0) begin
17        I(s,d)      <+ igscbd;
18        I(d,s)      <+ igdcbd;
19    end else begin
20        I(src,drc)  <+ igscbd;
21        I(drc,src)  <+ igdcbd;
22    end
23 end else begin
24     vinscbd      = 0;
25     vindcbd      = 0;
26 end

```

5.11 Distributed Gate Resistance Model

Large-periphery devices with long width-per-finger show significant delay along the gate-line as shown in the schematic of Fig. 32(a). A simple lumped RC-circuit approach to model gate-delay may not be sufficient at high-frequencies relevant for GaN HEMT-based RF-applications. Layout improvements such as multiple gate fingers as well as gate-contacts as shown in Fig. 32(b) can alleviate the gate-delay problem but do not mitigate it. In Fig. 32(b), the gate-line is contacted at two places ($N_{con} = 1, N_{con} = 2$) using pads as shown. The resistance along the gate-line portion in the non-active width (W) region; namely X_{ov} also needs accounting. MVSG model borrows from [17] to include these layout-dependent and distributed effects in modeling layout dependency in gate-resistance. [16]

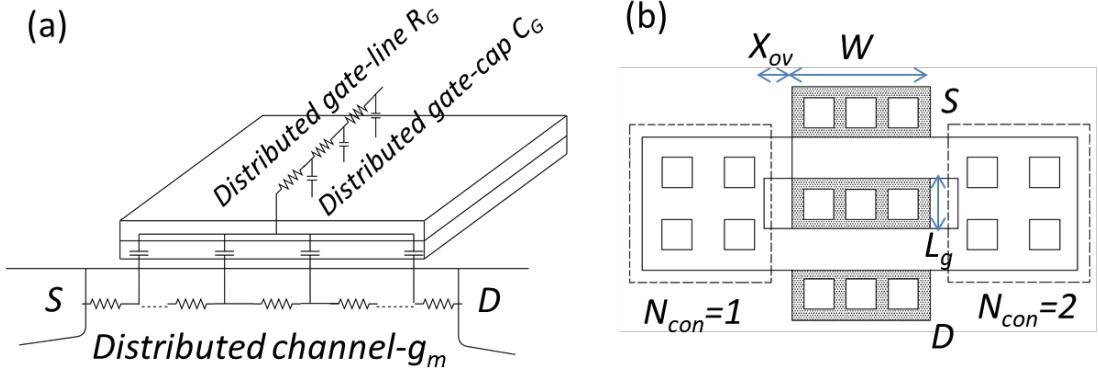


Figure 32: (a) Schematic showing the distributed effects in both gate-line and channel which cause non-quasi-static behavior at high-frequency. (b) Layout-schematic shows multiple-gate contacts, non-active portion of gate-finger etc. which have to be included in a scalable input-impedance model.

The gate-resistance of each finger is partly shunted by gate-capacitance of the FET (channel and fringing). It is well known that the real part of Y_{11} is lower at high frequencies in comparison to DC conditions. The portion of gate-resistance that is shunted out at high frequency by device-capacitance has been calculated in earlier works to be 2/3 [17]. The DC-gate-resistance (R_{G_DC}) is distributed by splitting the R_{G_DC} in the ratio of 1/3 and 2/3 and implemented in MVSG model as a series of two resistances R_{G1} and R_{G2} that requires an additional internal node. The DC-gate-resistance is computed using (4) that include the impact of multiple gate-contacts (N_{con}), resistance of the finger in the non-active region (X_{ov}) and finger-count (N_{gf}) [17] in accordance with the layout shown in Fig. 32(b). Here R_{sh} is the sheet resistance of gate-metal line.

$$R_{G_DC} = R_{G1} + R_{G2} = R_{sh}(X_{ov} + W/N_{con})/(N_{con}L_g N_{gf}) \quad (59)$$

$$R_{G1} = R_{SH}(X_{ov} + W/3N_{con})/(N_{con}L_g N_{gf}) \quad (60)$$

The distributed RC-circuit can be implemented in two ways as shown in Fig. 33. In the first approach shown in Fig. 33(a), the portion R_{G2} of gate-resistance R_{G_DC} is shunted by fringing gate-capacitances alone and not the channel capacitance. In the second approach as depicted in Fig. 33(b), the FET is split along its width direction to accurately capture the distributed nature of the gate-delay problem depicted in Fig. 32(a). The FET-element with width $W\alpha_{GATE}$ is connected to the internal gate-node G_{int} and shunts R_{G2} . While this approach captures bias-dependence of the RC-time constant more accurately, it increases simulation time as now there are two function calls to the non-linear device-current and charge formulations in MVSG core-model. Only the first approach is adopted in the official CMC-standard MVSG model as it suffices for reasonable accuracy with fast convergence characteristics.

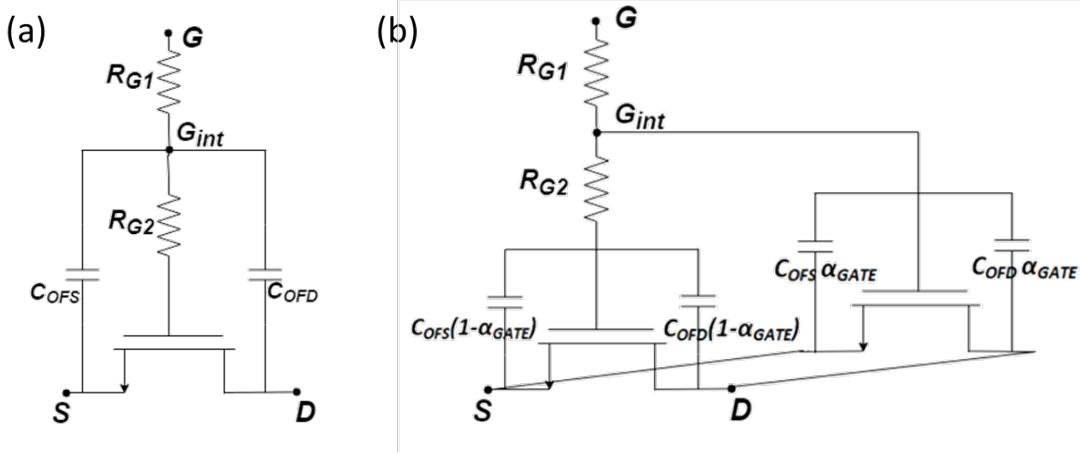


Figure 33: Equivalent circuit models adopted to capture non-quasi-static behavior at high-frequency with the distributed $R_{G_DC}=R_{G1}+R_{G2}$. (a) Simple equivalent circuit approach wherein only fringing capacitances shunt R_{G2} . (b) A more accurate approach uses both bias-dependent channel- and fringing-capacitance to shunt R_{G2} . This approach splits the FET in the ratio of $\alpha_{GATE} : (1-\alpha_{GATE})$ along width direction so that a portion of the channel-capacitance shunts R_{G2} . However, it requires two-time function calls (and computation) of device-currents and capacitances in the MVSG model.

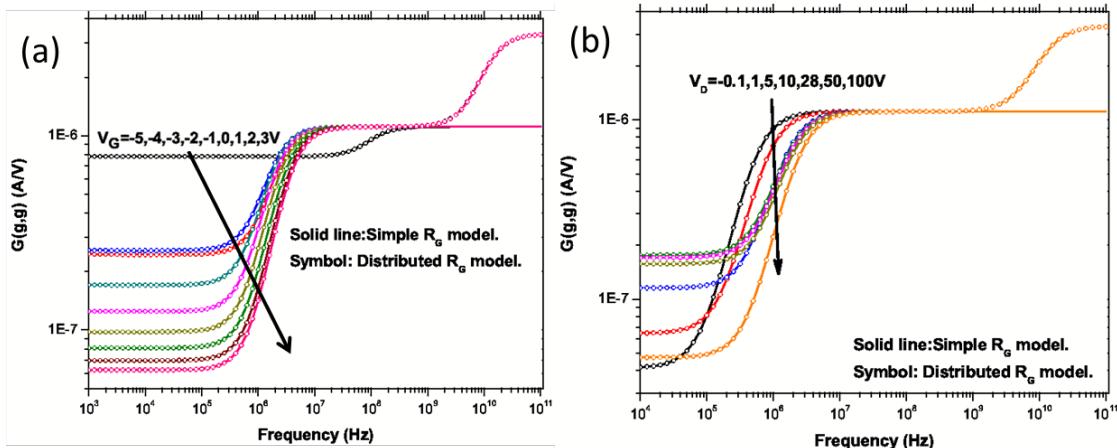


Figure 34: Frequency characteristics of the real part of input admittance ($G(g,g) = \text{Re}\{Y_{11}\}$) are plotted using the equivalent circuit model of Fig. 30(a) and compared against a simple non-distributed R_G -model. In (a), V_G is swept from off-to-on state in saturation region ($V_D = 28$ V). In (b), the drain voltage is swept from linear-to-saturation region with $V_G = -4$ V. In both cases, it can be seen that the high frequency value of $G(g,g)$ is $3\times$ higher than the non-distributed R_g -case indicating effective shunting of R_{G2} by the device-fringing capacitances. The corner frequency for this shunting effect is bias-independent at ~ 10 GHz.

Results of input-impedance simulations using the first equivalent circuit approach of Fig. 33(a) are shown in Fig. 35 along with a simple R_G model with the gate-delay model deactivated. The real part of Y_{11} is plotted as a function of frequency for different V_G in Fig.

35(a) and for different V_D in Fig. 35(b). The series RC time-constant is constant at 1 MHz and is present even in the simple R_G -model. However, the equivalent circuit approach of Fig. 33(a) shunts out R_{G2} through the fringing capacitance at 10 GHz. Since both the fringing capacitances and R_{G2} are bias independent, the parallel RC-corner frequency does not change with bias as can be seen. Beyond this point $G(g,g)$ in the distributed model increases to $3 \times$ the value of $G(g,g)$ from the simple R_g -model. Results of distributed nature of gate-delay using the equivalent circuit approach of Fig. 33(b) are given in Fig. 35. As the FET is split in the width-ratio of α_{GATE} and $(1-\alpha_{GATE})$ (where α_{GATE} is the input parameter) and the gate-capacitance of FET with width of $\alpha_{GATE}W$ effectively shunts out at R_{G2} high-frequency, the corner frequency becomes bias-dependent. The corner frequency goes down from ~ 10 GHz to ~ 0.1 GHz from off-to-on state due to increased channel-capacitance in the on-state.

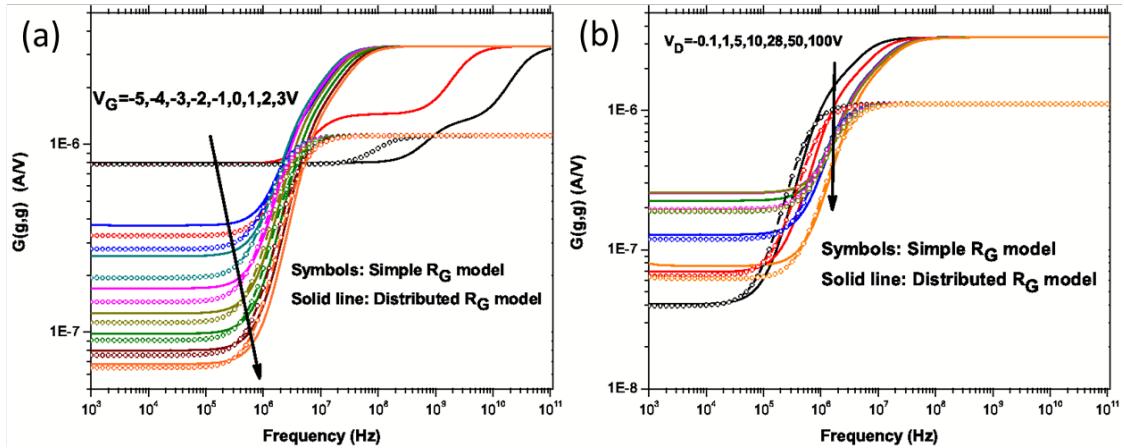


Figure 35: Frequency characteristics of the real part of input admittance ($G(g,g) = \text{Re}\{Y_{11}\}$) is plotted using the equivalent circuit model of Fig. 6 and compared against a simple non-distributed R_G -model. The same bias conditions are used as in Fig. 31. In both cases, it can be seen that the high frequency value of $G(g,g)$ is $3 \times$ higher than the non-distributed R_g -case indicating the shunting of R_{G2} by total device-capacitances. However, the corner frequency is bias-dependent especially for V_G close to V_T due to the change in channel-capacitances around V_T . The corner frequency changes from ~ 10 GHz to ~ 0.1 GHz from off-to-on state due to the increased channel capacitance in the on-state.

Distributed gate-resistance model

```

1 // Definition and Instantiation of rg1 and rg2
2 rg1 = ( rgsp / ngf / ngcon ) * ( lovg + agate * w / ngcon );
3 rg2 = ( rgsp / ngf / ngcon ) * ( (1.0 - agate) * w / ngcon );
4
5 // Connection to schematic
6 if ((rg1 >= minr) && (rg1 > 0)) begin
7     I(g,gi1) <+ V(g,gi1) / rg1;
8 end else begin
9     V(g,gi1) <+ 0;
10 end
11 if ((rg2 >= minr) && (rg2 > 0)) begin
12     I(gi1,gi2) <+ V(gi1,gi2) / rg2;
13 end else begin
14     V(gi1,gi2) <+ 0;
15 end

```

5.12 DC Gummel Symmetry Test

The DC Gummel Symmetry test is a benchmark test for compact models that states the drain and source terminals on the transistor are swappable. The nth order derivative of the channel current should be continuous and symmetric at and around $V_{DS} = 0\text{V}$. The workbench for the test is shown in Fig. 36 with a 4-terminal transistor representing the intrinsic transistor in the MVSG model. The body of the transistor is grounded and a voltage of V_0 is applied to the gate terminal of the device. The drain and source sides of the device have an equal in magnitude but opposite in polarity V_x applied to them. Users who would like to test for Gummel Symmetry using the MVSG model, with differentiability in the current around $V_{DS} = 0\text{V}$ should (i) choose an even *beta* parameter and (ii) the parameter *flaggum* should be toggled from 0 (default, Gummel Symmetry off) to 1 (Gummel Symmetry on).

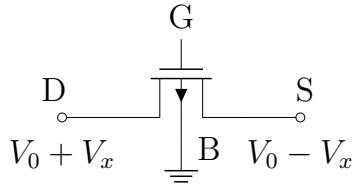


Figure 36: DC Gummel Symmetry Test Bench

By toggling the parameter *flaggum* from 0 to 1, a different smoothing function will be used and can be seen in the ***absfunc*** and ***mmax*** function implementation in Verilog-A code found at the end of this section. These functions are used to smooth out mathematical discontinuities in the channel current, but the default ones are insufficient for the case of the Gummel Symmetry test. The new smoothing function implemented specifically for the test is an infinitely differentiable exponential function, i.e. $\text{xtanh}(x)$. Its implementation can also be found in the ***absfunc*** and ***mmax*** function implementation at the end of this

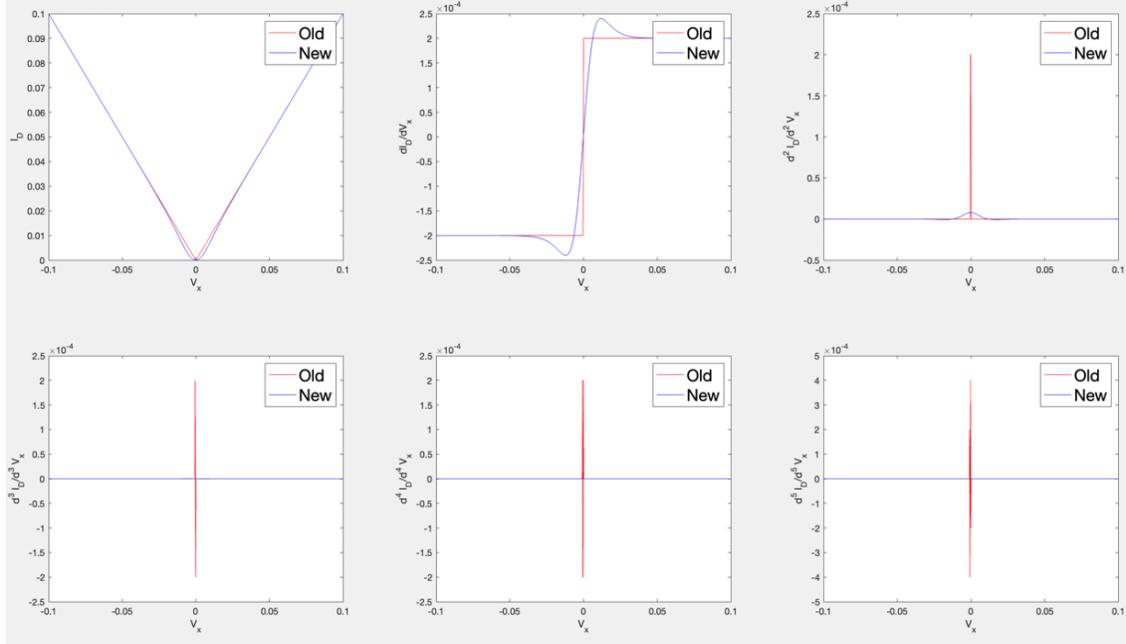


Figure 37: A comparison between the old and new smoothing functions used in ***absfunc*** and ***mmax***.

section. However, using new smoothing functions are computationally heavy and require a longer computation time. Users who would like quick computations without a need for differentiability at $V_{DS} = 0$ V should use the old default function (*flaggum*=0) and any value of *beta*. A comparison between the two smoothing functions is shown in Fig. 37 and a successful Gummel Symmetry test using the new smoothing function and *beta*=2 is displayed in Fig. 38.

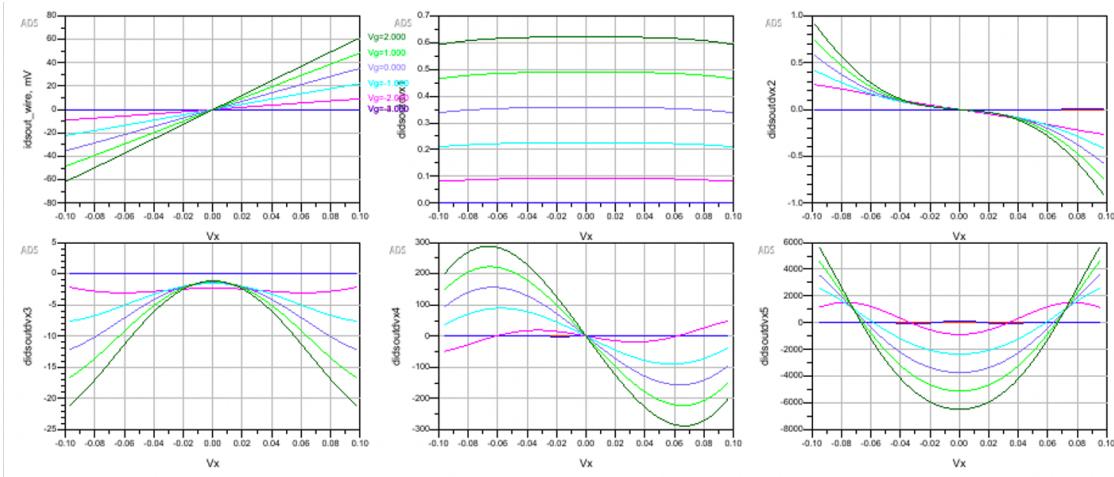


Figure 38: Gummel Symmetry test using the new **absfunc/mmax** functions and setting $\beta=2$.

absfunc and mmax function implementation in Verilog-A code

```

1 analog function real absfunc;
2   input x, s;
3   real x, s;
4   begin
5     if (flaggum == 0) begin
6       absfunc = sqrt( x * x + s );
7     end else begin
8       absfunc = x * tanh( ( 1.0e-3 / s ) * x );
9     end
10    end
11  endfunction
12
13 analog function real mmax;
14   input x,y,s;
15   real x,y,s;
16   begin
17     if (flaggum == 0) begin
18       mmax = 0.5 * ( x + y + sqrt( ( x - y ) * ( x - y ) + s ) );
19     end else begin
20       mmax = 0.5 * ( x + y + ( x - y ) * tanh( ( 1.0e-3 / s ) * ( x - y )
21 ) );
22     end
23   end
24 endfunction

```

6 MVSG Model: Parameter List

The following table shows the list of all parameters needed for fitting MVSG model. The macro, default value, units, & description are also listed. These were released along with the default parameters in the Verilog-A files: **mvsg_cmc_4.0.0.va**. The default parameter set used with the QAsuite in the parameters folder under the name: **dmodeParameters.txt** for depletion mode devices and **poweremodeParameters.txt** for power enhancement mode deviecs.

6.1 Instance Parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
IPRoz	w	180.0e-6	1e-6			m Width per Finger
IPRoz	l	250.0e-9				m Effective gate length
IPIco	ngf	1	1			Number of Fingers
IPRnb	dtemp	0.0				K Device temperature offset from ambient

6.2 Core Model Parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	version	4.00				Version number
MPRco	tnom	27.0				deg C Reference temperature for the model
MPIty	type	1	-1	1		nFET=1 pFET=-1
MPRoz	cg	4.00e-03	8e-4	8e-3	F/m^2	Gate cap/area
MPRnb	tcg	0.0	0		1/K	cg dependence on temperature
MPRcz	cofsm	0.0	0		F/m	Gate - Source outer fringing cap/width (bias-dependent component)
MPRcz	cofdm	0.0	0		F/m	Gate - Drain outer fringing cap/width (bias-dependent component)
MPRcz	cofdsm	0.0	0		F/m	Source - Drain outer fringing cap/width (bias-dependent component)
MPRcz	cofdsubm	0.0	0		F/m	Sub - Drain outer fringing cap/width (bias-dependent component)
MPRcz	cofssubm	0.0	0		F/m	Sub - Source outer fringing cap/width (bias-dependent component)
MPRcz	cofgsubm	0.0	0		F/m	Sub - Gate outer fringing cap/width (bias-dependent component)
MPRcz	cofsm0	0.0	0		F/m	Gate - Source outer fringing cap/width (bias-independent component)
MPRcz	cofdm0	0.0	0		F/m	Gate - Drain outer fringing cap/width (bias-independent component)
MPRcz	cofdsm0	0.0	0		F/m	Source - Drain outer fringing cap/width (bias-independent component)
MPRcz	cofdsubm0	0.0	0		F/m	Sub - Drain outer fringing cap/width (bias-independent component)
MPRcz	cofssubm0	0.0	0		F/m	Sub - Source outer fringing cap/width (bias-independent component)
MPRcz	cofgsubm0	0.0	0		F/m	Sub - Gate outer fringing cap/width (bias-independent component)

MPRnb	tcofs	0.0	0		1/K	cofs dependence on temperature
MPRnb	tcofd	0.0	0		1/K	cofd dependence on temperature
MPRnb	tcofds	0.0	0		1/K	cofds dependence on temperature
MPRnb	tcofssub	0.0	0		1/K	cofssub dependence on temperature
MPRnb	tcofdsub	0.0	0		1/K	cofdsub dependence on temperature
MPRnb	tcofgsub	0.0	0		1/K	cofgsub dependence on temperature
MPRnb	vtfrin	-50	-50		V	Threshold voltage for fringing fields
MPRoz	nfrin	1e2	0		V	Fringing capacitance's V-dependent slope; NOTE: Make sure it is larger than 65mV/decade
MPRoz	rsh	150.0	50	200	Ohms/Sq	2-DEG Sheet Resistance
MPRcz	rcs	800e-6	1e-4	1e-3	Ohms*m	Source contact resistance * Width
MPRcz	rcd	800e-6	1e-4	1e-3	Ohms*m	Drain contact resistance * Width
MPRoz	vx0	3.0e5	8e4	3e5	m/s	Source injection velocity
MPRoz	mu0	0.135	0.08	0.18	m^2/Vs	Low-field mobility
MPRoz	beta	2.0	0.5	3		Linear to saturation parameter; NOTE: Users who want differentiability should use even beta
MPRnb	vto	-2.72	-9	3	V	Threshold voltage
MPRoz	ss	0.120	0.065		V/dec	Sub-threshold slope
MPRcz	delta1	16e-3	0			DIBL Coefficient 1
MPRcz	delta2	0.0	0			DIBL Coefficient 2
MPRcz	dibsat	10.0			V	DIBL saturation Voltage
MPRcz	nd	0.0	0			Punchthrough factor for subth slope
MPRoz	alpha	3.5	2	5		Weak to strong inversion transition factor; NOTE: alpha should scale up linearly with ss: alpha=3.5 for ss=65mV/dec
MPRcz	lambda	0.0	0		1/V	CLM parameter
MPRcz	vtheta	0.0	0		1/V	Scattering: velocity reduction parameter with Vg
MPRcz	mtheta	0.0	0		1/V	Scattering: mobility reduction parameter with Vg
MPRcz	vzeta	150e3			1/K	vx0 dependence on temperature
MPRnb	vtzeta	-0.4e-3			V/K	vto dependence on temperature
MPRcz	epsilon	2.3	1	3.5		Mobility dependence on temperature
MPRnb	rct1	0.0	0		1/K	Linear Rsh and Rc temperature coefficient
MPRnb	rct2	0.0	0		1/K^2	Quadratic Rsh and Rc temperature coefficient
MPIsw	flagres	0	0	1		Flag parameter for resistor: resistor is chosen if flagres=1 or implicit transistor is chosen if flagres=0
MPIsw	flagsp	0	0	1		Flag parameter for VT-shift with surface potential: flagsp=0 by default turns it off (robust); flagsp=1 turns it on (possibility to have kinks in charge at certain parameter sets)
MPIsw	flaggum	0	0	1		Flag parameter for smoothing function in absfunc and mmax: xtanhx smoothing function used if flaggum=1 or original implementation if flaggum=0; source voltage of SAR and DAR uses xtanhx if flaggum=1 or original piecewise if flaggum=0
MPRcz	mmaxs	4.0e-5				Parameter to control how much smoothing in majority of function calls to mmax and absfunc

6.3 Source access region parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	lgs	3.0e-6	0		m	Source access region (SAR) length parameter
MPRnb	vtors	-650	-650	-15	V	SAR threshold voltage
MPRoz	cgrs	5.0e-3	1e-4	1e-2	F/m^2	SAR gate-cap/area
MPRoz	vx0rs	100e3	8e4	3e5	m/s	SAR source injection velocity
MPRoz	mu0rs	100e-3	0.08	0.18	m^2/Vs	SAR low-field mobility
MPRoz	betars	1.00	0.5	3		SAR linear to saturation parameter
MPRcz	delta1rs	100e-3	0			SAR DIBL Coefficient
MPRoz	srs	0.100	0.065		V/dec	SAR Sub-threshold slope
MPRcz	ndrs	0.0	0			SAR punchthrough factor for subth slope
MPRcz	vthetars	0.0	0		1/V	SAR scattering: velocity reduction parameter with Vg
MPRcz	mthetars	0.0	0		1/V	SAR scattering: mobility reduction parameter with Vg
MPRoz	alphars	3.5	2	5		SAR weak to strong inversion transition factor; NOTE: alphars should scale up linearly with srs: alphrs=3.5 for srs=65mV/dec

6.4 Drain access region parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	lgd	4.85e-6	0		m	Drain access region (DAR) length parameter
MPRnb	vtord	-650	-650	-15	V	DAR threshold voltage
MPRoz	cgrd	4.3e-3	1e-4	1e-2	F/m^2	DAR gate-cap/area
MPRoz	vx0rd	100e3	8e4	3e5	m/s	DAR source injection velocity
MPRoz	mu0rd	100e-3	0.08	0.18	m^2/Vs	DAR low-field mobility
MPRoz	betard	1.00	0.5	3		DAR linear to saturation parameter
MPRcz	delta1rd	0.35	0			DAR DIBL Coefficient
MPRoz	srd	0.3	0.065		V/dec	DAR Sub-threshold slope
MPRcz	ndrd	3.8	0			DAR punchthrough factor for subth slope
MPRcz	vthetard	0.0	0		1/V	DAR scattering: velocity reduction parameter with Vg
MPRcz	mthetard	0.0	0		1/V	DAR scattering: mobility reduction parameter with Vg
MPRoz	alphard	3.5	2	5		DAR weak to strong inversion transition factor; NOTE: alphard should scale up linearly with srd: alphrd=3.5 for srd=65mV/dec

6.5 Source-side Field-Plate 1 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfps1	1	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfps1	0.0	0		m	FP Length
MPRnb	vtofps1	-44.5	-600 0		V	FP threshold voltage
MPRoz	cgfps1	2.0e-4			F/m^2	FP gate-cap/area
MPRnb	tcfgps1	0.0	0		1/K	cfps1 dependence on temperature
MPIsw	flagfps1s	1	0 1			Flag parameter: cfps1s select=1 or cfp1s not select=0
MPRcz	cfps1s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfps1b	1	0 1			Flag parameter: ccfps1; cbfps1 select=1 or ccfps1; cbfps1 not select=0
MPRcz	ccfps1	0.9e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfps1	0.0	0		1/K	ccfps1 dependence on temperature
MPRcz	cbfps1	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfps1	0.0	0		1/K	cbfps1 dependence on temperature
MPRoz	vx0fps1	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fps1	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafps1	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fps1	0.0	0			FP DIBL Coefficient
MPRoz	sfps1	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfps1	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafps1	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafps1	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafps1	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafps1	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafps1 should scale up linearly with sfps1: alphafps1=3.5 for sfps1=65mV/dec

6.6 Source-side Field-Plate 2 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfps2	0	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfps2	0.0	0		m	FP Length
MPRnb	vtofps2	-74.5	-600 vtofps1		V	FP threshold voltage
MPRoz	cgfps2	1.0e-4			F/m^2	FP gate-cap/area
MPRnb	tcfgps2	0.0	0		1/K	cfps2 dependence on temperature
MPIsw	flagfps2s	1	0 1			Flag parameter: cfsp2s select=1 or cfps2s not select=0
MPRcz	cfps2s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfps2b	1	0 1			Flag parameter: ccfps2; cbfps2 select=1 or ccfps2; cbfps2 not select=0
MPRcz	ccfps2	0.3e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfps2	0.0	0		1/K	ccfps2 dependence on temperature
MPRcz	cbfps2	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfps2	0.0	0		1/K	cbfps2 dependence on temperature
MPRoz	vx0fps2	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fps2	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafps2	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fps2	0.0	0			FP DIBL Coefficient
MPRoz	sfps2	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfps2	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafps2	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafps2	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafps2	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafps2	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafps2 should scale up linearly with sfps2: alphafps2=3.5 for sfps2=65mV/dec

6.7 Source-side Field-Plate 3 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfps3	0	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfps3	0.0	0		m	FP Length
MPRnb	vtofps3	-74.5	-600 vtofps2		V	FP threshold voltage
MPRoz	cgfps3	1.0e-4			F/m^2	FP gate-cap/area
MPRnb	tgcfps3	0.0	0		1/K	cgfps3 dependence on temperature
MPIsw	flagfps3s	1	0 1			Flag parameter: cfps3s select=1 or cfps3s not select=0
MPRcz	cfps3s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfps3b	1	0 1			Flag parameter: ccfps3; cbfps3 select=1 or ccfps3; cbfps3 not select=0
MPRcz	ccfps3	0.3e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfps3	0.0	0		1/K	ccfps3 dependence on temperature
MPRcz	cbfps3	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfps3	0.0	0		1/K	cbfps3 dependence on temperature
MPRoz	vx0fps3	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fps3	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafps3	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fps3	0.0	0			FP DIBL Coefficient
MPRoz	sfps3	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfps3	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafps3	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafps3	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafps3	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafps3	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafps3 should scale up linearly with sfps3: alphafps3=3.5 for sfps3=65mV/dec

6.8 Source-side Field-Plate 4 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfps4	0	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfps4	0.0	0		m	FP Length
MPRnb	vtofps4	-74.5	-600 vtofps3		V	FP threshold voltage
MPRoz	cgfps4	1.0e-4			F/m^2	FP gate-cap/area
MPRnb	tgcfps4	0.0	0		1/K	cgfps4 dependence on temperature
MPIsw	flagfps4s	1	0 1			Flag parameter: cfps4s select=1 or cfps4s not select=0
MPRcz	cfps4s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfps4b	1	0 1			Flag parameter: ccfps4; cbfps4 select=1 or ccfps4; cbfps4 not select=0
MPRcz	ccfps4	0.3e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfps4	0.0	0		1/K	ccfps4 dependence on temperature
MPRcz	cbfps4	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfps4	0.0	0		1/K	cbfps4 dependence on temperature
MPRoz	vx0fps4	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fps4	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafps4	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fps4	0.0	0			FP DIBL Coefficient
MPRoz	sfps4	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfps4	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafps4	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafps4	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafps4	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafps4	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafps4 should scale up linearly with sfps4: alphafps4=3.5 for sfps4=65mV/dec

6.9 Field-Plate 1 Parameters

Macro	Parameter	Default Value	Typical Min and Max Value*	Units	Description	
MPIsw	flagfp1	1	0 1		Flag parameter: GFP=1 or SFP=0	
MPRcz	lgfp1	0.0	0	m	FP Length	
MPRnb	vtofp1	-44.5	-600	vtofps3	FP threshold voltage	
MPRoz	cgfp1	2.0e-4		F/m^2	FP gate-cap/area	
MPRnb	tcfp1	0.0	0	1/K	cgp1 dependence on temperature	
MPIsw	flagfp1s	1	0 1		Flag parameter: cfp1s select=1 or cfp1s not select=0	
MPRcz	cfp1s	0e-19	0	F/m	FP (source-side) to source cap/width	
MPIsw	flagfp1b	1	0 1		Flag parameter: ccfp1; cbfp1 select=1 or ccfp1; cbfp1 not select=0	
MPRcz	ccfp1	0.9e-10	0	F/m	Source or gate to drain (under FP) cap/width	
MPRnb	tccfp1	0.0	0	1/K	ccfp1 dependence on temperature	
MPRcz	cbfp1	0.0	0	F/m	Body to drain (under FP) cap/width	
MPRnb	tcbfp1	0.0	0	1/K	cbfp1 dependence on temperature	
MPRoz	vx0fp1	1.2e5	8e4 3e5	m/s	FP source injection velocity	
MPRoz	mu0fp1	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafp1	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fp1	0.0	0			FP DIBL Coefficient
MPRoz	sfp1	3.2	0.065	V/dec		FP Sub-threshold slope
MPRcz	ndfp1	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafp1	-0.4e-3		V/K		vto dependence on temperature
MPRcz	vthetafp1	0.0	0	1/V		FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafp1	0.0	0	1/V		FP scattering: mobility reduction parameter with Vg
MPRoz	alphafp1	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafp1 should scale up linearly with sfp1: alphafp1=3.5 for sfp1=65mV/dec

6.10 Field-Plate 2 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*	Units	Description	
MPIsw	flagfp2	0	0 1		Flag parameter: GFP=1 or SFP=0	
MPRcz	lgfp2	0.0	0	m	FP Length	
MPRnb	vtofp2	-74.5	-600	vtofp1	FP threshold voltage	
MPRoz	cgfp2	1.0e-4		F/m^2	FP gate-cap/area	
MPRnb	tcfp2	0.0	0	1/K	cgp2 dependence on temperature	
MPIsw	flagfp2s	1	0 1		Flag parameter: cfp2s select=1 or cfp2s not select=0	
MPRcz	cfp2s	0e-19	0	F/m	FP (source-side) to source cap/width	
MPIsw	flagfp2b	1	0 1		Flag parameter: ccfp2; cbfp2 select=1 or ccfp2; cbfp2 not select=0	
MPRcz	ccfp2	0.3e-10	0	F/m	Source or gate to drain (under FP) cap/width	
MPRnb	tccfp2	0.0	0	1/K	ccfp2 dependence on temperature	
MPRcz	cbfp2	0.0	0	F/m	Body to drain (under FP) cap/width	
MPRnb	tcbfp2	0.0	0	1/K	cbfp2 dependence on temperature	
MPRoz	vx0fp2	1.2e5	8e4 3e5	m/s	FP source injection velocity	
MPRoz	mu0fp2	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafp2	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fp2	0.0	0			FP DIBL Coefficient
MPRoz	sfp2	3.2	0.065	V/dec		FP Sub-threshold slope
MPRcz	ndfp2	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafp2	-0.4e-3		V/K		vto dependence on temperature
MPRcz	vthetafp2	0.0	0	1/V		FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafp2	0.0	0	1/V		FP scattering: mobility reduction parameter with Vg
MPRoz	alphafp2	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafp2 should scale up linearly with sfp2: alphafp2=3.5 for sfp2=65mV/dec

6.11 Field-Plate 3 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfp3	0	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfp3	0.0	0		m	FP Length
MPRnb	vtofp3	-74.5	-600 vtofp2		V	FP threshold voltage
MPRoz	cgfp3	2.0e-4			F/m^2	FP gate-cap/area
MPRnb	tcgfp3	0.0	0		1/K	cgfp3 dependence on temperature
MPIsw	flagfp3s	1	0 1			Flag parameter: cfp3s select=1 or cfp3s not select=0
MPRcz	cfp3s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfp3b	1	0 1			Flag parameter: ccfp3; cbfp3 select=1 or ccfp3; cbfp3 not select=0
MPRcz	ccfp3	0.9e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfp3	0.0	0		1/K	ccfp3 dependence on temperature
MPRcz	cbfp3	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfp3	0.0	0		1/K	cbfp3 dependence on temperature
MPRoz	vx0fp3	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fp3	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafp3	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fp3	0.0	0			FP DIBL Coefficient
MPRoz	sfp3	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfp3	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafp3	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafp3	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafp3	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafp3	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafp3 should scale up linearly with sfp3: alphafp3=3.5 for sfp3=65mV/dec

6.12 Field-Plate 4 parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagfp4	0	0 1			Flag parameter: GFP=1 or SFP=0
MPRcz	lgfp4	0.0	0		m	FP Length
MPRnb	vtofp4	-74.5	-600 vtofp3		V	FP threshold voltage
MPRoz	cgfp4	2.0e-4			F/m^2	FP gate-cap/area
MPRnb	tcgfp4	0.0	0		1/K	cgfp4 dependence on temperature
MPIsw	flagfp4s	1	0 1			Flag parameter: cfp4s select=1 or cfp4s not select=0
MPRcz	cfp4s	0e-19	0		F/m	FP (source-side) to source cap/width
MPIsw	flagfp4b	1	0 1			Flag parameter: ccfp4; cbfp4 select=1 or ccfp4; cbfp4 not select=0
MPRcz	ccfp4	0.9e-10	0		F/m	Source or gate to drain (under FP) cap/width
MPRnb	tccfp4	0.0	0		1/K	ccfp4 dependence on temperature
MPRcz	cbfp4	0.0	0		F/m	Body to drain (under FP) cap/width
MPRnb	tcbfp4	0.0	0		1/K	cbfp4 dependence on temperature
MPRoz	vx0fp4	1.2e5	8e4	3e5	m/s	FP source injection velocity
MPRoz	mu0fp4	0.2	0.08	0.18	m^2/Vs	FP low-field mobility
MPRoz	betafp4	1.00	0.5	3		FP linear to saturation parameter
MPRcz	delta1fp4	0.0	0			FP DIBL Coefficient
MPRoz	sfp4	3.2	0.065		V/dec	FP Sub-threshold slope
MPRcz	ndfp4	0.0	0			FP punchthrough factor for subth slope
MPRnb	vtzetafp4	-0.4e-3			V/K	vto dependence on temperature
MPRcz	vthetafp4	0.0	0		1/V	FP scattering: velocity reduction parameter with Vg
MPRcz	mthetafp4	0.0	0		1/V	FP scattering: mobility reduction parameter with Vg
MPRoz	alphafp4	1e-2	1e-3	5		FP weak to strong inversion transition factor; NOTE: alphafp4 should scale up linearly with sfp4: alphafp4=3.5 for sfp4=65mV/dec

6.13 Gate leakage parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	igmod	0	0	1		Flag parameter for gate leakage 0=off; 1=on
MPRcz	fracig	0	0	1		Fraction of IG de-biased through FP Transistors
MPRcz	vjg	1.1	0.9	1.5	V	Gate diode cut in voltage
MPRcz	pg-param1	820e-3	1e-3	1	1/V	Temperature coefficient of exponent
MPRcz	pg-params	1.00	0.1	5		G-S diode inverse of ideality factor
MPRcz	ijs	1.00e-12	1e-15	1e-10	A/m	G-S reverse leakage current normalized to width
MPRcz	vgsats	1.00	0	5	V	G-S high injection effect onset voltage
MPRcc	fracs	0.5	0	1		G-S fractional change in ideality factor due to high injection
MPRoz	alphags	1.0	0.9	1.5		G-S high injection smoothing parameter; smaller is less smoothing
MPRcz	pg_paramd	1.00	0.1	5		G-D diode inverse of ideality factor
MPRcz	ijd	1.00e-12	1e-15	1e-10	A/m	G-D reverse leakage current normalized to width
MPRcz	vgsatd	1.00	0	5	V	G-D high injection effect onset voltage
MPRcc	fracd	0.5	0	1		G-D fractional change in ideality factor due to high injection
MPRoz	alphagd	1.0	0.9	1.5		G-D high injection smoothing parameter; smaller is less smoothing
MPRcz	pgsrecs	0.5	0.1	5		G-S diode inverse of ideality factor reverse recombination
MPRcz	irecs	1.0e-18	1e-19	1e-10	A/m	G-S reverse leakage current normalized to width
MPRoz	vgsatqs	2.00	0	5	V	G-S mimics depletion saturation; effective maximum voltage
MPRoz	betarecs	2.00	0	600		G-S linear to saturation parameter; smaller is slower saturation
MPRcz	pgsrecd	0.8	0.1	5		G-D diode inverse of ideality factor for reverse recombination
MPRcz	irecd	2e-5	1e-19	1e-10	A/m	G-D reverse leakage current normalized to width
MPRoz	vgsatqd	0.8	0	5	V	G-D mimics depletion saturation; effective maximum voltage
MPRoz	betarecd	0.25	0	600		G-D linear to saturation parameter; smaller is slower saturation
MPRcz	kbdgates	0	0	1		G-S fitting parameter to turn on the breakdown of G-S diode
MPRcz	vbdgs	600	0	600	V	G-S soft breakdown voltage of G-S diode
MPRcz	pbdgs	4.00	1	5	1/V	G-S fitting parameter for breakdown: inverse of ideality factor
MPRcz	kbdgated	0	0	1		G-D fitting parameter to turn on the breakdown of G-D diode
MPRcz	vbdgd	600	0	600	V	G-D soft breakdown voltage of G-D diode
MPRcz	pbdgd	4.00	1	5	1/V	G-D fitting parameter for breakdown: inverse of ideality factor
MPIsw	igrecmod	0	0	1		Flag parameter to turn on secondary gate-recombination current 0=off; 1=on
MPRcz	pgsrecs2	0.5	0	1		Secondary G-S diode inverse of ideality factor reverse recombination
MPRcz	irecs2	1.0e-18	1e-19	1e-10	A/m	Secondary G-S reverse leakage current normalized to width
MPRoz	vgsatqs2	2.00	0	5	V	Secondary G-S mimics depletion saturation
MPRoz	betarecs2	2.00	0.7	3		Secondary G-S linear to saturation parameter

MPRcz	pgsrecd2	0.8	0	1		Secondary G-D diode inverse of ideality factor for reverse recombination
MPRcz	irecd2	2e-5	1e-19	1e-10	A/m	Secondary G-D reverse leakage current normalized to width
MPRoz	vgsatqd2	0.8	0	5	V	Secondary G-D mimics depletion saturation
MPRoz	betarecd2	0.25	0.7	3		Secondary G-D linear to saturation parameter

6.14 p-GaN junction parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	flagpgan	0	0 1			Flag parameter for p-GaN calculations 0=off; 1=on
MPRcz	pg.param_pgan	0.05	0 1			p-GaN forward diode inverse of ideality factor
MPRcz	ij_pgan	2e-5	1e-15 1e-4		A/m	p-GaN forward diode leakage current normalized to width
MPRcz	vgsat_pgan	3	0 10		V	p-GaN high injection effect onset voltage
MPRcc	frac_pgan	0.4	0 1			p-GaN fractional change in ideality factor due to high injection
MPRoz	alphag_pgan	1.0	0.9 1.5			p-GaN high injection smoothing parameter; smaller is less smoothing
MPRcz	pgsrec_pgan	0.5	0 1			p-GaN diode inverse of ideality factor reverse recombination
MPRcz	irec_pgan	1e-21	1e-25 1e-6		A/m	p-GaN reverse leakage current normalized to width
MPRoz	vgsatq_pgan	2e4	0		V	p-GaN mimics depletion saturation; effective maximum voltage
MPRoz	betarec_pgan	1	0.5 10			p-GaN linear to saturation parameter; smaller is slower saturation
MPIsw	pganrecmod	0	0 1			Flag parameter to turn on secondary gate-recombination current for p-Gan 0=off; 1=on
MPRcz	pgsrec_pgan2	0.5	0 1			Secondary p-GaN diode inverse of ideality factor reverse recombination
MPRcz	irec_pgan2	1e-21	1e-25 1e-6		A/m	Secondary p-GaN reverse leakage current normalized to width
MPRoz	vgsatq_pgan2	2e4	0		V	Secondary p-GaN mimics depletion saturation; effective maximum voltage
MPRoz	betarec_pgan2	1	0.5 10			Secondary p-GaN linear to saturation parameter; smaller is slower saturation
MPRoz	vcsh0	2.0	0 10		V	Built in potential of p-GaN Schottky junction
MPRcz	csh0	6e-8	1e-10 1e-5		F/m	p-GaN zero bias Schottky junction capacitance
MPRco	fc	0.5	0 0.9			Fractional change in voltage across p-Ga between 0 and vesh0 before Taylor series
MPIcc	pgancshorder	2	2 5			Order of Taylor series to compute p-GaN charge beyond fc*vcsh0
MPRcz	rsch0	0	0 100		Ohm*m	Ohmic contact for the Schottky junction normalized to width
MPRcc	ohmicratio	0	0 0.1		m	Fraction of device width that is ohmic; wsch = w * ohmicratio

6.15 Channel-breakdown parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	icbmod	0	0 1			Flag parameter for channel breakdown 0=off; 1=on
MPIsw	cbddbmod	1	0 1			Flag parameter for channel breakdown debiasing 0=off (to s & d)
MPRcz	ijscbd	1.00e-9	1e-12		A/m	S-D reverse channel breakdown leakage current normalized to width
MPRcz	vchbdgs	50	0		V	S-D soft breakdown voltage of channel diode
MPRcz	pchbdgs	4.00	1		1/V	S-D fitting parameter for channel breakdown: inverse of ideality factor
MPRcz	ijdcbd	1.00e-9	1e-12		A/m	D-S reverse channel breakdown leakage current normalized to width
MPRcz	vchbdgd	50	0		V	D-S soft breakdown voltage of channel diode
MPRcz	pchbdgd	4.00	1		1/V	D-S fitting parameter for channel breakdown: inverse of ideality factor

6.16 Thermal sub-circuit parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	rth	25	0 100		K/W	Thermal resistance
MPRcz	cth	1e-4	0 1e-3		s*W/K	Thermal capacitance

6.17 RF gm-dispersion parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	gmdisp	0	0 1			Flag parameter for gm-dispersion 0=off; 1=on
MPRcz	taugmrf	1e-3	0 1e-3		s	gm-dispersion time constant

6.18 Layout and DC-to-RF gate-resistance parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	rgsp	0.0	0 10		Ohms/m	Gate resistance / Width for 1 finger and 1 gate-contact
MPRoz	ngcon	1	1 3			Number of gate-contacts per finger
MPRcz	lovg	0	0 1e-6		m	Length of gate-finger line between gate-contact and the beginning of active gate-width
MPRcz	agate	1	0 0.33			DC-to-RF dispersion factor; fraction=1 DC value maintained at all frequencies

6.19 Trapping model parameters for Ron and Isat increase

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIcc	trapselect	0	0	2		Select knob for charge trapping 0=off; 1=Rdson trapping on; 2=Isat and Rdson trapping on
MPRoz	rintrap1	1e9	0		Ohm	Input trapping shunt resistance
MPRcz	ctrap	1e-3	0	1	F	DC-block capacitor
MPRcz	vttrap	100		800	V	Trapping stress threshold voltage
MPRcz	taut	3e-5	1e-6	1e-4	s	Trap time constant
MPRcz	alphat1	1e-3	0			Trap coefficient 1 on bias stress
MPRoz	alphat2	0.05	0		V	Trap coefficient 2 on bias stress
MPRoz	alphat3	1e-3	0			Input trapping feedback factor
MPRcz	tempt	1e-4			1/K	Temperature coefficient for trapping
MPRoz	vgltrapth	10			V	Trapping Drain-lag stress threshold voltage
MPRoz	vdltrapth	100			V	Trapping Gate-lag stress threshold voltage
MPRoz	rcapture	10.0	remission		Ohm	Trapping capture time constant associated with capture of electron (a slower process)
MPRoz	remission	50e-3	0	rcapture	Ohm	Trapping emission time constant associated with emission of electron (a faster process)
MPRoz	cdlag	1e-6			F	Trapping emission and capture time constant-C
MPRnb	rct1dl	-5e-3			1/K	Linear Drain-lag temperature coefficient
MPRnb	rct1gl	5e-3			1/K	Linear Gate-lag temperature coefficient
MPRnb	rct2dl	0.0			1/K^2	Quadratic Drain-lag temperature coefficient
MPRnb	rct2gl	0.0			1/K^2	Quadratic Gate-lag temperature coefficient
MPRcz	isat	1.0e-9			A	Trapping reverse saturation current for diode

6.20 Noise model parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPIsw	noisemod	0	0	1		Select knob for noise model 0=off; 1=on
MPRcz	shs	3.0		3		G-S shot noise parameter
MPRcz	shd	3.0	1	3		G-D shot noise parameter
MPRcz	kf	1.0e-4	0	1e-2		Flicker noise coefficient
MPRcz	af	2.0	1	2		Flicker noise exponent
MPRoz	ffe	1.2	1	2		Flicker noise exponent for frequency

6.21 Minimum element parameters

Macro	Parameter	Default Value	Typical Min and Max Value*		Units	Description
MPRcz	minr	1e-3	0	1e-3	Ohm	Minimum resistance
MPRcz	minl	1.0e-9	0	1e-9	m	Minimum length of access or FP regions for modeling them as transistors
MPRcz	minc	0.0	0	1e-15	F	Minimum capacitance

*The typical minimum and maximum values provided here are a subset of the range of allowed parameter values. They are based on the typical values that the model developers observed while fitting the model to several GaN-HEMT technologies. They are by no means exclusive. The full-allowed range is defined in the Verilog-A code itself.

7 MVSG Version History

V4.0.0 (2024-02-01)

Added

- p-GaN Module Functionality
 - High injection in forward mode current & associated parameters: *vgsat_pgan*, *frac_pgan*, *alphag_pgan*
 - Reverse recombination voltage saturation & associated parameters: *vgsatq_pgan*, *betarec_pgan*
 - Secondary reverse recombination current allowing modeling of “double-saturation” behaviour & associated parameters: *pganrecmod*, *pgsrec_pgan2*, *irec_pgan2*, *vgsatq_pgan2*, *betarec_pgan2*
 - Ohmic junction allowing hybrid p-GaN implementation & associated parameters: *rsch0*, *ohmicratio*
 - p-GaN parameters grouped by functionality
- Gummel Symmetry Compliance
 - New parameter *flaggum* which uses $x \tanh(x)$ smoothing for functions **absfunc** & **mmax**
 - Improvement in differentiability in current at $V_{DS} = 0\text{ V}$ up to fifth derivative when *flaggum*=1
 - New parameter *mmaxs* which controls level of smoothing in function calls to **absfunc** & **mmax**
 - Parameter *beta*=2 by default (use even values to ensure Gummel symmetry passes)
 - SAR & DAR source voltage uses smoothing function when *flaggum*=1
- New parameter macros: MPRcc, MPIcc; utilized by many existing and new parameters

Changed

- p-GaN Capacitance (C_{sch}) Model Changed
 - New formulation conserves charge fully, while *csh0* parameter uses more intuitive units, and permits more clamping options when bias approaches built in potential of Schottky junction (*vcsh0*)
 - For users coming from V3.2.0, apply $csh0(V4.0.0) = \frac{csh0(V3.2.0)}{\sqrt{vcsh0}}$ to maintain same capacitance values in region of interest (specifically, when $V(gi2p, gi2) \leq fc * vcsh0$)
 - Theoretical charge formulation equations cause blow up of capacitance when bias approaches built in potential of Schottky junction (*vcsh0*). Previous formulation clamped capacitance to a fixed constant value. Revised formulation extends domain with a Taylor series (starting at voltage determined by parameter *fc*) of order defined by parameter *pgancshorder*.

- Default p-GaN diode parameters changed such that IV characteristics match reversed gate diode default parameters
- New High Injection Formulation in ***calc_ig***
 - More physical behaviour and easier to extract parameters
 - Forward current is always monotonic no matter the values of high injection parameters
 - Parameters retain same meanings but previous fits will need to be re-extracted
 - Changes are done on ***calc_ig*** affecting all function calls to it
 - Fully compatible with all other gate leakage functionality including reverse recombination current & breakdown
- Minimum resistance *minr* can be set to zero, compliant with new CMC guidelines
- Gate leakage parameters reorganized and grouped by functionality
- Updated *rcapture* and *remission* parameter descriptions for clarity

Fixed

- Small amount of charge non-conservation in p-GaN capacitance when time stepping due to bias dependent capacitance
- White noise calculations only calculated and contributed for internal gate diodes and not on external gate diodes
- Unused internal nodes not tied off when *trapselect* = 1 or 2
- ***calc_capt*** function returns output value twice, once as function output and once as return value
- Extra nesting in ***explim*** function removed (does not affect model functionality)

V3.2.0 (2023-04-20)

Added

- p-GaN Module
 - Parameters related to p-GaN junction diode and junction capacitor
 - New node **gi2p**: from top to bottom we have nodes **G**, **gi1**, **gi2**, **gi2p**
 - Local variables related to floating p-gan behavior: **idsh**, **idshsat**, **idshrec**, **csh**
 - **idsh** calculation, **csh** calculation and contribution
 - Collapse of **gi2** and **gi2p** if p-GaN calculations are off *flagpgan=0*
- Externally Accessible thermal node **dt**

Changed

- Any connection to **gi2** in V3.1.0 is now connected to **gi2p** except field plate gate connections (for both source and gate field plates)

- All field plate voltage definitions remain to **gi2** so they connect to outside of the p-GaN layer

V3.1.0 (2022-07-17)

Added

- A complete overhaul to the trapping module allowing two time constants to be set for trapping and de-trapping
 - $trapselect=0$ (no trapping), $trapselect=1$ (R_{DSon} increase), $trapselect=2$ (I_{SAT} and Q_G reduction)
 - Drain lag and gate lag sub circuits added: transient dependence on V_D and V_G
 - Both emission and capture mechanisms included: $\tau_{emission}$ and $\tau_{capture}$
 - Changes R_{DSon} , I_{SAT} under switching conditions when activated
 - Added linear and quadratic temperature coefficients for $\tau_{emission}$ and $\tau_{capture}$ time constants
 - Uniform branch current based assignments in $trapselect=2$ model
 - $trapselect$ set as model parameter, $n_{gf}=1$ QA test added
- $igmod=1$ & $cth=0$, QA test bias points reduced for faster simulation

V3.0.0 (2021-09-08)

Added

- Parameter $flagsp$ added to include/exclude V_T variation with surface potential
- Gate diode assignment changed from internal (**si**, **di**) nodes to external (**fps4**,**fp4**) as default
- $fracig$ parameter added to allow fraction of I_G to be debiased through FP transistors
- Bias dependence added to fringing capacitances: No further need to add “dummy” FPs

Changed

- Flicker noise model updated to work for $V_{DS} < 0$
- Channel breakdown de-biasing turned on by default: $cbddbmod=1$
- $minr$ parameter definition updated
- Added a note to scale $alpha$ with SS of transistors to avoid discontinuities in CV transitions
- Added clamps for $\log(1+\exp())$ terms in charge calculations that are differentiable

Fixed

- Default trapping model convergence issue solved

- Bug in rsh parameter definition corrected to exclude $rsh=0$
- Corrected the bias dependence of fringing capacitances

V2.1.0 (2020-09-14)

Added

- Channel breakdown diode-current de-biased through contact resistances
- Temperature coefficients added to fringing, channel, and FP capacitances
- Different temperature coefficients added to vto of field plates

Changed

- $gmin$ default set to 0
- Multiple internal variables associated with breakdown currents and access transistor current and charge are initialized to 0.

Fixed

- $agate$ parameter changed to unitless
- bug on source side FP flag parameters corrected

V2.0.0 (2020-02-18)

- OMI and aging parameters updated

V1.2.0 (2019-12-04)

- FPs added on source side
- Channel breakdown model added
- Bug in gate resistance scaling with W and ngf corrected
- Module to include gate line delay: DC to RF gate resistance change
- Optimization of function calls to some temperature dependent functions
- Default parameters in Verilog-A code updated

V1.1.0 (2018-07-18)

- V_T and V_{Dsat} OP-points added
- $type$ parameter corrected to support P-FETs
- Access region V_{DS} -swapping bug corrected
- Inductor vs. Capacitor implementation for channel NQS or gm-dispersion effect

V1.0.0 (2018-04-30)

- Basic code release with 4 FPs and simple rth , cth , and $igmod$

8 Parameter Extraction Procedure for MVSG Model

The following flowchart shows the sequence of extraction procedure of important parameters of MVSG model.

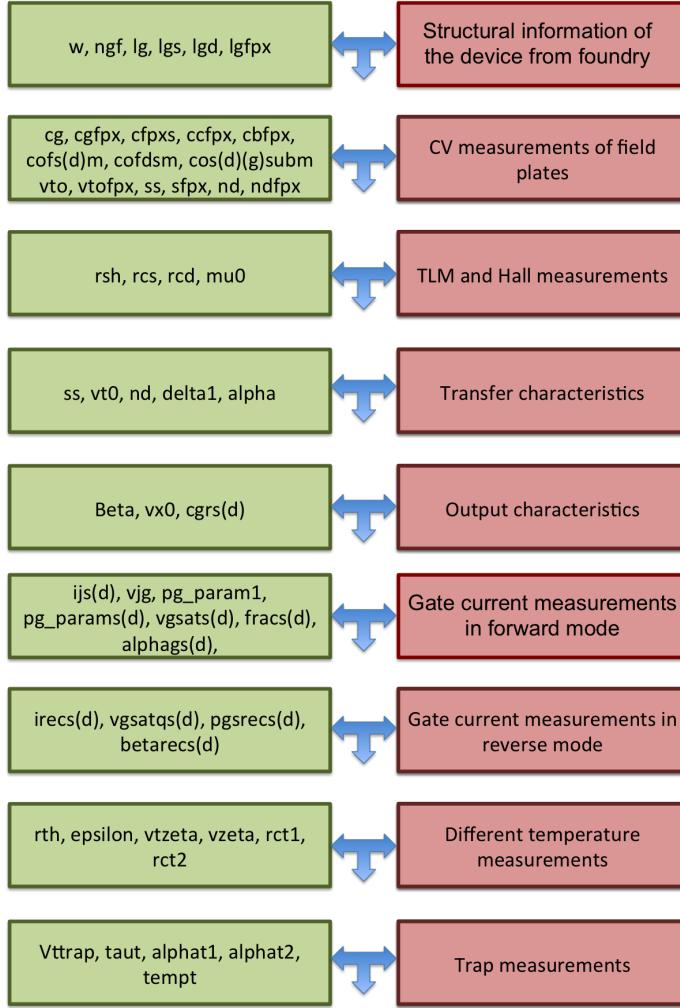


Figure 39: Flowchart showing parameter extraction flow. This is not the exhaustive list of parameters but the most significant ones. Most of the other parameters are either fitting parameters or constants for GaN HEMT. All parameters will be discussed.

8.1 Device Parameters

Geometry and structural information are best provided by foundry. For the model, geometry parameters needed are: Gate length (L_g), Source access region (L_{gs}), drain-access region length (L_{gd}), device-width (W). In addition, parameters related to field plate such as field plate length (L_{gfpx}), inter-layer dielectric thickness etc. will be necessary for modeling. Other additional useful parameters required by the model are: Low field mobility (μ_o), Contact resistance (R_c) and sheet resistance (R_{sh}), 2DEG density. If these are not provided, additional measurements might be needed to extract them. μ_o and R_{sh} extraction would

require Hall measurements and special hall structures. R_c can be extracted by measuring resistances of TLM structures of different lengths and extracting the offset at $L_g = 0$. Correct extraction of these parameters can also be verified from R_{on} match in output characteristics.

8.2 C_g Extraction

C_g is an important model parameter in MVSG model. Its accurate extraction is essential for correct modeling. C_g must be extracted from CV measurements rather than from analytical calculation. Accurate analytical calculation must also include quantum correction as charge centroid in 2DEG is shifted away from the interface. This needs dedicated calculations/simulation, which from a compact modeling perspective might not be critical as long as we can directly measure the capacitance. To get C_g , two terminal CV (with $V_{DS} = 0$) of devices with different gate length but identical widths and access region lengths must be measured. The gate to channel capacitance in strong accumulation scales as a function of L_g . From the slope we get the value of C_g (areal gate capacitance) and the intercept gives the parasitic capacitance. Parasitic capacitance includes outer fringing capacitance (C_{of}) and pad parasitic. To remove the pad parasitic, we need CV of open test structures.

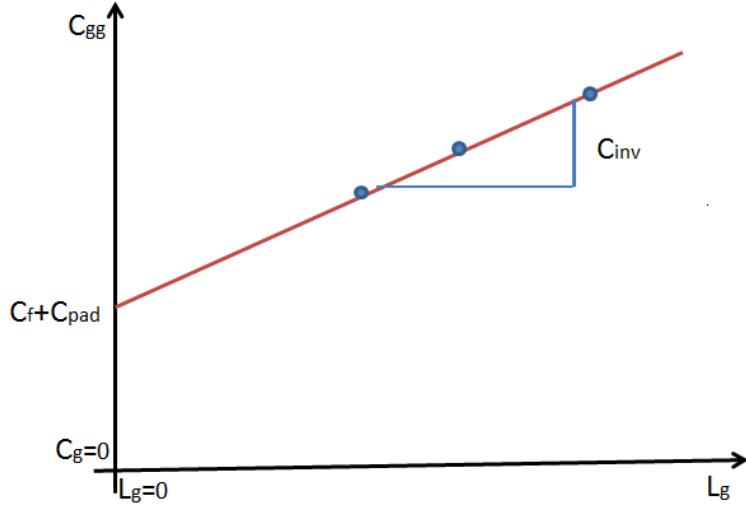


Figure 40: Illustration of extraction of C_g devices of different gate lengths

8.3 Device Parameters for FPs

Geometry and structural information of field plates along with their configuration are best provided by foundry. For the FP model, the only geometry parameter needed is gate length of FPs (L_{gfp}). It is the length of the FP metal, which has direct control over the 2DEG under it. So if a SFP metal runs from the source contact over the intrinsic-gate metal and gate FP metal, the SFP gate length is only that length of the SFP metal that extends beyond the edge of the GFP metal to its edge (where there is no other metal between it and the 2DEG).

8.4 Extraction of Parameters from C_{ISS} vs. V_G Measurements

Gate capacitance measurements vs. V_G at $V_{DS} = 0$ V will yield the areal gate capacitances and V_T s of all gate-connected field plates. This is shown in Fig. 41 where at $V_G = \text{vto}$ of the FET can be obtained and the step in CV curve at this V_G normalized to the width and gate-length (which are known) gives cg the areal gate-capacitance. Similarly the transition at $V_G = -50$ V the figure is due to the depletion of the GFP1 occurring at its V_T (vtوفp1) and the areal gate-capacitance (cgfp1) is the step in the CV curve at that V_G . In addition, the electrostatic parameters such as sub-threshold slope sfp1 can be obtained from the slope of transition. The off-state capacitance obtained from calibrated CV measurements yields the total metal capacitances associated with gate terminal ($\text{cofsm} + \text{cofdm}$). Individual components can then be obtained from C_{gs} and C_{gd} measurements using bias-Ts to apply the DC bias.

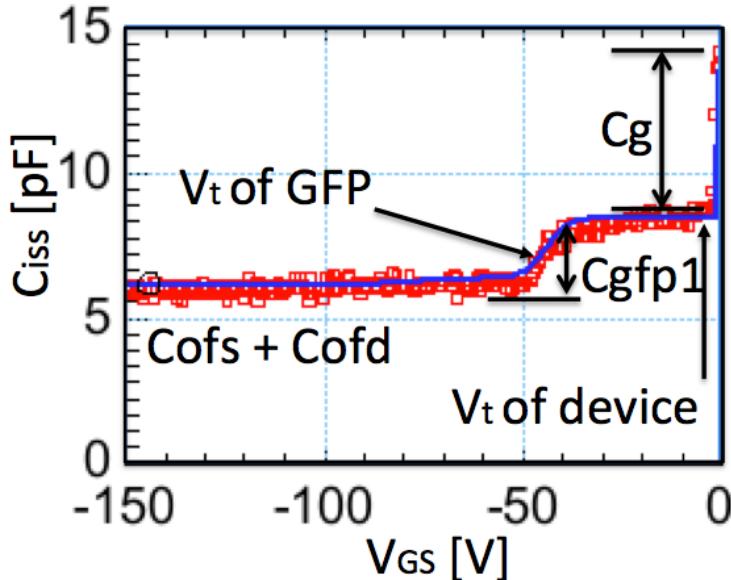


Figure 41: Illustration of extraction of gate-field plate parameters of devices from C_{iss} vs. V_g measurements

8.5 Extraction of Parameters from C_{OSS} , C_{RSS} , C_{ISS} vs. V_D Measurements

Input, output and reverse transfer capacitance measurements vs. V_D in off-state will yield the areal gate capacitances, cross-coupled capacitances and V_T s of all field plate transistors. Fig. 42 shows representative C_{iss} , C_{oss} and C_{rss} plots which shows transitions at $V_D = V_T$ s of different field plates which are due to depletion of these transistors. From C_{iss} (or C_{rss}) the areal gate capacitances of GFP transistors (cgfp1) (can be cross-checked from previous plot) and cross-coupled capacitances of SFP transistors (ccfp2) can be obtained. Metal capacitances between gate- and other terminals (cofs , cofd , cofgsub) of the device can be extracted as well. From C_{oss} plot, the capacitances associated with the source terminal can be obtained, which includes the areal-gate capacitances of SFP transistors (cgfp2) and

cross-coupled capacitances of GFP transistors (**ccfp1**) along with the metal capacitances associated with source-drain terminals (**cofds**).

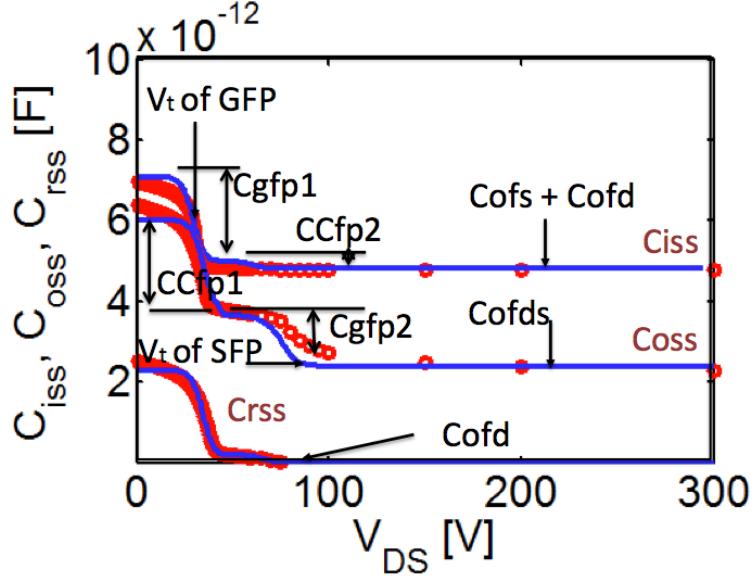


Figure 42: Illustration of extraction of field plate parameters of devices from capacitance vs. drain voltage measurements

This completes the important parameter extraction flow for the field plates of GaN HEMT. The transport parameters associated with the field plates should be kept the same as those extracted from the IV characteristics for the intrinsic transistor, unless model fits demand that they be set different. However usually parameters such as mobility, carrier velocity do not change for different transistors in the model sub-circuit. Stand-alone FP transistors or test-structures with devices having the FP connections whose gate-bias can be independently controlled can used to get a more accurate estimate of electrostatic and transport parameters of FPs.

8.6 Extraction of Tempcos of CV Measurements

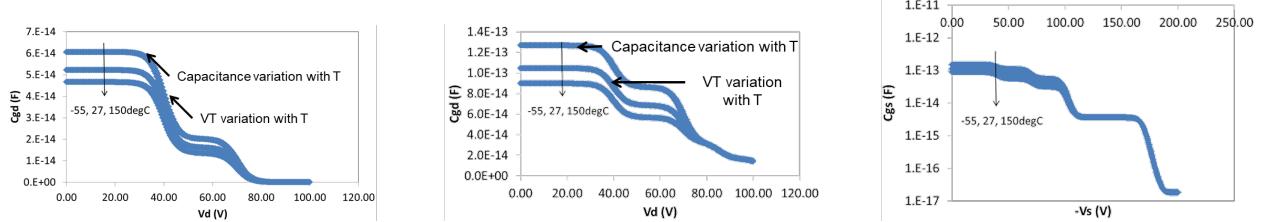


Figure 43: Extraction of Tempcos in channel-, FP- and fringing-capacitances; both their values and V_{TS}

Linear variation of threshold voltages and on-state capacitance-values of channel-, FP-, and fringing-capacitances are implemented in the model. These can be extracted from multi-

temperature measurements of C_{iss} , C_{rss} , C_{oss} measurements. Atleast two-temperatures are required for extraction of tempcos and a third T-measurement is useful for benchmarking the accuracy of the T-dependent charge-model.

8.7 Extraction of V_{TO} , S and DIBL (Delta 1)

Threshold voltage (V_t) computation requires knowledge of piezoelectric charges at the interface, heterostructure composition and thickness. Again the model is simplistic in the sense that V_{to} needed for the model can be extracted from device data. The requirement is one data point (V_G , I_D , V_D) in weak accumulation (just beyond strong to weak accumulation transition) at low V_D ($\sim 0V$ where DIBL has negligible impact). Alternately V_{to} can be approximated as V_G at the same (V_G , I_D , V_D) point on transfer curve.

Sub threshold slope (S) is obtained from the slope of the transfer curve on log scale in weak accumulation regime. Low V_D is preferred to avoid shift of S due to modest punch through in the device. The parameter extracted must make sense for the L_g of the device. DIBL is extracted from the lateral shift of I_D (due to shift of V_t) as V_D is increased in the transfer curves in weak accumulation. DIBL is multiplied by intrinsic drain voltage (V_{Di}) in the expression for threshold voltage in the model. It can be extracted from the weak accumulation regime as shown.

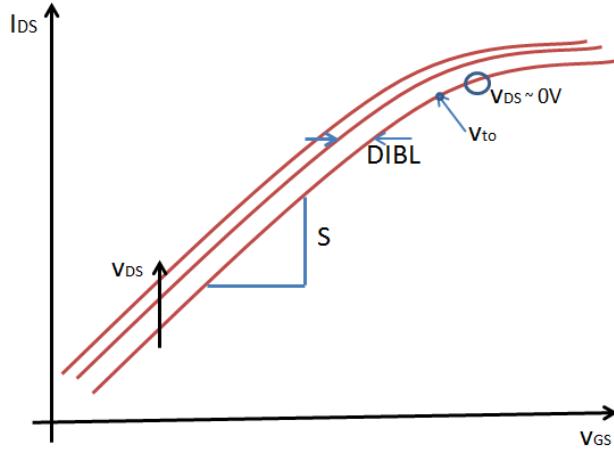


Figure 44: Illustration of extraction of V_{to} , S and DIBL from transfer curves

8.8 Extraction of v_{sato}/v_{xo} , β (beta) and θ_v (vtheta), θ_μ (mtheta) and R_{th}

v_{sato}/v_{xo} , β and θ_v , θ_μ and R_{th} can be extracted from output characteristics. v_{sato}/v_{xo} can be fitted to get accurate match with saturation current level. v_{xo} extracted must lie between the bracket of peak electron velocity (2.5×10^7 cm/s) and saturation velocity (1.3×10^{10} cm/s) depending on gate length. The transition from linear to saturation current in output characteristics is governed by F_{sat} which has a parameter β . β should ideally lie between 1.5-3 for these type of HEMTs depending on saturation.

η_v is thermal coefficient affecting velocity. They can be extracted from slope of output curves in saturation at large V_g where self-heating is dominant. η_v together with the thermal resistance (R_{th}) is directly responsible for the negative slope of the output curves and can be extracted from fitting. θ_v and θ_μ are also fitting parameters which affect V_{DSAT} . They can be extracted from V_{DSAT} at lower V_{GS} when self-heating has not yet kicked in. Thus by fitting to get correct linear-to-saturation transition voltages at larger V_{GS} we can get values of θ_v and θ_μ . R_{th} of the thermal network is also obtained in high bias-region where self-heating is predominant. Since R_{th} characterization through TCAD and evaluation of thermal coefficients through multi-temperature measurements has not been done yet, it has been reduced to a fitting parameter for now.

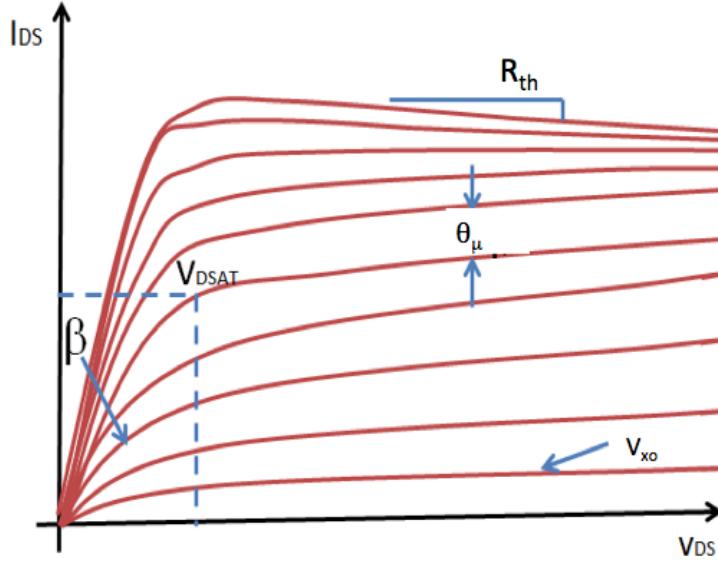


Figure 45: Illustration of extraction v_{sato}/v_{inj} , β and θ_v , θ_μ , R_{th} and η_v from output curves

The implicit-gate transistors on the source and drain access regions should ideally have same transport parameters as that of other transistor regions. The short channel effect parameters and sub-threshold slopes of these regions are fitting parameters or can be extracted from TLM measurements. The key parameters for these transistor regions are the **cig** (implicit-gate capacitance) parameters, which affect the quasi-saturation behavior in high V_g regimes in the output characteristics.

8.9 Extraction of Gate Current Parameters

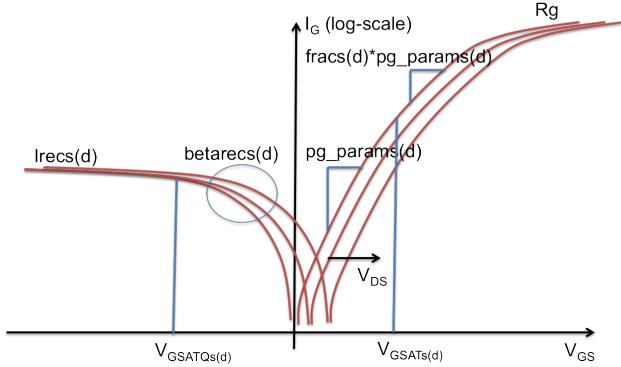


Figure 46: Illustration of extraction gate current parameters from gate-current curves

The gate current parameters such as ideality factors (**`pg_params(d)`**, **`pg_param1`**), reverse saturation currents (**`irecs(d)`**, **`ijg`**), along with reverse current parameters (**`Vgsatqs(d)`**, **`betarecs(d)`**) can be extracted from gate-current plots.

In addition to the parameters in the model, additional passives associated with the device such as terminal resistances, inductances and pad capacitances are critical to capture small and large signal device characteristics at RF frequencies. Since these device-level parasitics are layout and process dependent, it is not included as part of the model file. Instead they are to be added at the schematic level. While this is not necessary for power conversion applications and hence Toshiba HV-GaN HEMTs, it is critical for RF devices and for Qorvo device data for fitting S-parameter, power sweep, source and loadpull data. The schematic and values are in the ADS files are attached in the release. This section gives a rough idea of the model parameters of MVSG model and the regions of the terminal characteristics that are significantly impacted by these parameters for easy extraction.

Primary and Secondary-recombination models

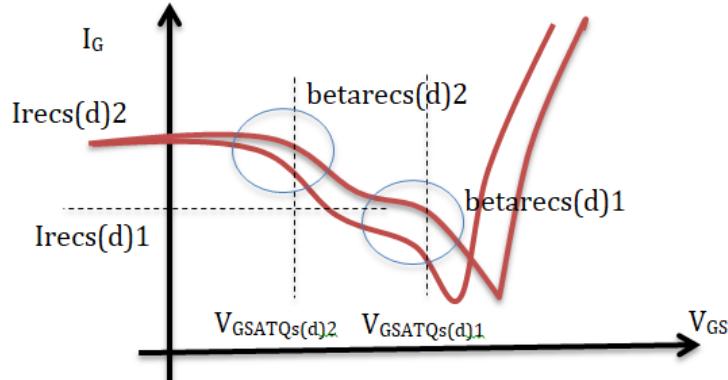


Figure 47: Illustration of extraction gate current parameters from gate-current curves

The recombination gate current can have “double-saturation” characteristics as illustrated in Fig. 47. Two model-calls are done to the recombination-gate-current mod-

ule. The saturation voltages (**Vgsatqs(d)1**, **Vgsatqs(d)2**), the saturation-smoothness parameter (**betarecs(d)1**, **betarecs(d)2**) and the reverse-recombination saturation currents (**irecs(d)1**, **irecs(d)2**) are extracted from different regions as highlighted.

8.10 Extraction of Noise Parameters

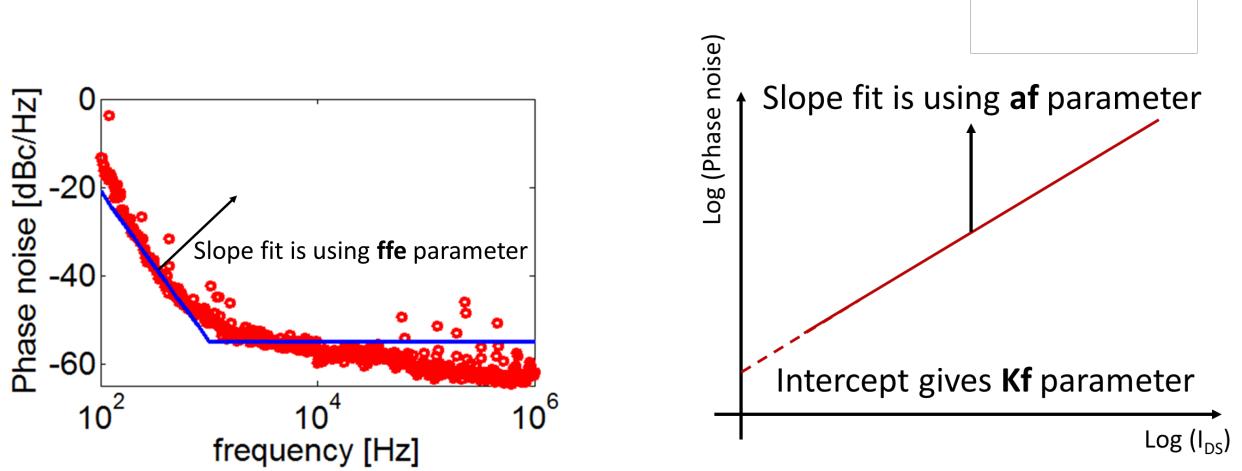


Figure 48: Illustration of extraction of flicker noise parameters from phase noise

The flicker noise parameters are frequency slope (**ffe**), current dependence (**Kf** and **af** for **current-dependence: exponent and pre-factor**).

The nature of traps determine **ffe** parameter: the slope of low-frequency phase noise skirts which can be measured from frequency spectra at base-band or up-converted spectra through a simple oscillator as shown in Fig. 48(a). The Leeson's model which is adopted here has a pre-factor and exponent term for the drain current. The bias-dependence is captured indirectly via the drain-current through the MVSG model. However, the pre-factor (**Kf**) and exponent terms (**af**) can be determined from phase noise spectra vs. I_{DS} for a given frequency-offset as shown in Fig. 48(b).

For the RF-noise model, the Johnson's noise model requires no additional parameters for thermal noise from channel and access regions. The small-signal and DC model extraction will suffice to give accurate estimations of RF-noise from these resistive regions. The only parameters that impact RF-noise that require separate extraction are the shot noise parameters (**shs** and **shd**) which requires RF-noise figure plotted against gate-current at $V_{DS} = 0$ V. Ideally $shs=shd=1$ but from past measurements the shot-noise is higher than that resulting out of those values.

In addition to the parameters in the model, additional passives associated with the device such as terminal resistances, inductances and pad capacitances are critical to capture small and large signal device characteristics at RF frequencies. Since these device-level parasitics are layout and process dependent, it is not included as part of the model file. Instead they are to be added at the schematic level. While this is not necessary for power conversion applications and hence Toshiba HV-GaN HEMTs, it is critical for RF devices and for Qorvo device data for fitting S-parameter, power sweep, source and loadpull data. The schematic

and values are in the ADS files are attached in the release. This section gives a rough idea of the model parameters of MVSG model and the regions of the terminal characteristics that are significantly impacted by these parameters for easy extraction.

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