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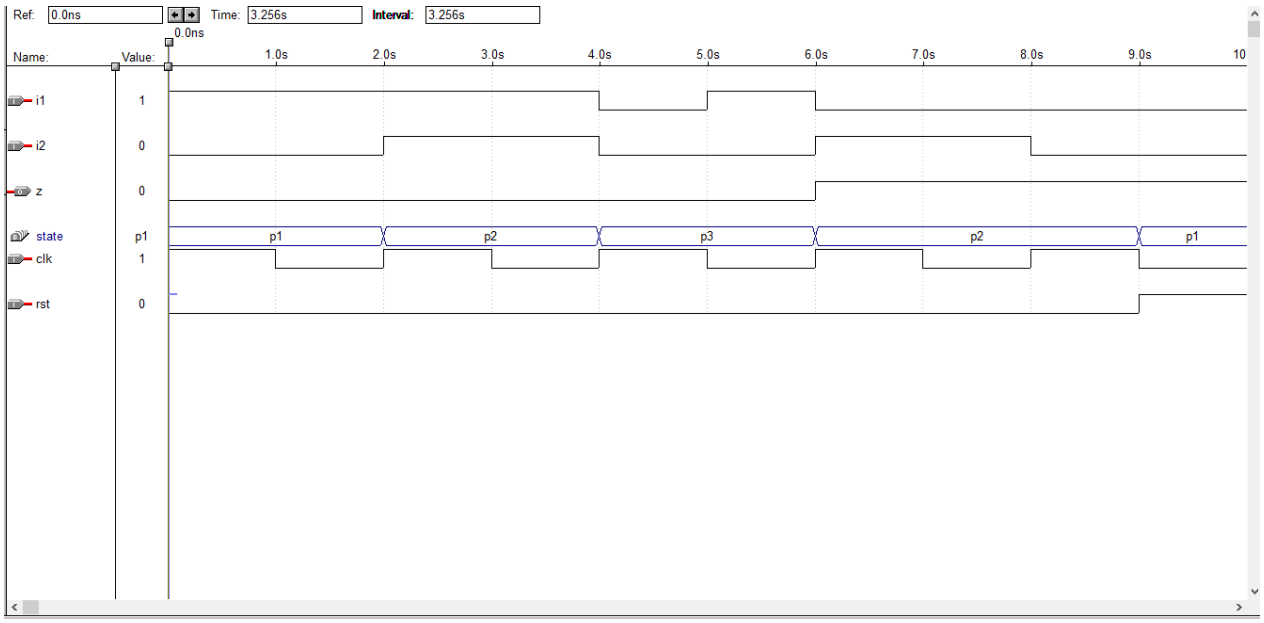
Partie 1 :

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY devoir IS
    PORT (
        i1, i2, clk, rst : IN STD_LOGIC;
        z : OUT STD_LOGIC);
END devoir;

ARCHITECTURE behavioral OF devoir IS
    TYPE etats IS (p1, p2, p3, p4);
    SIGNAL state : etats;

BEGIN
    PROCESS (clk, rst)
    BEGIN
        IF (rst = '1') THEN
            state <= p1;
        ELSIF (clk = '1' AND clk'event) THEN
            CASE state IS
                WHEN p1 =>
                    IF (i1 = '0' AND i2 = '0') THEN
                        z <= '0';
                        state <= p1;
                    ELSIF (i1 = '1' AND i2 = '0') THEN
                        z <= '0';
                        state <= p2;
                    ELSIF (i1 = '0' AND i2 = '1') THEN
                        z <= '1';
                        state <= p4;
                    END IF;

                WHEN p2 =>
                    IF (i1 = '1' AND i2 = '0') THEN
                        z <= '0';
                        state <= p2;
                    ELSIF (i1 = '0' AND i2 = '0') THEN
                        z <= '1';
                        state <= p1;
                    ELSIF (i1 = '1' AND i2 = '1') THEN
                        z <= '0';
                        state <= p3;
                    END IF;

                WHEN p3 =>
                    IF (i1 = '1' AND i2 = '1') THEN
                        z <= '0';
                        state <= p3;
                    ELSIF (i1 = '1' AND i2 = '0') THEN
                        z <= '1';
                        state <= p2;
                    ELSIF (i1 = '0' AND i2 = '1') THEN
                        z <= '0';
                        state <= p4;
                    END IF;

                WHEN p4 =>
                    IF (i1 = '0' AND i2 = '1') THEN
                        z <= '0';
                        state <= p4;
                    ELSIF (i1 = '1' AND i2 = '1') THEN
                        z <= '1';
                        state <= p3;
                    ELSIF (i1 = '0' AND i2 = '0') THEN
                        z <= '0';
                        state <= p1;
                    END IF;
            END CASE;
        END IF;

    END PROCESS;

END ARCHITECTURE;
```



Partie 2 :

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY devoir_p2 IS
    PORT (
        clk, clr : IN STD_LOGIC;
        e : IN STD_LOGIC;
        q : OUT STD_LOGIC_VECTOR(2 DOWNTO 0)

    );
END devoir_p2;
ARCHITECTURE behavioral OF devoir_p2 IS
    SIGNAL qs : STD_LOGIC_VECTOR(2 DOWNTO 0);
BEGIN

    PROCESS (clk, clr)
    BEGIN
        IF clr = '1' THEN
            qs <= "000";
        ELSIF clk'event AND clk = '1' THEN
            qs(2) <= e;
            qs(1 DOWNTO 0) <= qs(2 DOWNTO 1);
        END IF;
    END PROCESS;
    q <= qs;

END behavioral;
```