University of Pisa
Computer Engineering

Digital System Design Project

APPROXIMATION OF COMPLEX NUMBER MODULE BY ACTIVE HDL

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Introduction

A complex number is represented in several way. One of these is the following: $P+iQ$ where P is the real part and Q is the imaginary part. In order to compute the module of this complex number, we can use this formula: $\sqrt{(P^2+Q^2)}$.

Using the binary notation isn't possible use the square root and squared operations, but it's possible to use an approximate formula:

$$\sqrt{(P^2+Q^2)} \simeq max(|P|,|Q|)+\frac{1}{2}min(|P|,|Q|)-\frac{1}{16}(max(|P|,|Q|)+min(|P|,|Q|))$$

The project consists to compute the complex number module in which the real and imaginary part are N bits wide. N in this specific case is equal to 10. One bit is used for represent the sign. The binary numbers have module which range is: $[0,2^{N-1}-1]$. In particular if N is equal to 10, the range is $[0,511]$.
The principal goal is to compute the Mean Square Error (MSE) of this approximation.

The possible applications are several in engineering fields. For instance compute the signal power, signal analysis and so on. Another application could be to compute the vector module that not necessary has a real part and an imaginary part.

Project Design

The project design is made in more logical blocks. Each blocks has a proper functionality. The blocks diagram and block description table are the following:

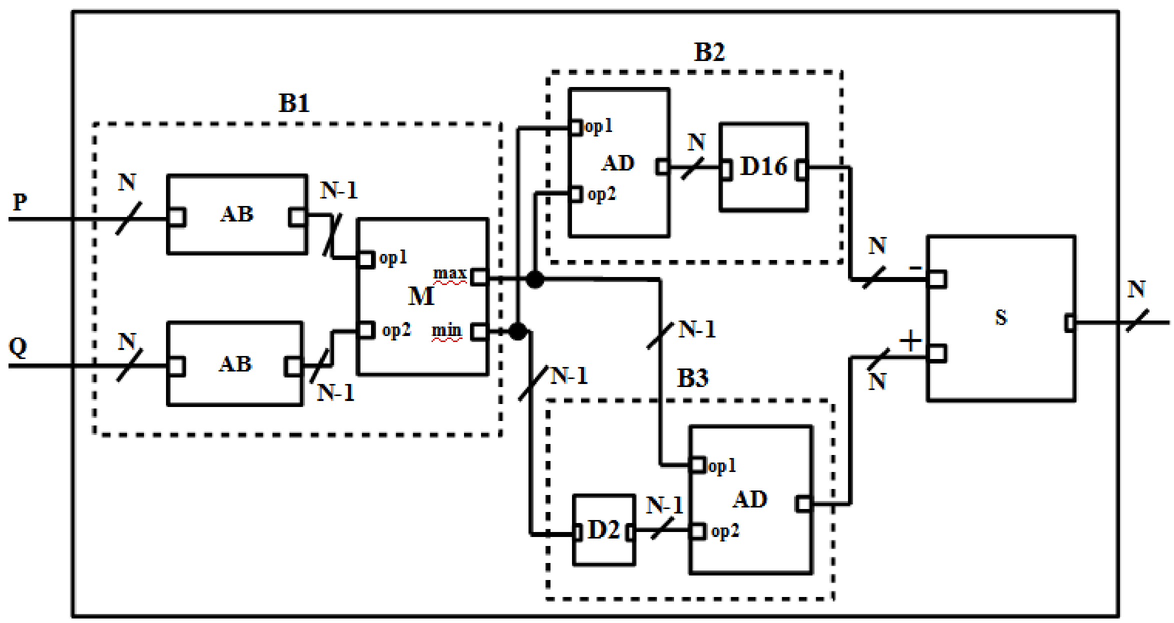


Illustrazione 1: Diagram block

Block name	**AB**	**AD**	**M**	**D2**	**D16**	**S**
Input bits	N	N-1	N-1	N-1	N-1	N-1
Output bits	N-1	N	N-1	N-1	N-1	N-1
Functionality	Get absolute value from the input.	Compute the sum from the inputs.	Get the minimum and the maximum from inputs.	Compute the division by 2 from input.	Compute division by 16 from input.	Difference between inputs.

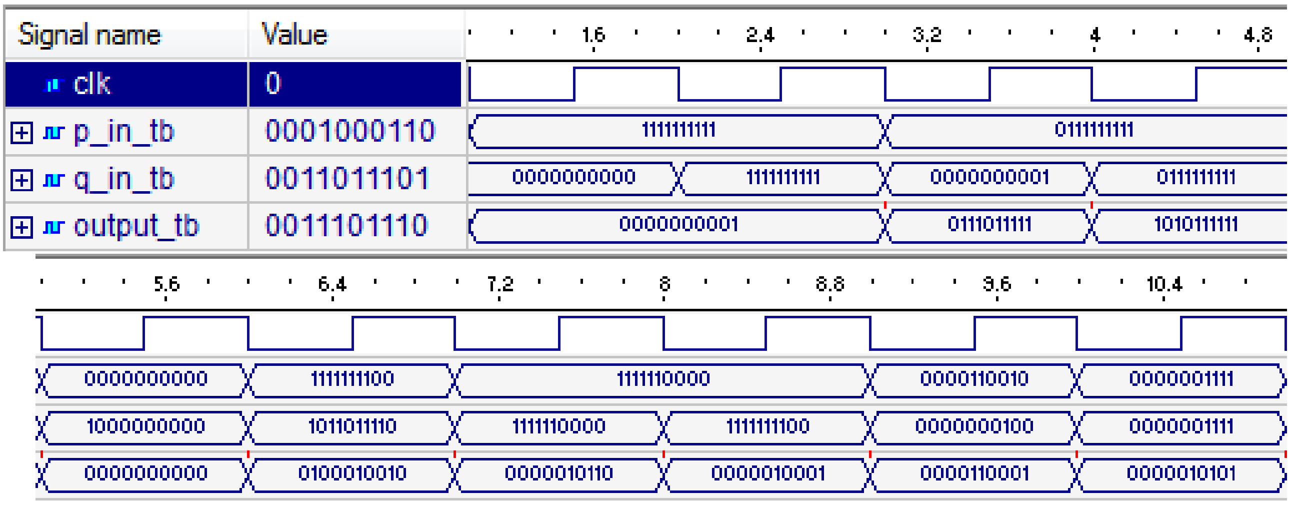
VHDL Code

For each block there is a .vhd file with a vhd testbench file in order to test the block itself.

The more detailed block description and source code are present in the PDF files stored in the same directory of this file.

Testbench

(The following waveform image is divided in two rows for visibility reasons)
In order to validate the model some tests are performed.



These inputs are also used in order to compute the expected value of complex number. As it's shown in the following table.

	INPUTS					
	P	Q	Output	Expected	Absolute difference	Squared error
Corner cases	0	0	0	0	0	0
	-1	0	1	1	0	0
	-1	-1	1	1,414214	0,4142135624	0,1715728753
	511	1	479	511,001	32,0009784726	1024,062623207
	511	511	703	722,6631	19,6631303727	386,6386960519
	0	-1	1	1	0	0
Test inputs	-4	-290	274	290,0276	16,027584895	256,883477565
	-16	-16	22	22,62742	0,627416998	0,3936520893
	-16	-4	17	16,49242	0,5075774975	0,257634916
	50	4	49	50,15974	1,1597448159	1,3450080381
	15	15	21	21,2132	0,2132034356	0,045455705
	70	221	238	231,8211	6,1789483244	38,1794023951

The above table shows the squared error between the approximation algorithm and the real result for each case.

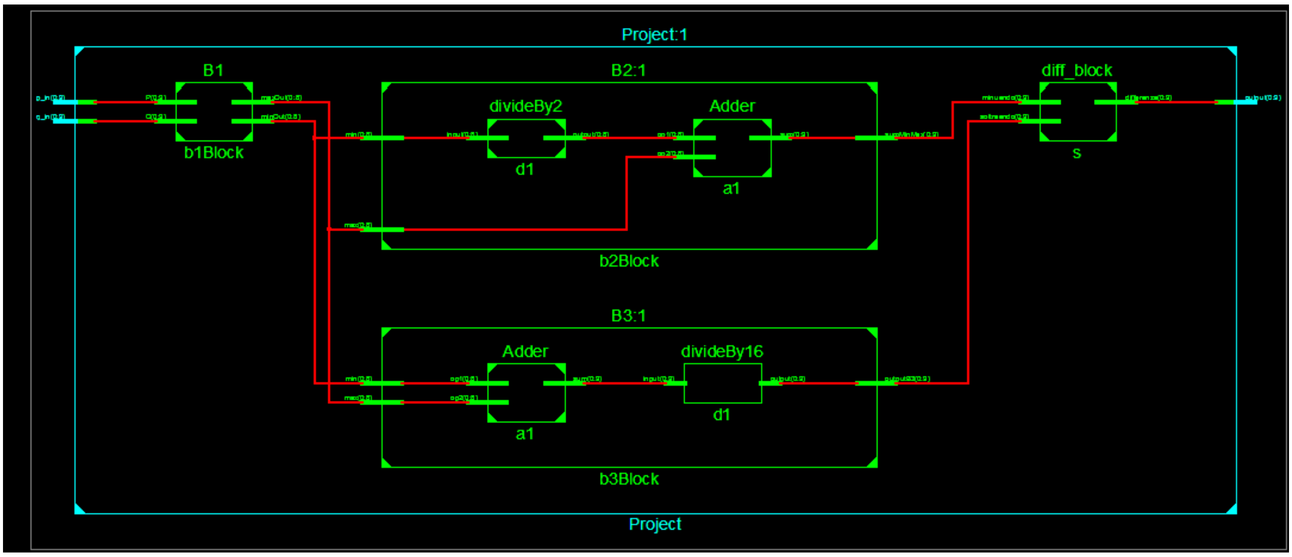
For these cases the MSE is this way: is the average of the more right columns values. It is equal to 142,33.

The more detailed table with intermediate outputs are put in the excel file in the same directory of this file.

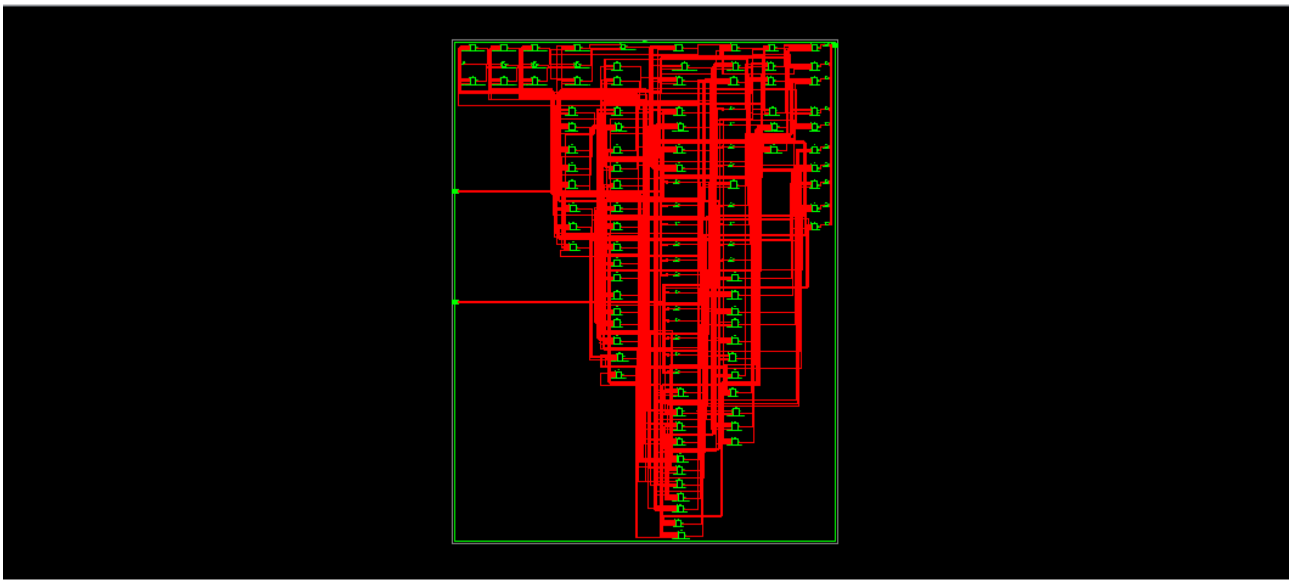
Synthesis

The synthesis is made by Xilinx tool.

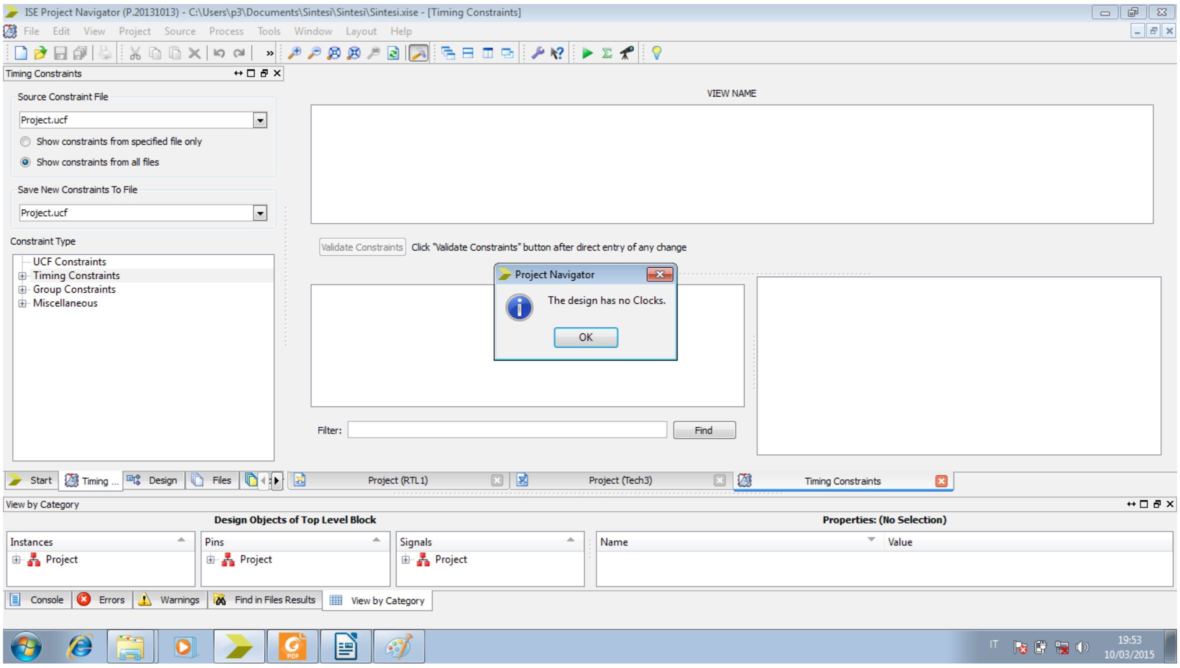
In first place I've considered the schematic representation.



The I've made, always by Xilinx tool, the schematic representation of the design in terms of logic elements.



The project is a combinator network. For this reason it isn't possible to evaluate the maximum frequency which it works.



ISE Project Navigator (P.20131013) - C:\Users\p3\Documents\Sintesi\Sintesi\Sintesi.xise - [Timing Constraints]

Timing Constraints

Source Constraint File: Project.ucf

○ Show constraints from specified file only

● Show constraints from all files

Save New Constraints To File: Project.ucf

Constraint Type

- UCF Constraints
- Timing Constraints
- Group Constraints
- Miscellaneous

VIEW NAME

Click "Validate Constraints" button after direct entry of any change

Project Navigator

The design has no Clocks.

View by Category

Design Objects of Top Level Block

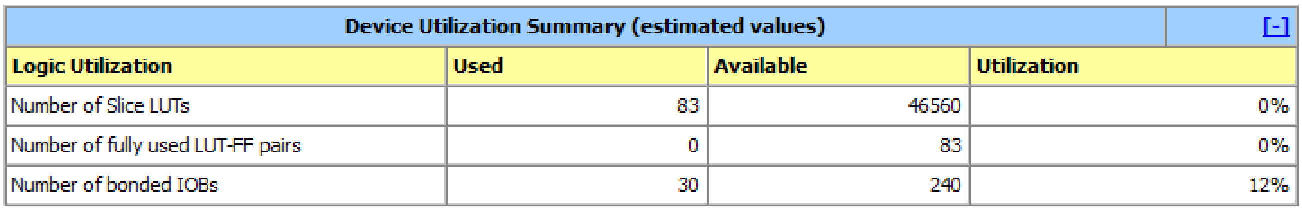
Instances	Pins	Signals
Project	Project	Project

Properties: (No Selection)

Name	Value

The maximum combinational path delay computed is 9.612ns.

The following table shows the Device Utilzation summary.



Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	83	46560	0%
Number of fully used LUT-FF pairs	0	83	0%
Number of bonded IOBs	30	240	12%

Actually the number of Slice LUTs used is 0,0018 %.

Conclusions

The algorithm is a good approximation of the complex number module. It's important to note that the absolute difference value has to be weighted on the complex number module value. For instance, if we consider this case: P=511 and Q=1. The absolute difference value between expected value and output is equal to 32. It looks like a big value, but weighted on the real value which is 511 the difference “weights” only 32/511= $32/511 \simeq 0.06$. It is only 6% of difference.

On the other hand when there are small value in inputs, for instance P=0 and Q=1 the variation in percentage respect to expected value is almost 30%. In this specific case the approximation isn't acceptable.

The other cases don't figure out big percentage variation respect to expected values.