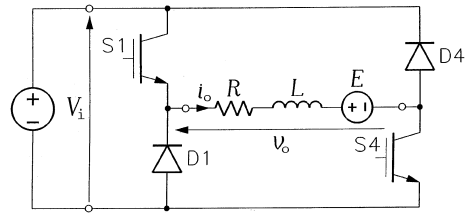

FIGURE 1.42
First-and-fourth-quadrant chopper.

A step-up (boost) chopper, shown in Fig. 1.43, produces a pulsed output voltage, whose amplitude, $V_{o,p}$, is higher than the input voltage. If a sufficiently large capacitor is connected across the output terminals, the output voltage becomes continuous, with $V_o \approx V_{o,p} > V_i$. When switch S is turned on, the input inductor, L_c, is charged with electromagnetic energy, which is then released into the load by turning the switch off. The magnitude control ratio, M, defined as $V_{o,p}/V_i$, in an ideal (lossless) step-up chopper is given by

$$M = \frac{1}{1 - D} \tag{1.18}$$

where D denotes the duty ratio of the switch. In real choppers, the value of M saturates at a certain level, usually not exceeding 10 and dependent mostly on the resistance of the input inductor. Example waveforms of the output voltage and current in a step-up chopper without the output capacitor are shown in Fig. 1.44.

1.5 DC TO AC CONVERTERS

Dc to ac converters are called *inverters* and, depending on the type of the supply source and the related topology of the power circuit, they are classified as *voltage-source inverters* (VSIs) and *current-source inverters* (CSIs). The simplest, single-phase, half-bridge, VSI is shown in Fig. 1.45. The switches may not be ON simultaneously, because they would short the supply source. There is no danger in turning both switches off, but the output voltage, v_o, would then depend on the conducting diode, that is, it could not be determined without some current sensing arrangement. Therefore, only two states of the inverter are allowed. Consequently, a single switching function, a, can be assigned to the inverter. Defining it as

$$a = \begin{cases} 0 & \text{if SA} = \text{ON} \quad \text{and} \quad \text{SA}' = \text{OFF} \\ 1 & \text{if SA} = \text{OFF} \quad \text{and} \quad \text{SA}' = \text{ON}, \end{cases} \tag{1.19}$$

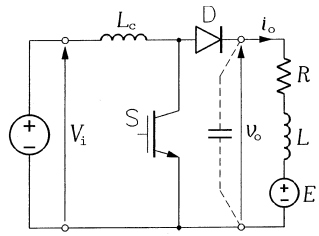

FIGURE 1.43
Step-up chopper.

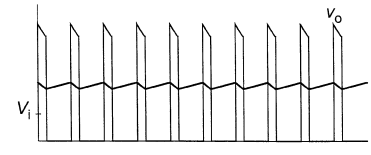

FIGURE 1.44
Output voltage and current waveforms in a step-up chopper ($D = 0.75$).

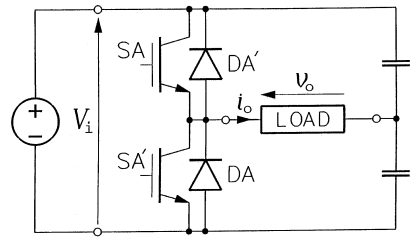

FIGURE 1.45
Single-phase, half-bridge, voltage-source inverter.

the output voltage of the inverter is given by

$$v_o = V_i\left(a - \frac{1}{2}\right) \tag{1.20}$$

where V_i denotes the dc input voltage. Only two values of v_o are possible: $V_i/2$ and $-V_i/2$. To prevent the so-called *shot-through*, that is, a short circuit when one switch is turned on and the other has not yet turned off completely, the turn-on is delayed by a few microseconds, called a *dead*, or *blanking*, *time*. The same precaution is taken in all VSIs, with respect to switches in the same leg of the power circuit.

The more common, single-phase full-bridge VSI, shown in Fig. 1.46, has two active legs, so that two switching functions, a and b, must be used to describe its operation. Notice that the topology of the inverter is identical to that of the four-quadrant chopper in Fig. 1.40. The output voltage can be expressed in terms of a and b as

$$v_o = V_i(a - b) \tag{1.21}$$

which implies that it can assume three values: V_i, 0, and $-V_i$. Thus, the maximum voltage gain of this inverter is twice as high as that of the half-bridge inverter.

Two modes of operation can be distinguished: the square-wave mode, loosely related to the phase-control mode in rectifiers, and the PWM mode. In the square-wave mode, so named because of the resultant shape of the output voltage waveform, each switch of the inverter is turned on and off only once per cycle of the output voltage. A specific sequence of inverter states is imposed, the state being designated by the decimal equivalent of ab_2. For example, if $a = 1$ and $b = 1$, the full-bridge inverter is said to be in State 3 because $11_2 = 3_{10}$. The output voltage waveform for the full-bridge inverter in the so-called optimal square-wave mode, which results in the minimum total harmonic distortion of this voltage, is shown in Fig. 1.47.

The output current, i_o, depends on the load, but generally, because of the high content of low-order harmonics (3rd, 5th, 7th, etc.) in the output voltage, it strays substantially from a sinewave.

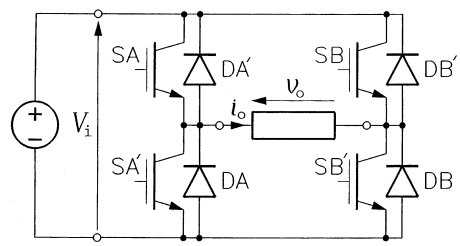

FIGURE 1.46
Single-phase, full-bridge, voltage-source inverter.

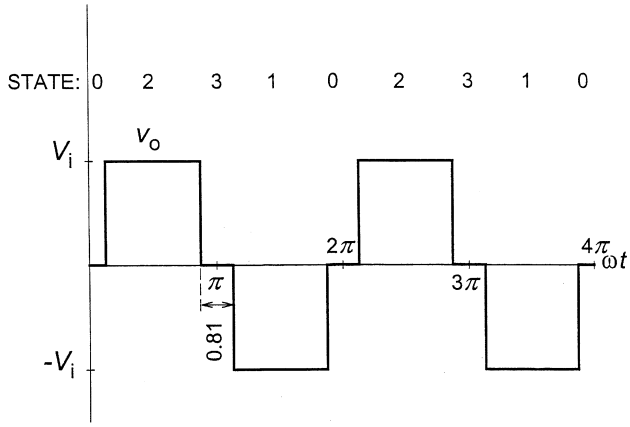

FIGURE 1.47
Output voltage waveform in a single-phase, full-bridge, voltage-source inverter in the optimal square-wave mode.

Not so in an inverter operating in the PWM mode, which results in a sinusoidal current with high-frequency ripple. Example waveforms of v_o and i_o in a PWM inverter are shown in Fig. 1.48.

Three-phase counterparts of the single-phase half-bridge and full-bridge VSIs in Figs. 1.45 and 1.46 are shown in Figs. 1.49a and 1.49b, respectively. The three-phase full-bridge inverter is one of the most common power electronic converters nowadays, predominantly used in ac adjustable speed drives and three-phase ac uninterruptable power supplies (UPSs).

The capacitive voltage-divider leg of the incomplete-bridge inverter also serves as a dc link. Two switching functions, a and b, can be assigned to the inverter, because of the two active legs of its power circuit. The line-to-line output voltages are given by

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = V_i \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -\frac{1}{2} \\ -1 & 0 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ 1 \end{bmatrix} \tag{1.22}$$

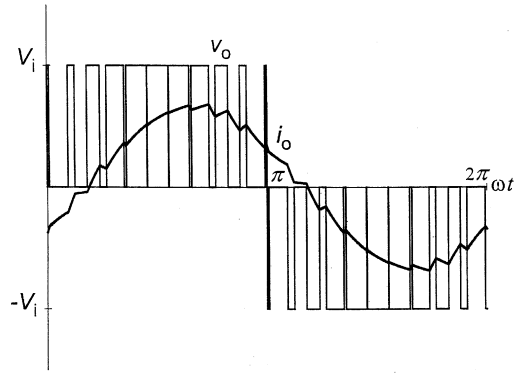

FIGURE 1.48
Output voltage and current waveforms in a single-phase, full-bridge, voltage-source inverter in the PWM mode.

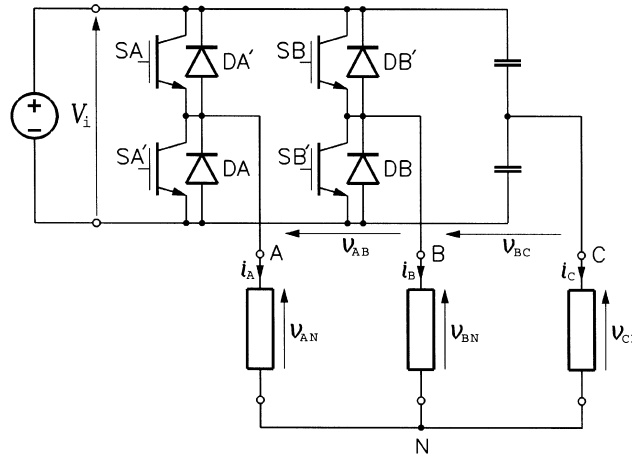

FIGURE 1.49
Three-phase voltage-source inverters: (a) incomplete-bridge, (b) full-bridge.

and the line-to-neutral voltages by

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{V_i}{3} \begin{bmatrix} 2 & -1 & -\frac{1}{2} \\ -1 & 2 & -\frac{1}{2} \\ -1 & -1 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ 1 \end{bmatrix}. \tag{1.23}$$

Voltage v_{AB} can assume three values, $-V_i$, 0, and V_i, but v_{BC} and v_{CA} can assume only two values, $-V_i/2$ and $V_i/2$. The line-to-neutral voltages v_{AN} and v_{BN} can assume four values, $-V_i/2$, $-V_i/6$, $V_i/6$, and $V_i/2$, and v_{CN} can assume three values, $-V_i/3$, 0, and $V_i/3$. This voltage asymmetry makes the square-wave operation impractical, and the incomplete-bridge inverter can only operate in the PWM mode. The maximum voltage gain, taken as the ratio of the

maximum available peak value of the fundamental line-to-line output voltage to the input voltage, is only 0.5. Therefore, in spite of the cost savings resulting from the reduced device count, the incomplete-bridge inverter is rarely used in practice.

Because of the three active legs, three switching functions, a, b, and c, are associated with the full-bridge three-phase inverter. The line-to-line and line-to-neutral output voltages are given by

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = V_i \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{1.24}$$

and

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{V_i}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}. \tag{1.25}$$

Each line-to-line voltage can assume three values, $-V_i$, 0, and V_i, and each line-to-neutral voltage five values, $-2V_i/3$, $-V_i/3$, 0, $V_i/3$, and $2V_i/3$. In the PWM mode, the maximum voltage gain is 1, that is, the maximum attainable peak value of the fundamental line-to-line voltage equals the dc supply voltage.

As in single-phase inverters, the state of the full-bridge inverter can be defined as the decimal equivalent of abc_2. The 5-4-6-2-3-1 . . . state sequence, each state lasting one-sixth of the desired period of the output voltage, results in the square-wave mode of operation, illustrated in Fig. 1.50. In this mode, the fundamental line-to-line output voltage has the highest possible peak value, equal to $1.1V_i$, yielding a maximum voltage gain 10% higher than that in the PWM mode. At the same time, in the inverter, there is no possibility of magnitude control of the output voltage, and the voltage waveforms are rich in low-order harmonics, spoiling the quality of output currents. Therefore, in practical energy conversion systems involving inverters, the square-wave mode is used sparingly, only when a high value of the output voltage is necessary.

Example waveforms of switching functions and output voltages of the three-phase full-bridge inverter in the PWM mode are shown in Fig. 1.51. The cycle of output voltage is divided here into 12 equal *switching intervals*, pulses of switching functions located at centers of the intervals. Thus, the switching frequency, f_{sw}, is 12 times higher than the output frequency, f. In practical inverters, the switching frequency is usually maintained constant and independent of the output frequency, at a level representing the best trade-off between the switching losses and quality of the output currents.

The so-called *voltage space vectors*, an idea originally conceived for analysis of three-phase electrical machines, are a useful tool for analysis and control of three-phase power converters as well. Denoting individual phase voltages of an inverter by v_a, v_b, and v_c (they can be line-to-line, line-to-ground, or line-to-neutral voltages), the voltage space vector, $\mathbf{v}$, is defined as

$$\mathbf{v} = v_d + jv_q \tag{1.26}$$

where

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \tag{1.27}$$

Reduction of three phase voltages, v_a, v_b, and v_c, to two components, v_d and v_q, of the voltage vector is only valid when $v_a + v_b + v_c = 0$. Then, only two of these voltages are independent

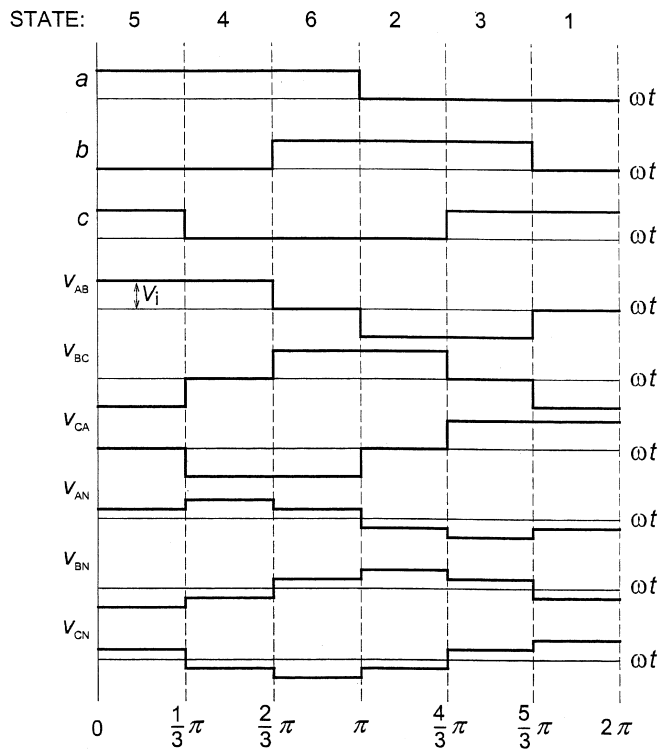

FIGURE 1.50
Waveforms of switching functions and output voltages in a three-phase, full-bridge inverter in the square-wave operation mode.

variables, so that the amount of information carried by v_a, v_b, and v_c is the same as that carried by v_d and v_q.

If

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = V_p \begin{bmatrix} \cos(\omega t + \varphi) \\ \cos(\omega t + \varphi - \frac{2}{3}\pi) \\ \cos(\omega t + \varphi - \frac{4}{3}\pi) \end{bmatrix}, \tag{1.28}$$

then

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{3}{2} V_p \begin{bmatrix} \cos(\omega t + \varphi) \\ \sin(\omega t + \varphi) \end{bmatrix}, \tag{1.29}$$

that is,

$$\mathbf{v} = \frac{3}{2} V_p e^{j(\omega t + \varphi)}. \tag{1.30}$$

Thus, as the time, t, progresses, the voltage space vector, $\mathbf{v}$, revolves with the angular velocity ω in a plane defined by a set of orthogonal coordinates d and q.

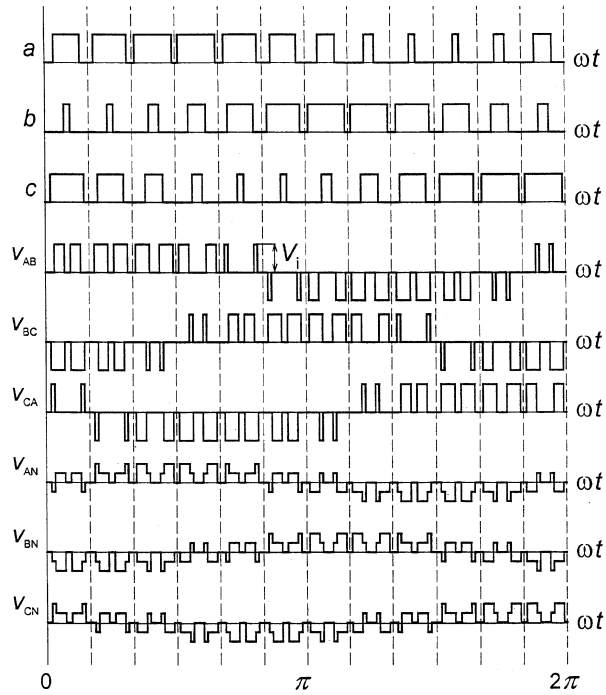

FIGURE 1.51
Waveforms of switching functions and output voltages in a three-phase, full-bridge inverter in the PWM mode.

In application to VSIs, the revolving voltage vector describes the fundamental output voltages. Each state of the inverter produces a specific stationary voltage space vector, and the revolving vector, **v**, which is to follow a reference vector, **v***, must be synthesized from the stationary vectors in a time-averaging process. The maximum possible value of **v** determines the maximum voltage gain of the inverter.

The four stationary voltage vectors, $\mathbf{V}_0$ through $\mathbf{V}_3$, of the three-phase incomplete-bridge inverter, corresponding to its four allowable states, are shown in Fig. 1.52 in the per-unit format. The input voltage, V_i, is taken as the base voltage. In the process of pulse width modulation, the vector, **v**, of fundamental output voltage is synthesized as

$$\mathbf{v} = \sum_{S=0}^{3} D_S \mathbf{V}_S \tag{1.31}$$

where D_S denotes the duty ratio of State S ($S = 0 \ldots 3$). Each switching interval, a small fraction of the period of output voltage, is divided into several nonequal subintervals, constituting durations of individual states of the inverter. Not all four states must be used; three are enough. The vectors employed depend on the angular position of the synthesized vector **v**. Since the sum of all the duty ratios involved equals 1, the maximum available voltage vector to be generated is limited. It can be shown that the circle shown in Fig. 1.52 represents the locus of that vector. In other words, the maximum magnitude of **v** is $\sqrt{3}/4\ V_i$, which corresponds to the peak value of the line-to-line fundamental output voltage being equal to one-half of the dc supply voltage of the inverter.

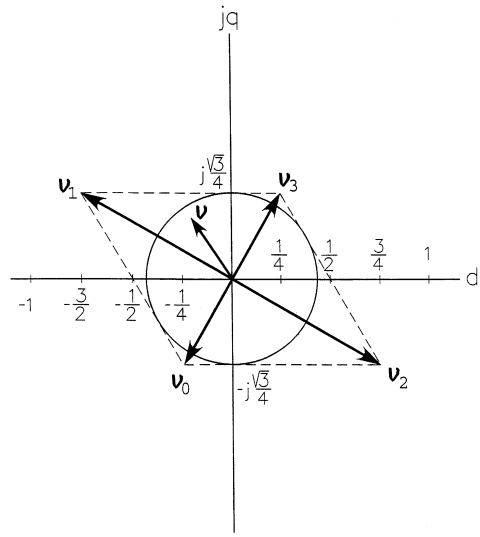

FIGURE 1.52
Space vectors of line-to-neutral output voltage in a three-phase incomplete-bridge voltage-source inverter.

Space vectors of line-to-line output voltage of the full-bridge inverter are shown in Fig. 1.53. There are six nonzero vectors, $\mathbf{V}_1$ through $\mathbf{V}_6$, whose magnitude equals the dc input voltage, V_i, and two zero vectors, $\mathbf{V}_0$ and $\mathbf{V}_7$. In general,

$$\mathbf{v} = \sum_{S=0}^{7} D_S \mathbf{V}_S, \tag{1.32}$$

but in practice, only a zero vector and two nonzero vectors framing the output voltage vector are used. For instance, the vector $\mathbf{v}$ in Fig. 1.53 is synthesized from vectors $\mathbf{V}_2$ and $\mathbf{V}_3$ and a zero vector, $\mathbf{V}_0$ or $\mathbf{V}_7$. The radius of circular locus of the maximum output voltage vector indicates a voltage gain twice as high as that of the incomplete-bridge inverter. Specifically, the maximum

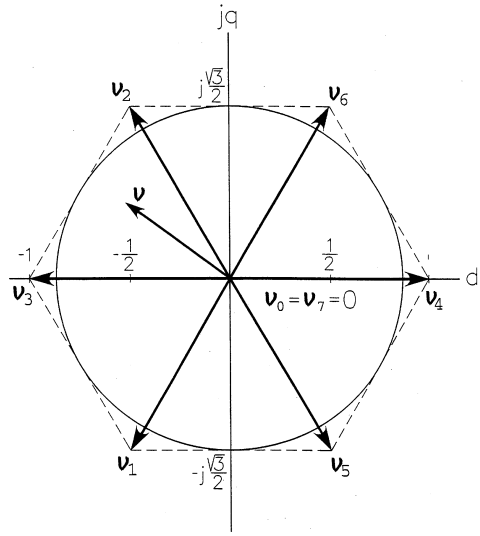

FIGURE 1.53
Space vectors of line-to-neutral output voltage in a three-phase full-bridge voltage-source inverter.

available peak value of the fundamental line-to-line output voltage equals V_i. Notice that going clockwise around the vector diagram yields the state sequence 4-6-2-3-1-5 . . ., characteristic for square-wave operation with positive phase sequence, A-B-C. The counterclockwise state sequence 4-5-1-3-2-6 . . ., would result in a negative phase sequence, A-C-B.

The voltage-source inverters described can be termed "two-level," because each output terminal, temporarily connected to either of the two dc buses, can only assume two voltage levels. Recently, *multilevel inverters* have been receiving increased attention. Using the same power switches, they have higher voltage ratings than their two-level equivalents. Also, their output voltage waveforms are distinctly superior to these in two-level inverters, especially in the square-wave mode.

The most common, *three-level neutral-clamped* inverter is shown in Fig. 1.54. Each leg of the inverter is comprised of four semiconductor power switches, S_1 through S_4, with freewheeling diodes, D_1 through D_4, and two clamping diodes, D_5 and D_6, that prevent the dc-link capacitors from shorting. The total of 12 semiconductor power switches implies a high number of possible inverter states. In practice, 27 states are employed only, as each leg of the inverter is allowed to assume only the three following states: (1) S1 and S2 are ON, S3 and S4 are OFF, (2) S2 and S3 are ON, S1 and S4 are OFF, and (3) S1 and S2 are OFF, S3 and S4 are ON. It can be seen that the dc input voltage, V_i, is always applied to a pair of series-connected switches, which explains the

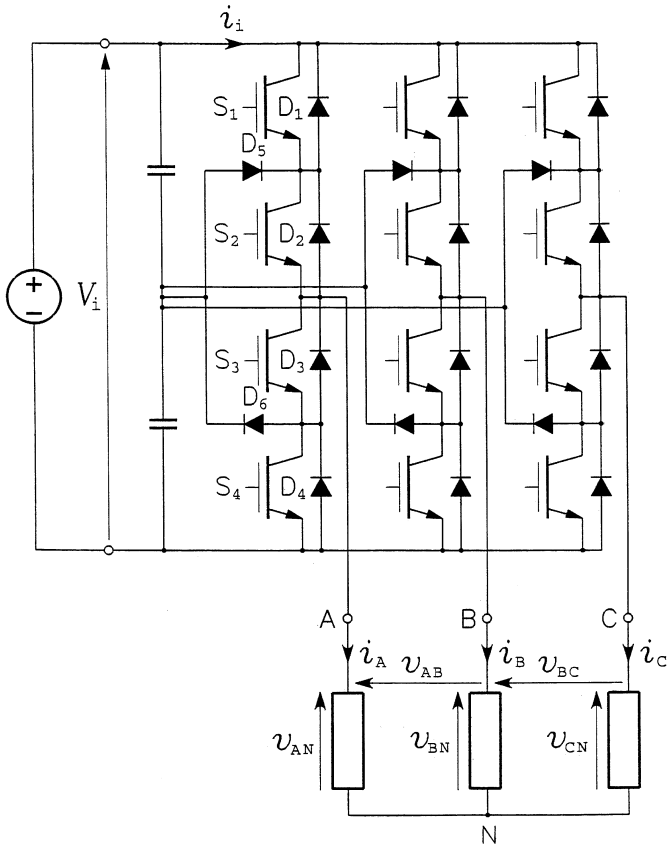

FIGURE 1.54
Three-level neutral-clamped inverter.

already-mentioned advantage of multilevel inverters with respect to the voltage rating. It can be up to twice as high as the rated voltage of the switches.

Stationary space vectors of output voltage of the three-level inverter are shown in Fig. 1.55. The maximum voltage gain of the inverter is the same as that of the two-level full-bridge inverter, but the availability of 27 stationary voltage vectors allows for higher quality of the output voltage and current. For instance, the square-wave mode of operation results in five-level line-to-line output voltages and seven-level line-to-neutral voltages. Waveforms of output voltages in the three-level inverter operating in the square-wave mode are shown in Fig. 1.56. PWM techniques produce output currents with very low ripple even when medium switching frequencies are employed.

All the inverters described so far are *hard-switching* converters, switches of which turn on and off under nonzero voltage and nonzero current conditions. This results in switching losses, which at high switching frequencies can be excessive. High rates of change of voltages (dv/dt) and currents (di/dt) cause a host of undesirable side effects, such as accelerated deterioration of stator insulation and rotor bearings, conducted and radiated electromagnetic interference (EMI), and overvoltages in cables connecting the inverter with the motor. Therefore, for more than a decade, significant research effort has been directed toward development of practical *soft-switching* power inverters.

In soft-switching inverters, switches are turned on and off under zero-voltage or zero-current conditions, taking advantage of the phenomenon of electric resonance. As is well known, transient currents and voltages having *ac-type* waveforms can easily be generated in low-resistance inductive-capacitive (LC) *dc-supplied* circuits. Thus, a resonant LC circuit (or circuits) constitutes an indispensable part of the inverter. Two classes of soft-switching inverters have emerged. In the first class, no switches are added to initiate the resonance. A representative of this class, the classic *resonant dc link* (RDCL) inverter with voltage pulse clipping, is shown in Fig. 1.57.

The resonant circuit consists of an inductor, L_r, and capacitor, C_r, placed between the dc link (not shown) and the inverter. Low values of the inductance and capacitance make the resonance

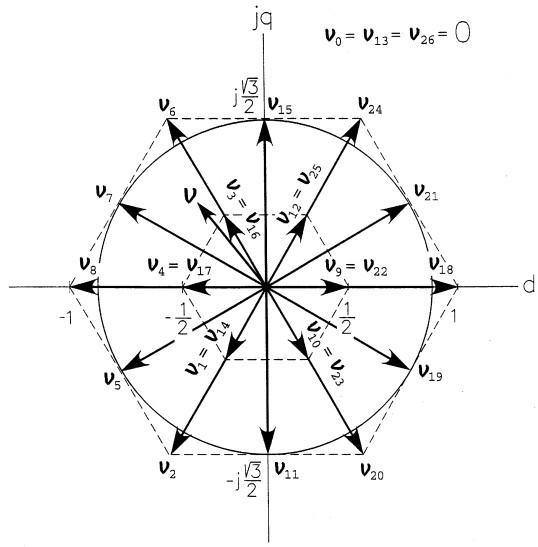

FIGURE 1.55
Space vectors of line-to-neutral output voltage in a three-level neutral-clamped inverter.

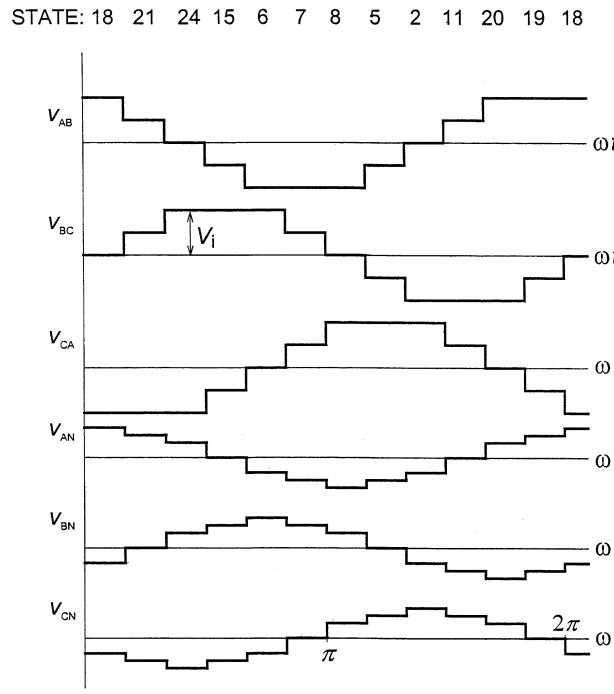

FIGURE 1.56
Output voltage waveforms in a three-level neutral-clamped inverter in the square-wave mode.

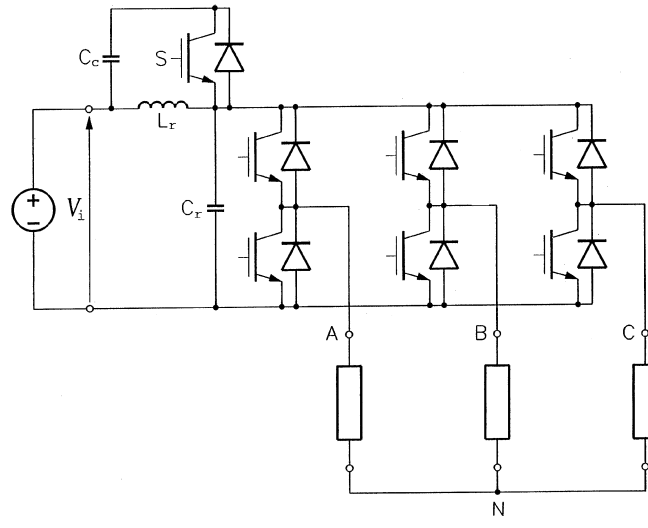

FIGURE 1.57
Resonant dc link inverter.

frequency several orders of magnitude higher than the output frequency of the inverter. The resonance is initiated by turning on, for a short period of time, both switches in a leg of the inverter bridge. This loads L_r with electromagnetic energy, which is then released into C_r when one of the switches in question is turned off. Because of the low resistance of the resonant circuit, the voltage across the capacitor acquires a sinusoidal waveform. Should the clamping circuit, based on switch S and capacitor C_c, be inactive, the peak value of the output voltage would approach $2V_i$. When the voltage drops to zero, the freewheeling diodes of the inverter become forward biased and they short the dc buses of the power circuit. This creates zero-voltage conditions for inverter switches, allowing lossless switching of these switches.

Output voltage waveforms in the RDCL inverter consist of packets of narrowly spaced resonant pulses. The clamping circuit clips these pulses in order to increase voltage density. A packet of clipped voltage pulses is shown in Fig. 1.58. It represents the equivalent of a single rectangular pulse of output voltage in a hard-switching inverter. It can be seen that the voltage pulses have low dv/dt, which alleviates certain undesirable side effects of inverter switching.

In the other class of soft-switching inverters, auxiliary switches trigger the resonance, so that the main switches are switched under zero-voltage conditions. One phase (phase A) of such a converter, the *auxiliary resonant commutated pole* (ARCP) inverter, is shown in Fig. 1.59. To minimize high dynamic stresses on main switches SA and SA′, a resonant snubber, based on the inductor L_A and capacitors C_{A1} and C_{A2}, is employed. The resonance is initiated by turning on the bidirectional switch, composed of auxiliary switches S_{A1} and S_{A2} and their antiparallel diodes. The auxiliary switches are turned on and off under zero-current conditions.

ARCP inverters, typically designed for high-power applications, provide highly efficient power conversion. In contrast to the RDCL inverter, whose output voltage waveforms consist of packets of resonant pulses, the ARCP inverter is capable of true pulse width modulation, but with the voltage pulses characterized by low dv/dt. Typically, IGBTs or GTOs are used as main switches, while MCTs or IGBTs serve as auxiliary switches.

The voltage source supplying a VSI provides a fixed dc input voltage. A battery pack or, more often, a rectifier (usually uncontrolled) with a dc link, such as the dc source for choppers shown in Fig. 1.37, is used. Consequently, polarity of the input current depends on the direction of power transfer between the source and the load of the inverter, which explains the necessity of the freewheeling diodes. Voltage sources are more "natural" than current sources. However, a fair representation of a current source can be obtained combining a current-controlled rectifier

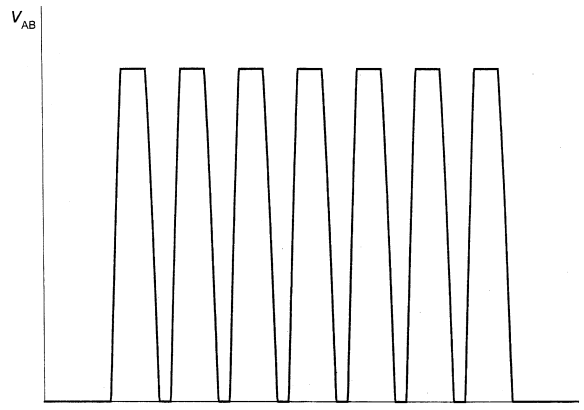

FIGURE 1.58
Packet of output voltage pulses in a resonant dc link inverter.

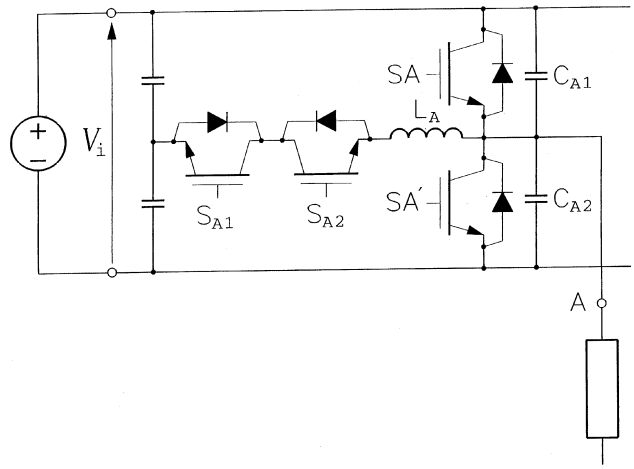

FIGURE 1.59
One phase of the auxiliary resonant commutated pole inverter.

and a large series inductor, as illustrated in Fig. 1.60. Such a source can be used for supplying dc power to a current-source inverter. In that case, it is the input current, I_i, that is maintained constant, and reversal of the power transfer is accompanied by a change in polarity of the input voltage.

The three-phase current-source inverter, shown in Fig. 1.61, differs from its full-bridge voltage-source counterpart by the absence of freewheeling diodes, which, because of the unidirectional input current, would be superfluous. Analogously, the single-phase CSI can be obtained from the single-phase full-bridge VSI in Fig. 1.46 by removing the freewheeling diodes.

In contrast to VSIs, both switches in the same leg of a CSI can be ON simultaneously. Because of the current-source characteristics of the supply system, no overcurrent will result. It is interruption of the current that is dangerous, because of the large dc-link inductance. Therefore, when changing the state of the inverter, both switches in one phase are kept closed for a short period of time, an analogy to the dead time in VSIs.

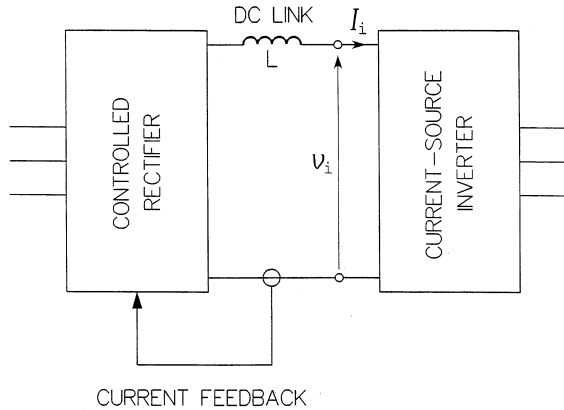

FIGURE 1.60
Supply arrangement for the current-source inverter.

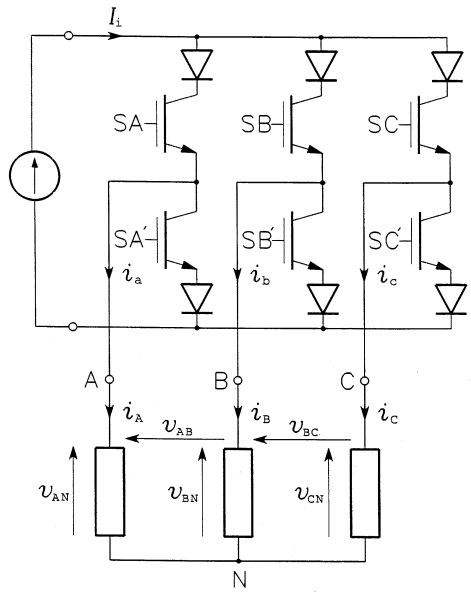

FIGURE 1.61
Three-phase current-source inverter.

Because both switches in the same phase can be ON or OFF simultaneously and one switch can be ON while the other is OFF, switching functions for individual phases would have to be of the quaternary type (having values of 0, 1, 2, or 3). This would be inconvenient; therefore, binary switching functions, a, a', b, b', c, and c', are assigned to individual switches, SA through SC′, instead. This makes for 64 possible states of the inverter, of which, however, only 9 are employed, to avoid the uncertainty resulting from supplying a multipath network from a current source. Only one path of the output current is permitted, for example, from terminal A to terminal C, that is, with $i_A = -i_C$.

The output line currents in the three-phase CSI can be expressed as

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = I_i \left(\begin{bmatrix} a \\ b \\ c \end{bmatrix} - \begin{bmatrix} a' \\ b' \\ c' \end{bmatrix} \right). \tag{1.33}$$

Defining the state of a CSI as $aa'bb'cc'_2$, only States 3, 6, 9, 12, 18, 24, 33, 36, and 48 are used, States 3, 12, and 48 producing zero output currents. Space vectors of the CSI are shown in Fig. 1.62. To facilitate interpretation of individual vectors, terminals of the inverter passing the output current are also marked. For example, current vector $\mathbf{i}_{33}$, produced in State 33, represents the situation when the load current flows between terminals A and C, that is, $i_A = I_i$ and $i_C = -I_i$.

Analogously to the VSI, when the state sequence corresponding to sequential current vectors $\mathbf{i}_{36}, \mathbf{i}_{33}, \mathbf{i}_9, \mathbf{i}_{24}, \mathbf{i}_{18}, \mathbf{i}_6, \ldots$, is imposed, with each state lasting one-sixth of the desired period of the output voltage, the CSI operates in the square-wave mode illustrated in Fig. 1.63. In practice, the rate of change of the current at the leading and trailing edge of each pulse is limited. Still, the load inductance generates spikes of the output voltage at these edges which, in addition to the nonsinusoidal shape of current waveforms, constitutes a disadvantage of CSIs. Sinusoidal currents (with a ripple) are produced in the PWM CSI, which is obtained by adding capacitors

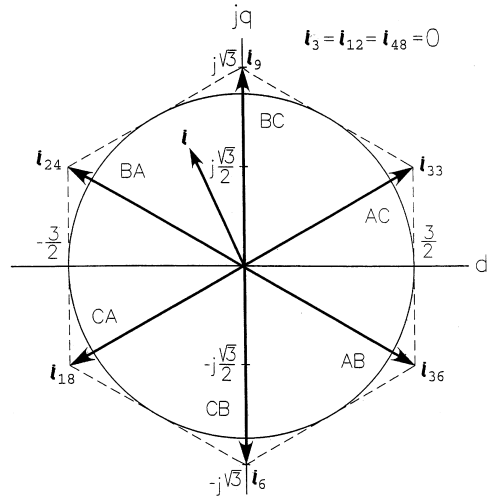

FIGURE 1.62
Space vectors of line current in a three-phase current-source inverter.

between the output terminals. These capacitors shunt a part of the harmonic content of square-wave currents, so that the load currents resemble those of the VSI.

1.6 CONCLUSION

The described variety of power electronic converters allows efficient conversion and control of electrical power. Pulse width modulated converters offer better operating characteristics than the phase-controlled ones, but the very process of high-frequency switching creates undesirable side effects of its own. It seems that phase-controlled rectifiers and ac voltage controllers will

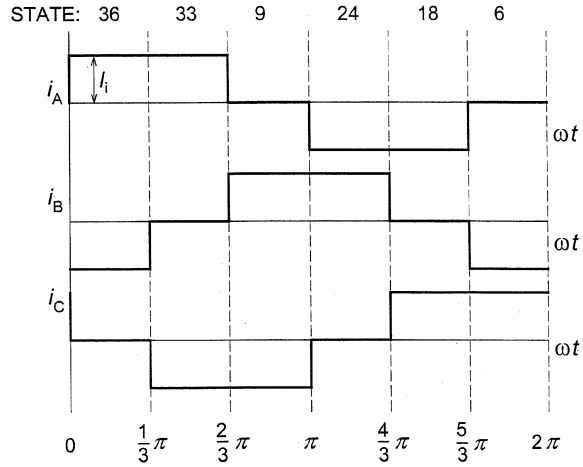

FIGURE 1.63
Output current waveforms in a current-source inverter in the square-wave mode.

maintain their presence in power electronics for years to come. The same observation applies to hard-switching converters, although the soft-switching ones will certainly increase their market share.

Switching functions, which stress the discrete character of power electronic converters, and space vectors of voltage and current, are convenient tools for analysis and control of these converters. It is also worth noting that the progress in speed and efficacy of information and power processing in modern PWM converters makes them nearly ideal power amplifiers.

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CHAPTER 2

Resonant dc Link Converters

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Applying soft switching reduces device-switching losses compared to hard-switched voltage source inverter (VSI), making it an interesting alternative. In contrast to the PWM-VSI, where the snubberless main circuit design is dominant, there is no resonant circuit configuration that has a dominant position. There are a variety of different circuits that are able to realize device soft switching; every circuit has its own merits and demerits. This chapter will present a few different converter configurations which are considered to be basic. The basic configuration has inspired a wide variety of converters; a few of those are also presented. Finally, discrete modulators are presented.

2.1 OVERVIEW OF RESONANT DC LINK CONVERTERS

2.1.1 Parallel Resonant dc Link

Reduction of the switching losses in the PWM-VSI may be done by a snubber circuit, which is robust and simple to realize. However, snubber circuits are designed to dissipate switching power in a resistor and the total losses are increased. The resonant circuit is ideally a nondissipative circuit and therefore an interesting alternative to snubber circuits.

The parallel resonant dc link (RDCL) converters have an oscillating link voltage that oscillates between zero voltage and a peak voltage. Figure 2.1 shows a parallel resonant converter. The switching of the transistors in the converter must be synchronized with the zero voltage periods of v_{do} [1] to obtain zero voltage switching (ZVS). This strategy eliminates the possibility of high-resolution PWM, and instead discrete pulse modulation (DPM) must be used. In [2] DPM is described, and it is concluded that the DPM has a performance comparable to that of PWM-VSI if the resonant link frequency is more than 6 times higher than the PWM switching frequency. When a comparison of the output waveforms is done in [3, 2], it is shown that DPM converter's spectrum performance relative to PWM is lower at modulation indexes below 0.3–

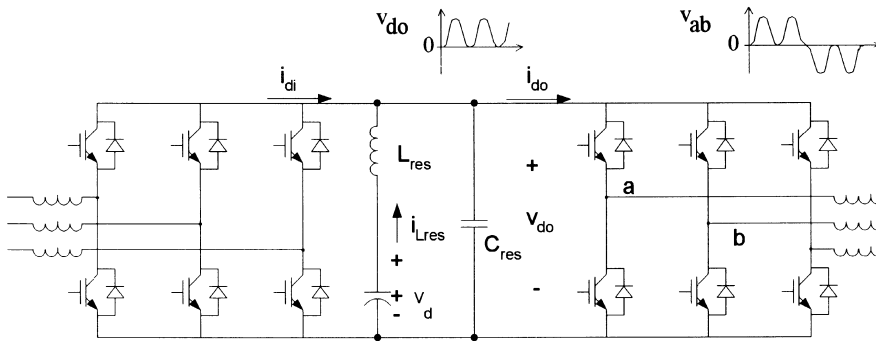


FIGURE 2.1
Parallel resonant dc link converter.

0.5. Compared to hard switching converters with a stiff dc voltage link, the voltage peak-to-peak amplitude seen by the transistors can be more than twice the dc voltage, V_d. The peak voltage of v_{do} is often limited by an auxiliary clamp circuit [4]. A high peak voltage across the terminals has several disadvantages: high voltage rating of converter devices, and stress on load-machine insulation, which may cause insulation breakdown.

2.1.2 Series Resonant dc Link

The series resonant dc link converter (Fig. 2.2) uses the principle of zero current switching (ZCS), where lossless switching is obtained. The converter is closely related to the thyristor converter and the link voltage is bipolar, which demands switches with symmetrical voltage blocking capability. The dc link current is oscillating between zero and, at a minimum, twice the dc link current, which is supplied by a dc inductor, L_d. There must always be a current path for the inductive dc link current and a capacitor filter is therefore necessary.

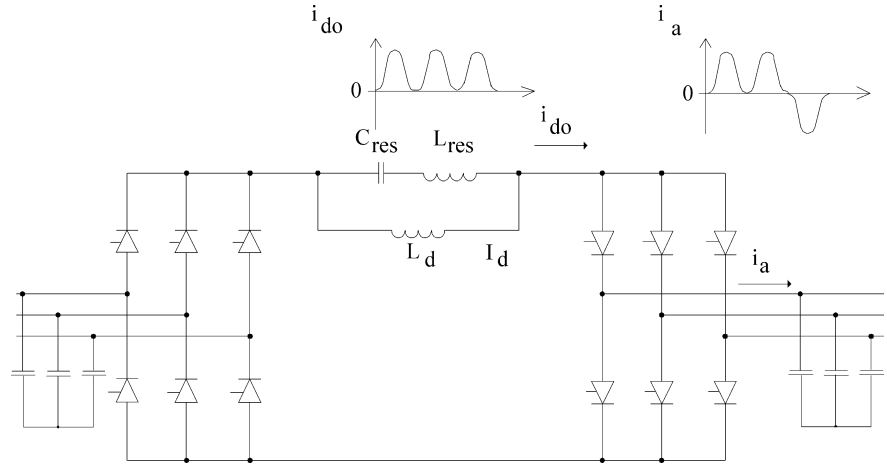


FIGURE 2.2
Series resonant dc link converter.

The converter is born with the possibility of rectification with unity power factor and bidirectional power flow. When using a parallel resonant topology, the ac voltage rectification is often done by diodes that eliminate the controlled switches, the bidirectional power flow, and the unity power factor correction options. With series resonant converters only 12 thyristors are needed for a full-bridge three-phase ac to ac conversion, whereas in parallel resonant converters 12 transistors and 12 diodes are used.

The firing of the thyristors must be synchronized with the zero current periods in the link, and again DPM is used. Spectral performance is dependent on the switching frequency. Normally the switching frequency is limited to 30 kHz because of the relative slow switching times of thyristors [5].

The link current stress is minimum twice the dc inductor current, and the conduction losses are thus relatively high compared to parallel resonant converters.

One general drawback of the serial converter is the necessary filter capacitance on the ac sides [6]. The interaction of the filter capacitance and the motor load inductance causes high-frequency oscillations on the load current. Further on the ac capacitor is bulky. A passive first-order filter can be used to reduce the high-frequency oscillation to an acceptable level at the expense of extra components and ohmic power dissipation [6]. This solution makes the size of the converter dependent on the load.

2.1.3 Pole Commutated dc Link

The pole commutated converter (Fig. 2.3) has a stiff dc link voltage, but the converter switches are switched under zero voltage conditions, and therefore low switching losses are obtained. To obtain ZVS an auxiliary resonant circuit is used. Each converter branch uses one circuit and the auxiliary circuit has four terminals. Three are connected to the dc link terminals and the fourth terminal is connected to the branch terminal [7, 8].

Unlike the parallel and series resonant dc link converters, the pole commutated converter is able to perform PWM. Another advantage is that the main load current is not flowing through the resonant elements, and in this way the current stress on the resonant inductor is relatively small.

Compared to hard switching converters the voltage stress on the converter switches is almost the same and with less output voltage dv/dt. There is a trade-off between a low dv/dt and a small

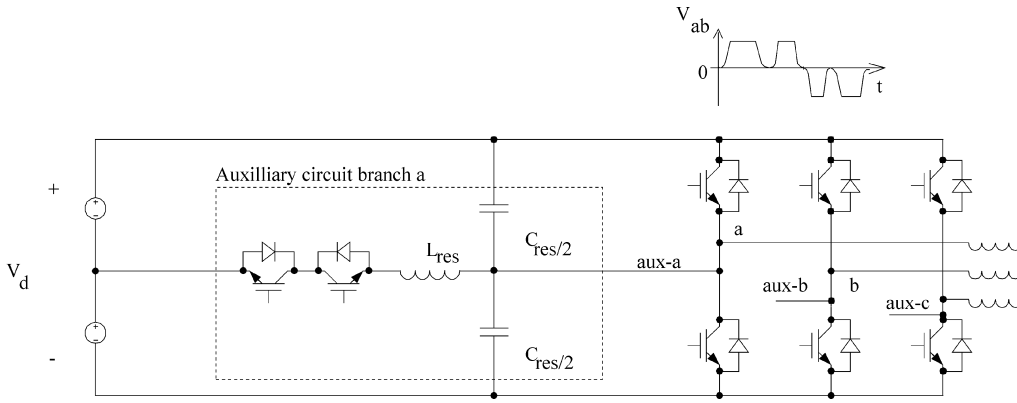


FIGURE 2.3
Auxiliary pole commutated converter.

minimum pulse-width duration. An increased resonant frequency, given by L_{res} and C_{res}, increases the dv/dt but lowers the limits on the pulse width. This will give a better spectral performance. The pole commutated converters obtain a spectral performance close to that of the PWM-VSI for a given switching frequency [7].

2.2 PARALLEL RESONANT CONVERTERS

To limit the peak voltage of the parallel resonant dc link converters a clamping method must be used. Often an additional clamp circuit is used, but it is also possible to limit the peak voltage simply by controlling the inverter switches. Three different methods are described in the following.

2.2.1 Passive Clamp

The passively clamped parallel resonant dc link converter is described in [9]. The link clamp circuit is a transformer with a diode as shown in Fig. 2.4. Ideally the transformer clamp the link voltage v_{do} to a clamp level of 2 times the dc link voltage V_d. In practice stray inductance causes a clamping level higher than twice the V_d. A link voltage clamp factor of 2.02 is obtained in [9]. The link voltage amplitude is 1252 V with a link voltage $V_d = 620$ V.

2.2.2 Active Clamp

In the active clamped resonant dc link (ACRDCL) converter the link voltage amplitude, v_{do}, is limited below 2 times V_d by a clamp circuit. The ACRDCL [10] is shown in Fig. 2.5.

The link voltage amplitude v_{do} is clamped by the voltages, $V_k + V_d$ when diode D_1 conducts. During the period diode D_1 conducts, the inductor L_{res} discharges. In order to enable the next resonant cycle to reach zero voltage, the inductor L_{res} must be recharged. Switch S_1 is turned on during the recharge of the inductor.

A control strategy for the active clamp is found by energy considerations. Energy flowing into the clamp source V_k must be equal to the energy flowing out. The active clamp circuit uses an ideal voltage source, in a realization of the clamp circuit voltage sources are often avoided, due to

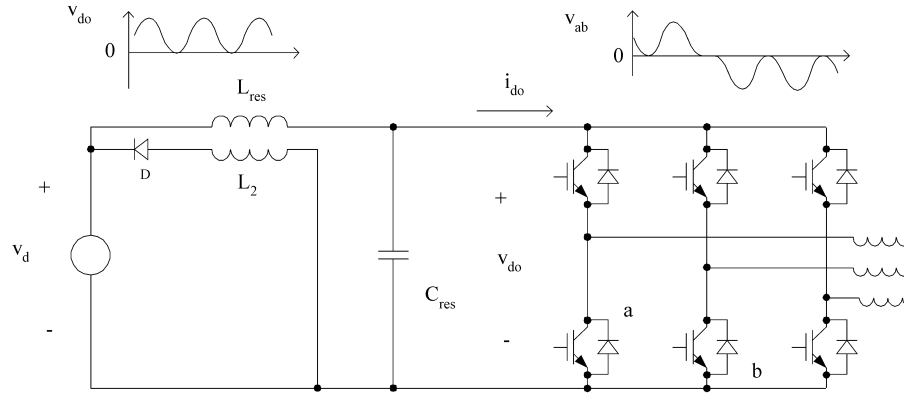


FIGURE 2.4
Passive clamped resonant converter.

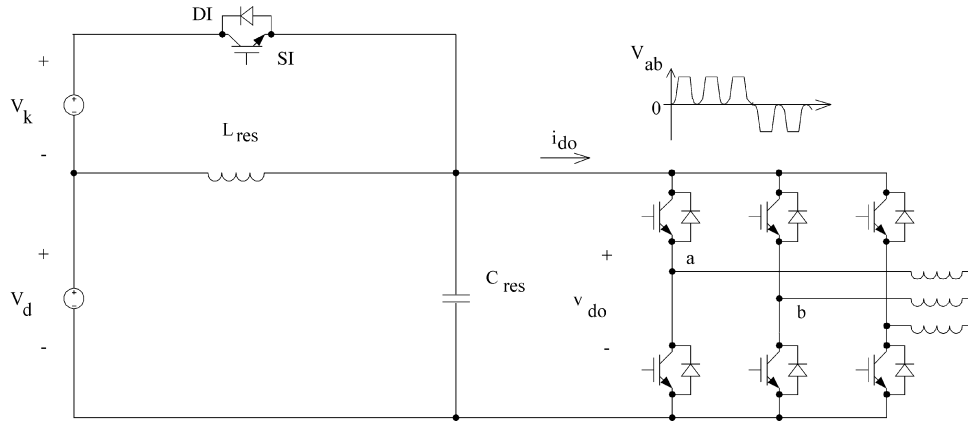


FIGURE 2.5
Active clamped resonant converter.

the circuit complexity and costs. In [10, 11] several suggestions from the literature describe how to realize the clamp circuit.

2.2.3 Voltage Peak Control

A voltage peak higher than $2V_d$ is generated if the resonant inductor L_{res}, shown in Fig. 2.1, is suddenly discharged and the inductor discharge through the resonant capacitor. This situation is shown in Fig. 2.6a. An IGBT in the inverter is turned off and the link current i_{do} abruptly changes amplitude. The following charge of the resonant capacitor is responsible for the high voltage peak. The high voltage peak can be prevented. By turning the IGBT off a short time before the zero dc link voltage condition the charge of the capacitor can be controlled. Turning the IGBT off at a link voltage level of ΔV_{do} causes the next resonant voltage peak to be twice the dc link voltage. The principle is illustrated in Fig. 2.6b.

The voltage peak control (VPC) strategy used to control the resonant dc link voltage is derived in [12]. The strategy can be formulated using

$$\Delta V_{do} = V_d\left(1 - \cos\left(a \sin\left(\frac{\Delta i_{do} Z_{res}}{2V_d}\right)\right)\right)$$

where V_d is the dc link voltage, Z_{res} is the resonant impedance $= \sqrt{L_{res}/C_{res}}$, and Δi_{do} is the link current change.

The ΔV_{do} is the resonant voltage level where the dc link current must change, to make the next resonant voltage peak twice the dc link voltage. Experimental results are shown in Fig. 2.7.

2.3 PARALLEL RESONANT PWM CONVERTERS

This section deals with the type of parallel resonant converters which use PWM and have zero voltage switching of the main switches. Three converters are presented: the notch commutated three-phase PWM converter [13, 14], the zero switching loss PWM converter with resonant circuit [15], and the modified ACRDCL converter for PWM operation [16].

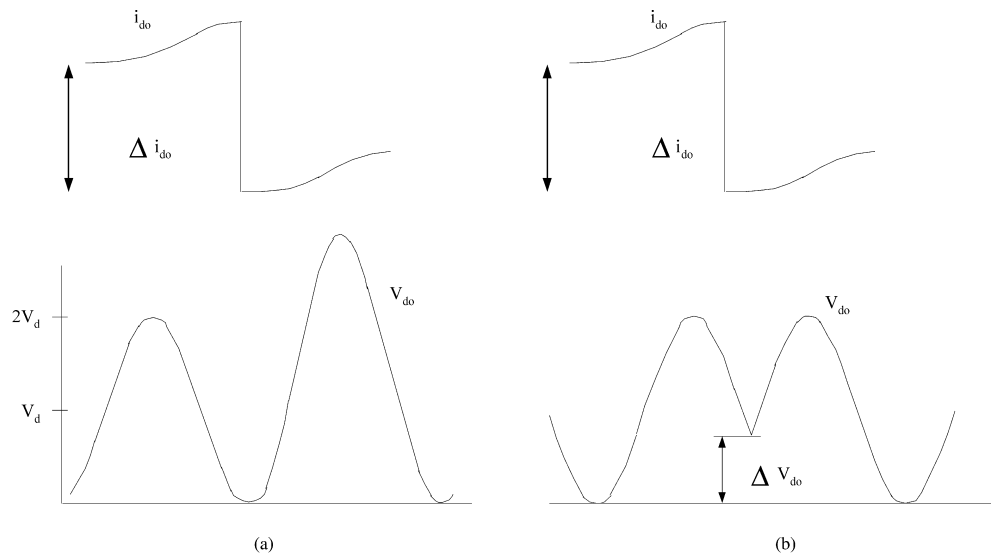


FIGURE 2.6
Principle of the voltage peak control strategy. (a) dc link current change i_{do} causes an increased resonant voltage peak of v_{do}. (b) Timing the link current change the increased voltage peak of v_{do} is avoided.

2.3.1 Notch Commutated Three-Phase PWM Converter

In the notch commutated three-phase PWM converter the zero voltage periods do not happen at discrete instants but are synchronized with a pulse from the pulse width modulator. Figure 2.8 shows the converter.

The converter link circuit makes synchronization with the converter switches possible. Until a commutation is wanted, the switch S_1 is off. Then S_1 turns on and decreases the resonant inductor current to an initial value, which ensures a resonant period with ZVS. The clamp voltage, V_k, and the size of the inductor L_{res} determine the time it takes to reach the initial current.

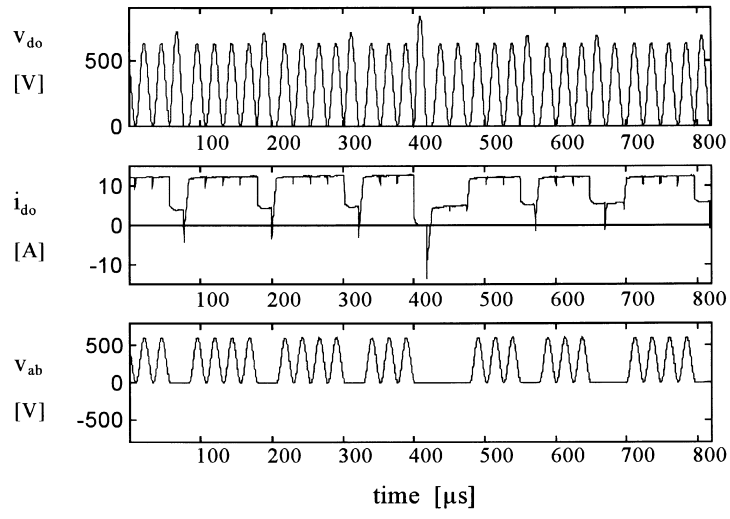
The energy in C_{res} is dissipated in S_1 at turn-on, and the clamp level is therefore low. In [14] the clamp level is about 1.2.

The converter has the desirable features of PWM, but there are turn-on losses when S_1 is turned on due to a discharge of the C_{res} capacitors.

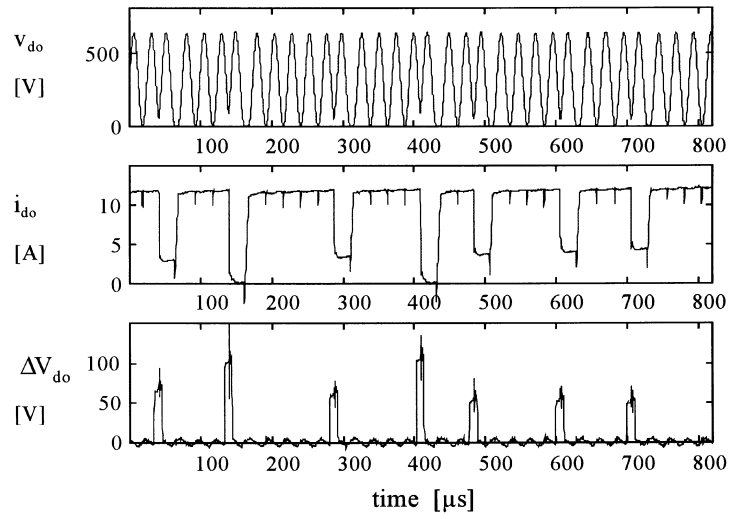
2.3.2 Zero Switching Loss PWM Converter with Resonant Circuits

This converter offers PWM and zero voltage switching like the notch commutated converter described earlier, but the voltage stress on the converter components is lower. The converter is presented in [15]. Figure 2.9 shows the converter.

The voltage stress on the converter switches is similar to PWM-VSI, but the topology requires 2 switches and 3 diodes compared to the notch converters with 1 transistor and 1 diode. The resonant circuit is different from the other described resonant circuits. It uses two resonant states, determined by changing the resonant capacitor value. Changing a resonant state makes a link oscillation possible without any dc-link voltage overshoot ($V_k = 0$). However, there is a higher current stress on the converter components.



(a)



(b)

FIGURE 2.7
(a) Experimental results of the RDCL converter. dc link voltage $V_d = 300$ V. (b) Experimental results of the RDCLVPC converter. dc link voltage $V_d = 300$ V.

2.3.3 Modified ACRDCL for PWM Operation

This converter offers zero voltage switching of the converter switches and PWM operation of the converter [16]. It is an extension of the ACRDCL with an extra switch and diode. Figure 2.10 shows the converter.

The voltage stress on the converter switches is limited to V_d, until converter switching is needed. Before the converter switching takes place, the energy of the resonant inductor L_{res} must

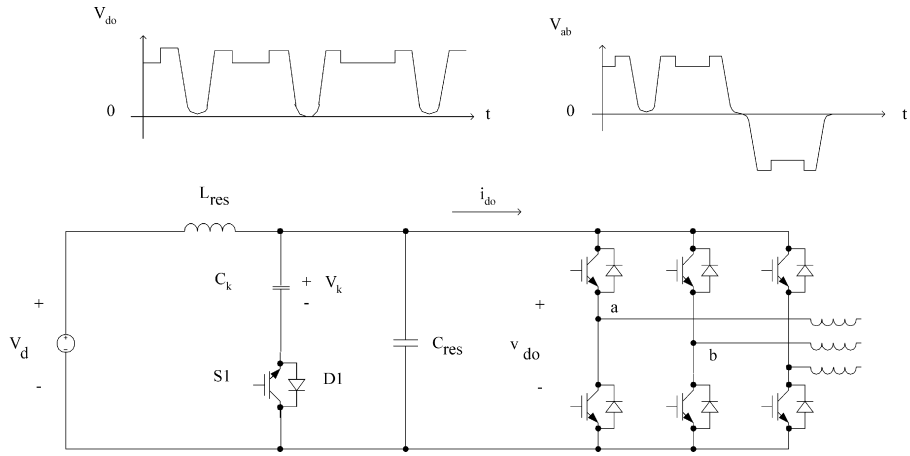


FIGURE 2.8
The notch commutated converter.

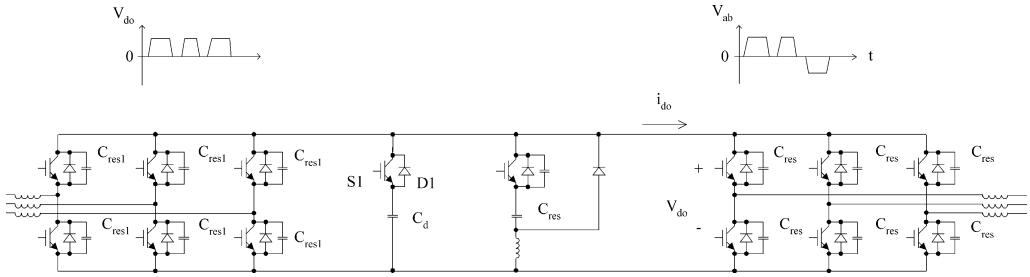


FIGURE 2.9
The zero switching loss PWM converter with resonant circuits.

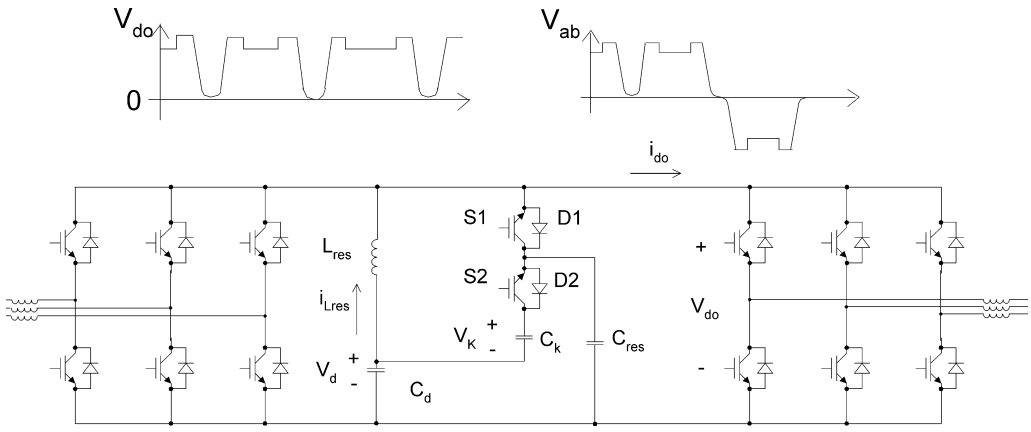


FIGURE 2.10
The modified ACRDCL for PWM operation.

increase. The resonant inductor energy is supplied from the clamp source V_k. During the charging interval of the resonant inductor the link voltage is $v_{do} = V_d + V_k$.

Finishing the resonant cycles it is necessary to clamp the voltage at $V_d + V_k$. During this clamp interval the energy applied during the charging interval of the inductor is transferred back to the clamp circuit.

2.4 MAINTAINING RESONANCE

This section describes how the resonance of the resonant circuit is kept on. At first sight the problem appears simple; after some time one realizes this is wrong. The maintaining of the resonance is a key problem that must be solved. Proper operation of the resonance ensures zero or low voltage switching of the inverter switches. During a design procedure there are several things to consider:

1. How to initiate the resonance? This can be done in a rough or a gentle way as described later.
2. The resonance must be error tolerant, meaning that if an error occurs and the resonance is prevented from completing, the resonant circuit control must be able to restore the resonance in the next resonant cycle. It is not acceptable if the whole converter stops because of electrical noise.
3. The resonant circuit stores reactive power, and in order to keep resonant circuit losses low, the level of reactive power must be kept low.
4. Finally, the circuit that controls the resonance should be capable of operating the converter at dc link voltages as high as 500 V.

Two methods are presented. The first is known as the short circuit method. The second is proposed based on the experience of working with the first described method. It is a bit more complex to describe theoretically than the short circuit method and it apparently requires a few extra components.

2.4.1 Short Circuit Method

The resonance is maintained by a short circuit of the inverter bridge legs, during the zero voltage interval. The short circuit interval ensures sufficient energy storage in the resonant inductor to overcome the circuit losses and therefore ensures that the link voltage resonates to zero voltage in the next time interval.

Several major loss elements are present in a resonant circuit, where the most significant are the serial resistance of the resonant inductor. The total resistive losses are determined from an experiment where a measurement of succeeding resonant voltage amplitudes is used to determine the quality factor, Q. With the knowledge of Z_{res} the equivalent serial resistor is $R = Z_{res}/Q$. An equation may be found which describes the level of current in L_{res} needed to overcome the resistor losses:

$$\Delta I_{Lres} = \sqrt{\frac{R\left(\frac{V_d}{Z_{res}}\right)^2}{f_{res} L_{res}}}.$$

2.4.2 Realization of the Short Circuit Method

The short circuit of the resonant inverter is done by turning all the inverter switches on when the resonant link voltage v_{do} reaches zero voltage. During the first part of the short circuit period L_{res} is properly discharged and the antiparallel diode conducts. After the resonant inductor is discharged, the current flow turns and the charging of the resonant inductor begins. The short circuit lasts until the inductor current has increased to $\Delta I_{Lres} + i_{phase}$. Since the beginning of the zero period is easy to detect, turning the short circuit on is straightforward, but turning it off is more difficult.

Several methods can be used to decide when to turn the short circuit off. A measurement of the resonant inductor current is the most direct way, but a high-speed, low-inductance current shunt is needed. Or, measure the on-state IGBT voltage drop and, from this, determine how long the IGBTs should be conducting. Implementing the method is relatively simple, but its accuracy is not good because of the on-state voltage dependency on conducted current.

One may decide to use a direct current measurement method. The advantage of this method is better accuracy, but the implementation is quite complex.

In Fig. 2.11 link current and resonant voltage are shown for a dc link voltage of 150 V. The initial inductor current is kept close to 1.5 A; a lower initial current was tried, but caused instability. An increase in the dc link voltage increases the initial resonant inductor current and the reactive losses.

2.4.3 A Non-Short Circuit Method

Transferring energy to the resonant circuit is necessary in order to compensate for loss elements. In the short circuit method this is done at the beginning of the resonant period. Another method is to transfer the energy inductively, which can be done by a secondary winding on the resonant coil, making it a transformer. The secondary side energy source is a current generator that produces pulses with the frequency of the resonant circuit as shown in Fig. 2.12. If galvanic isolation is not required the transformer may be omitted.

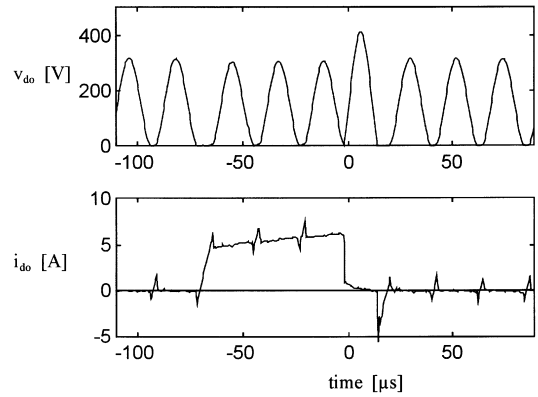


FIGURE 2.11
Measured resonant link voltage and current. The resonance is maintained by the short circuit method.

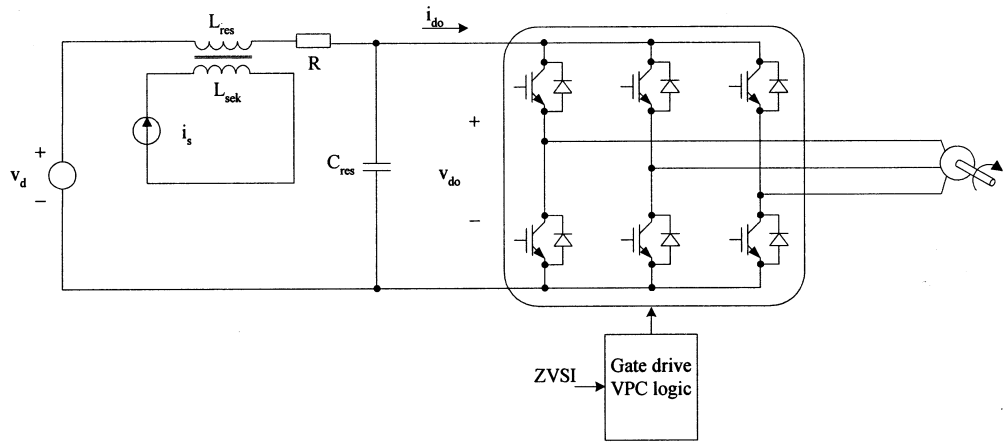


FIGURE 2.12
Non-short circuit method to maintain the resonance, using a transformer and current generator.

The current source is typically a square wave, in phase with the resonant inductor voltage. The advantage of zero-phase displacement is that the transition of current happens at zero voltage, and therefore the current source switches have low switching losses.

If there is excessive energy in the resonant circuit, it is transferred to the voltage source V_d during the conducting interval of the antiparallel diodes. If the voltage v_{do} fails to reach zero, the current generator will continue to supply the resonant circuit with energy and eventually the voltage reaches zero. This method of energizing the resonant circuit makes the resonance robust.

With an approximation assuming $R \ll Z_{res}$, the current amplitude of the current generator may be calculated:

$$\hat{i}_s = R\frac{V_d}{Z^2}.$$

In Table 2.1 two current equations are shown in the non-short circuit method box. The amplitude of i_s covers the case of a sinusoidal current source and i_{ds} is used for square wave currents.

2.4.4 A Laboratory Test of the Non-Short Circuit Method

Since there were stability problems with the short circuit method operating at dc link voltages above 300 V, the converter was first tested at the 300-V level, then a 500-V level was used. Stable converter operation was a fact, using the non-short circuit method.

Looking at Fig. 2.13 it can be seen that energy is stored in the resonant inductor at the end of a resonant period. The energy is transferred to the dc link voltage capacitor during the antiparallel diode conducting interval.

Based on simulation and laboratory experience the following is concluded about the non-short circuit method:

1. The resonance is started without current stress of the inverter switches, or any excessive stress at all.
2. If an error occurs and the resonant voltage v_{do} does not resonate below, e.g., 15 V, the resonance is not terminated, the energy transfer to the resonant circuit is continued, and the converter operation is not affected. This makes the converter operation robust.

Table 2.1 Calculation of Initial Current Using the Short Circuit Method and Current Amplitude Using the Non-Short Circuit Method

$V_d = 500\,V$, $L_{res} = 150\,\mu H$, $C_{res} = 100\,nC$, $Z_{res} = 38.7\,\Omega$, $f_{res} = 41.09\,kHz$, $R = 0.35\,\Omega$.

Short circuit method	Non-short circuit method
$\Delta i_{Lres} = \sqrt{\dfrac{R\left(\dfrac{V_d}{Z_{res}}\right)^2}{f_{res} L_{res}}}$	$\hat{i}_s = R\dfrac{V_d}{Z_{res}^2}$
	$i_{ds} = \hat{i}_s \dfrac{\pi}{4}$
$\Delta i_{Lres} = 3.1\,A$	$i_{ds} = 92\,mA$

3. The resonant converter is operated at a dc link voltage of 500 V, and there is no reason why this should not be increased.

Another advantage of the method is that no phase current or link current measurement is required.

2.5 CONVERTER MODULATION STRATEGIES

In this section discrete pulse modulation strategies are presented. Three different strategies are described briefly. The switching of the converter devices happens at discrete instants in synchronization with the link voltage zero intervals. It is not realistic to use a standard PWM strategy, since the resonant frequency is much lower than the normal clock frequency of the

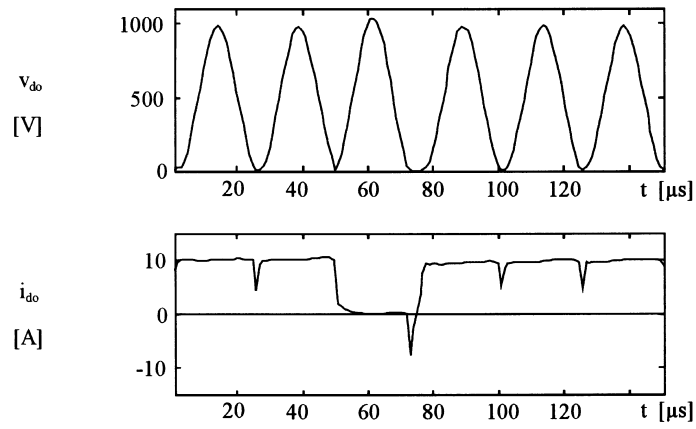


FIGURE 2.13
Measured link voltage and link current using the non-short circuit method.

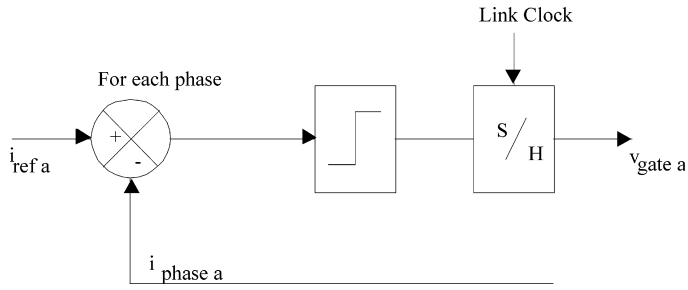


FIGURE 2.14
Delta current modulator.

PWM timer, which is in the megahertz region. Fortunately, discrete pulse modulation is available; in contrast to PWM, the switching frequency is not constant, causing an output voltage spectrum with the harmonics spread out between the fundamental and the resonant frequency. The most common modulators are described in [2, 11, 17, 18].

2.5.1 Delta Current Modulator

The delta current modulator (DCM), shown in Fig. 2.14, is a single-phase modulator with zero hysteresis comparator; the phase–phase voltage changes polarity relatively often compared to PWM. Usually PWM only allows one branch switchover between two succeeding active vectors. The resonant link current changes polarity often; therefore, the link stress is relatively high.

2.5.2 Adjacent State Current Modulator

The adjacent state current modulator (ASCM), shown Fig. 2.15, is a modification of the delta current modulator. The adjacent state modulator allows only the converter to generate succeeding active vectors that are adjacent vectors.

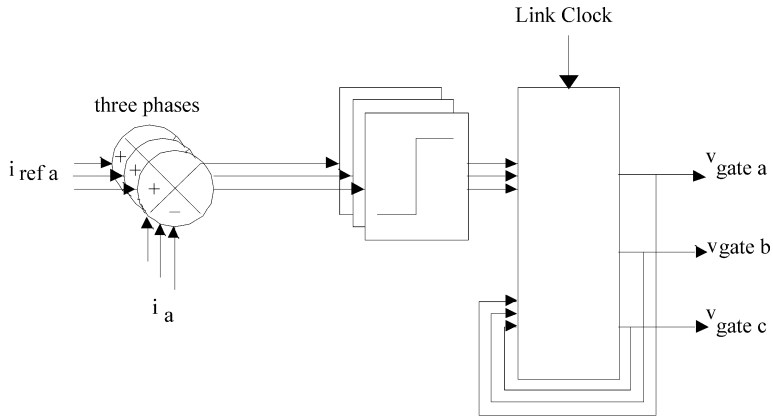


FIGURE 2.15
Adjacent state current modulator.

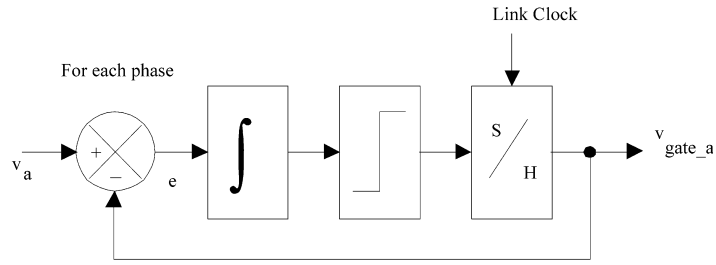


FIGURE 2.16
Single phase sigma delta modulator (SDM).

The vector sequence 100 → 110 → 010 is allowed, but the vector sequence 100 → 010 is not allowed. If the succeeding vector to an active results in more than one BSO, a zero voltage vector is selected. The zero voltage vector that is closest to the preceding vector is selected.

The use of zero voltage vectors limits the link stresses considerably because the link current reversals are eliminated.

2.5.3 Sigma Delta Modulator

Sigma delta modulators, shown in Figs. 2.16 and 2.17, are simpler to realize than the DCM and ASCM because they require only a voltage reference and no feedback from the load. The sigma delta modulator has lower dynamic performance compared to the DCM, but it has superior THD performance.

2.6 CONCLUSIONS

Resonant converters offer the advantage of soft switching, thus decreasing the switching losses relative to hard-switched converters, but this is no guarantee that the efficiency of the resonant converter is higher, because the resonant circuit is not lossless. The output voltage quality of the

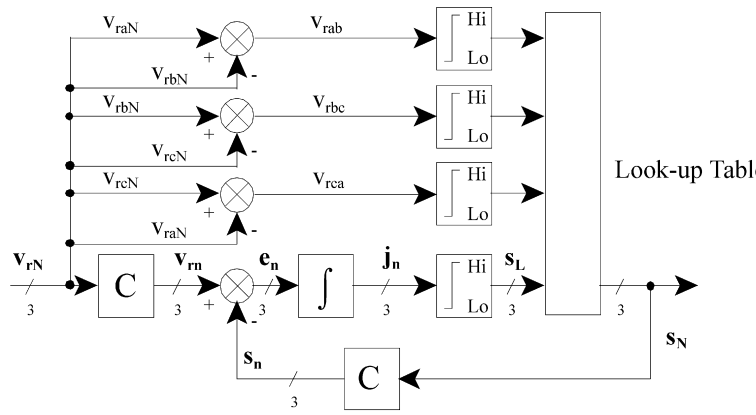


FIGURE 2.17
Space vector sigma delta modulator for a three-phase inverter.