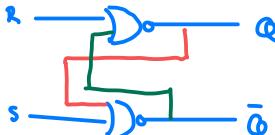


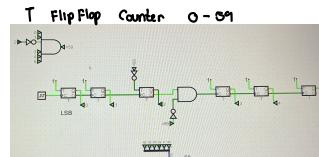
RS-LATCH

1. NOR

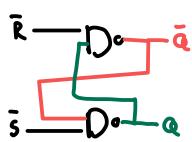


Characteristic Equations

$$\begin{aligned} R-S: \quad Q+ &= S + \bar{R}Q \\ D: \quad Q+ &= D \\ J-K: \quad Q+ &= J\bar{Q} + \bar{K}Q \\ T: \quad Q+ &= T\bar{Q} + \bar{T}Q \end{aligned}$$



2. NAND

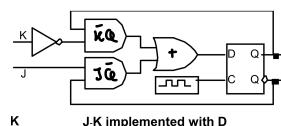


Q	Q ⁺	R	S	J	K	T	D
0	0	0	0	0	X	0	0
0	1	0	1	0	1	1	1
1	0	1	0	X	1	1	0
1	1	0	1	X	0	0	1
1	1	1	1	X	X		

HOLD
RESET
SET
Not Allowed

Excitation table

Q	Q ⁺	R	S	J	K	T	D
0	0	X	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	1	0
1	1	0	X	X	0	0	1



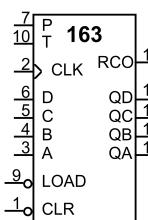
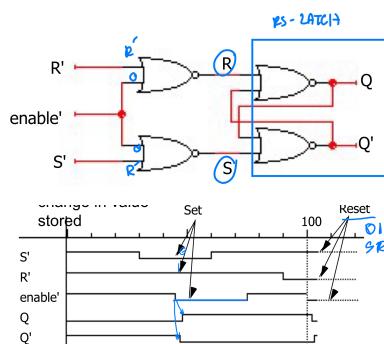
\rightarrow K-map vs Q^+

कॉन्क्रिप्शन वाला वा

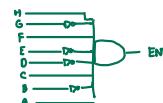
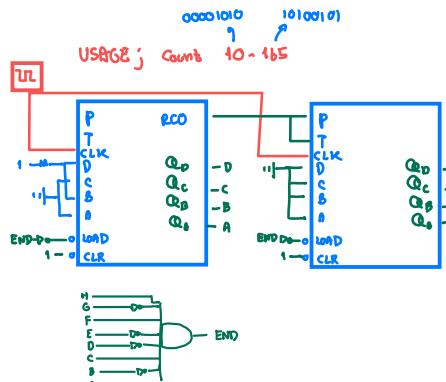
J, K तरी

$D = J\bar{Q} + \bar{K}Q$

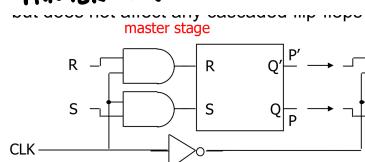
GATED RS-LATCH



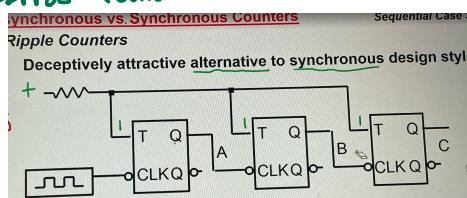
74163 counter



MASTER SLAVE



RIPPLE Counter

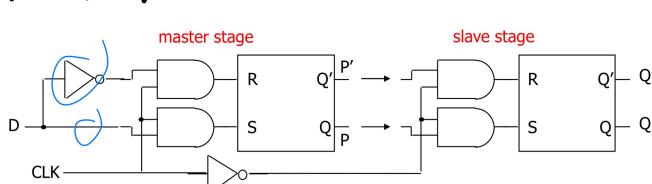


JK - FLIPFLOP

J(t)	K(t)	Q(t)	Q(t+Δ)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

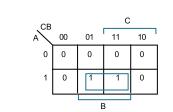
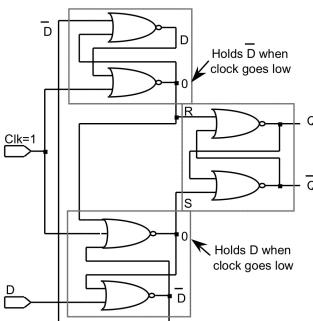
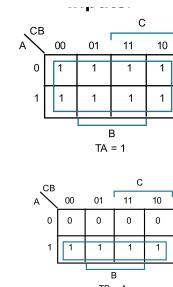
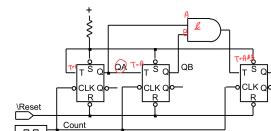
HOLD
RESET
SET
TOGGLE

D - Flip Flop



Present State		Next State		Flip Flops Inputs				
C	B	A	C+	B+	A+	TC	TB	TA
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	1	0	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Resulting Logic Circuit



$TC = A \cdot B$