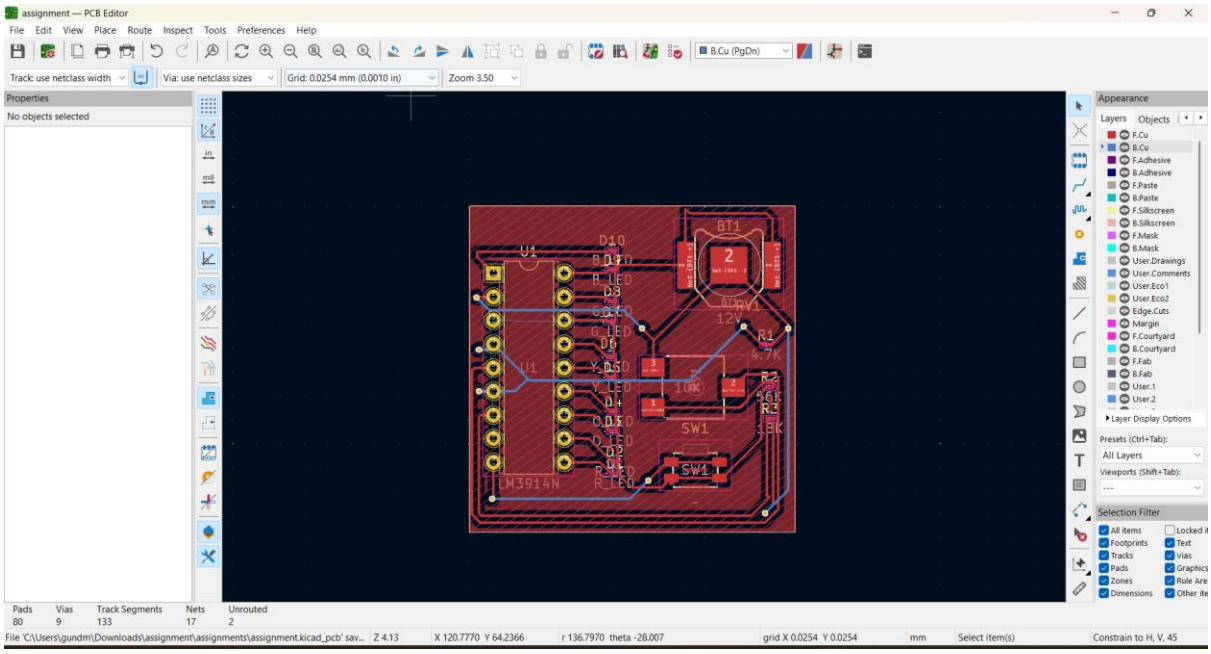
PCB Design Considerations



Layer Stack-up (4-layer)

A 4-layer stack-up is ideal for clean power delivery and signal integrity:[4]

1. **Top Layer (Signal/Component):** NPM1100, all SMD components, critical high-speed traces (e.g., SW node if buck switch external, though the NPM1100 is integrated).
2. **GND Layer (Internal):** Solid **Ground Plane** for noise reduction, thermal dissipation, and short return paths. This is crucial for the buck regulator's performance.
3. **Power Layer (Internal):** Dedicated planes for (5V) and (3.0V), or split and planes.
4. **Bottom Layer (Signal/Trace):** Routing for non-critical signals, and large copper pours for headers and mounting holes.

Layout and Routing

- **Compactness:** The board size is restricted to . Place the NPM1100 and associated ceramic capacitors (,) **as close as possible** to minimize loop inductance, which is critical for good performance of the integrated buck regulator.
- **Thermal Management:** The NPM1100's QFN package uses its **center pad** for both electrical grounding and **thermal dissipation**. This pad must be connected to the internal **GND plane** using a generous array of **thermal vias**.
- **Decoupling:** , , and must be placed immediately adjacent to the relevant NPM1100 pins.
- **Charge Sense Resistor ():** Place close to the ISET pin and connect it directly to the ground plane.
- **Headers:** Place pin headers (J1-J4) along the edges of the PCB for easy access. The host I/O header (J4) should include pins for: , GND, ENABLE, SHIP_MODE, CHG_STATUS, PWR_STATUS, and .