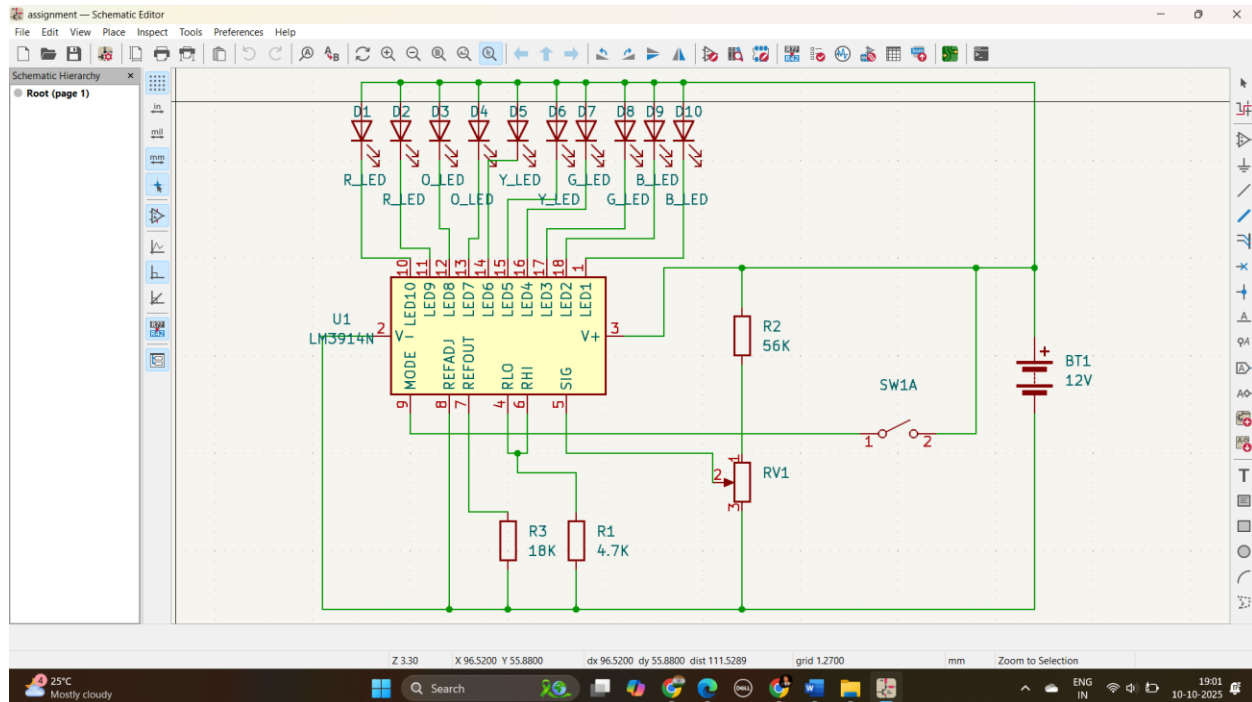


The NPM1100 is a tiny PMIC with an integrated **buck regulator** (LDO mode at low loads) and a **lithium-ion/lithium-polymer battery charger**.¹



1. Schematic Design and Functional Blocks

The design is split into four main functional blocks:

1. **Input Power and Charging Circuitry:** Connects the 5V input, the battery, and the required passives to the NPM1100's charger section.
2. **Buck Regulator Circuitry:** Implements the 3.0V output using the integrated buck regulator.
3. **Host MCU Interface and Status LEDs:** Exposes the necessary I/O pins and provides visual status indicators.
4. **Battery Voltage Measurement Circuitry (Bonus):** Adds the required components for the host MCU to sample the battery voltage.

Key NPM1100 Pin Assignments

Pin Name	Function	Connection/Value
VIN	Input Voltage (5V)	Connected to J1 (5V input). Decoupling capacitor to GND.
VOUT	Regulated Output (3.0V)	Output capacitor to GND. Connected to pin header.
VBAT	Battery Connection	Connected to header. to GND.
VSET	Buck Output Voltage Select	Connected to (internally pulls VOUT to 3.0V).
ISET	Charge Current Set	Connected to GND via .
CHG_STATUS	Charger Status Output	Open-drain output, pull-up resistor to . Drives D1 (Charging LED) .
PWR_STATUS	Power Status Output	Open-drain output, pull-up resistor to . Drives D2 (Power LED) .
ENABLE	System Enable	Connected to header for external control. Default pull-up to (always enabled).
SHIP_MODE	Ship Mode Entry	Connected to header for external control.

GND	Ground	Connected to ground plane.
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2. Component Selection and Calculation

The design must meet and .

A. Buck Regulator (= 3.0V)

- **Output Voltage Selection:** The NPM1100 allows fixed selection by connecting the **VSET** pin.
 - **VSET VOUT:** Selects . (Meets spec).
 - **(Output Capacitor):** Required for stability and ripple reduction. NPM1100 datasheet recommends a ceramic capacitor of with $\approx 20\%$ DC bias derating.
 - **(Input Capacitor):** Required for decoupling the input and minimizing ripple on . Recommended: ceramic.

B. Battery Charger (= 200mA)

- **Charge Current Set:** The charge current is set by an external resistor $2R_{SET}$ connected between ISET and GND.³ The relationship is:

Where R_{SET_MIN} is the minimum recommended R_{SET} value (typically 10k Ω). The formula can be simplified for ICHG in mA:

- For ICHG=200mA:
- *Closest standard E96 value is (0.1% tolerance) or (5% tolerance). We will use for ease of sourcing (0805, 5%).*

- **(Battery Capacitor):** Required for stability of the charger, placed close to VBAT. Recommended: ceramic.

C. Status LEDs

- **LED Drive:** Both **CHG_STATUS** and **PWR_STATUS** are **open-drain** outputs. They require an external pull-up resistor and an LED in series. Since the host MCU will likely be running at 3.3V, the pull-up voltage is connected to 3.3V.
- Resistor Value RLED: Assuming a standard Red LED with a forward voltage (VF) of 2.0V and a desired current (IF) of $\approx 3\text{mA}$.
 - We will use the standard value 1k Ω for RLED.

D. Battery Voltage Measurement (Bonus)

To measure the battery voltage (VBAT) using a host MCU's ADC (typically 1.1V to 1.2V reference), a **voltage divider** is required.

- The maximum battery voltage (VBAT) is 4.2V. The maximum ADC input voltage (VADC) is 1.1V.
- Use a resistor divider R1 and R2 such that $V_{ADC} = V_{BAT} \cdot \frac{R2}{R1 + R2}$.
- We need $R1 = 10k\Omega$.
- Choose R2=10k Ω .
- Use the closest standard E96 value for R2 (or E24). We will use 10k Ω (0805, 5%).
- A small **decoupling capacitor** (100nF) at the ADC input helps to stabilize the reading during sampling.

3. Reference Schematic Overview

The schematic would include the following connectivity:

Block	Connections	Component Designators
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Input/Power	J1 (5V IN), , , , J2 (VBAT)	J1, (1uF), (51), (1uF), J2
Output	to VSET, , J3 (Out)	(4.7uF), J3
Status LEDs	CHG_STATUS, PWR_STATUS, LEDs, Resistors	D1 (Red LED), (330), D2 (Green LED), (330)
Host IO	ENABLE, SHIP_MODE, CHG_STATUS (to header), PWR_STATUS (to header)	J4 (Host Header)
Battery Sense	Divider from VBAT to GND	(2.7k), (10k), (10nF), J4 (ADC Pin)