EC340 COMPUTER ORGANISATION AND ARCHITECTURE

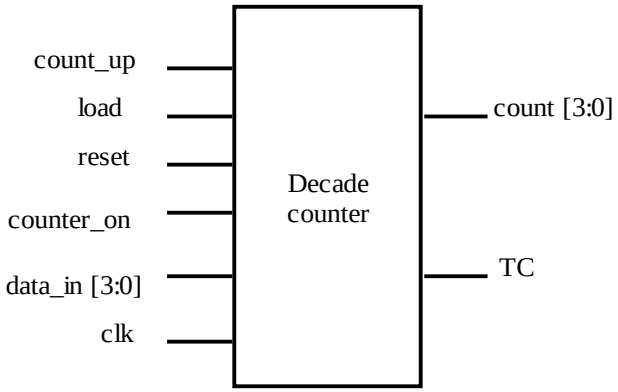
Assignment 1

Date of submission – February 16, 2022

The assignment can be done as a group of 2 students. Only one submission is required per group.

Write a Verilog code and (i) implement it on Intel Cyclone V (5CSEMA5F31C6) FPGA and find the device utilization statistics and timing reports (ii) verify it on modelsim simulator. The report should include all assumptions; block diagrams, etc. needed to understand your code, simulation waveforms, device utilisation statistics, timing reports etc. The verilog codes (including testbench) with proper comments has to be uploaded

1. (a) 8 bit ripple carry adder (b) 8 bit controllable adder/subtractor
2. **Decade Counter** - Model a synchronous up/down decade counter with asynchronous reset. The counter is rising edge triggered.
   If the **load = 1**, the data **data_in** is loaded into the counter.
   If the **counter_on=counter_up=1,** the counter is incremented, the Terminal carry output **TC=1** when the counter is in state 9
   If the **counter_on=1 and counter_up=0,** the counter is decremented, the Terminal carry output **TC=1** when the counter is in state 0.



3. Serial adder to add two 8 bit numbers using a single full adder and registers
4. Shift and add multiplier in Verilog to multiply two 8 bit numbers using RTL approach. It should be capable of multiplying both positive and negative numbers. Negative numbers are represented in 2'sC representation.
5. To compute the factorial of a 3 bit number using RTL approach.