EC340 COMPUTER ORGANISATION AND ARCHITECTURE

Exercise – Single cycle MIPS

Date of submission – March 26, 2022

The assignment can be done as a group of 2 or 3 students. Only one submission is required per group.

The Verilog code corresponds to the single cycle MIPS and supports the following instructions – add, sub, lw, sw, beq, slt. Simulate the verilog code for the single cycle MIPS processor with the test bench provided in the link. Make sure you understand the code and it executes correctly before you do the exercise.

1. Add the following MIPS instructions – addi, bne, j (use the MIPS instruction encoding format)
2. Test using the assembly level code for Q1 in Exercise L22 (*Assume that you have an array of 10 elements with base address in $s0. Write an assembly program to find the minimum value from the array and swap it with the last element in the array*) Use SPIM to get the machine language code. Make sure your code uses the 3 new instructions you added (addi, bne & j)