■ STA Fundamentals - Key Notes Summary

■ Static Timing Analysis Basics

Static Timing Analysis (STA) is a fast, exhaustive, and deterministic method to verify timing of digital circuits without simulation vectors. It checks all possible timing paths and ensures that setup and hold constraints are met for reliable operation.

■ STA vs Dynamic Timing Analysis

STA does not require test vectors and checks all paths, making it faster but conservative compared to dynamic timing analysis which uses simulation vectors and reports actual delays.

■ Timing Path Types

1. Register-to-Register – Launch FF → Capture FF 2. Input-to-Register – Input → Capture FF 3. Register-to-Output – Launch FF → Output 4. Input-to-Output – Pure combinational path

■ Setup and Hold Time

• Setup Time (Tsu): Data must be stable before the clock edge. Equation: Data Arrival + Tsu ≤ Clock Arrival Fixes: Reduce delay or increase clock period. • Hold Time (Th): Data must remain stable after the clock edge. Equation: Data Arrival ≥ Clock Arrival + Th Fixes: Add delay or buffer.

■ Slack Calculations

Setup Slack = Data Required (setup) - Data Arrival Hold Slack = Data Arrival - Data Required (hold) Positive slack means timing met; negative means violation.

■■ Key Timing Metrics

• WNS (Worst Negative Slack): Most severe violation • TNS (Total Negative Slack): Sum of all violations • FEP (Failing End Points): Number of failing paths Goal: WNS ≥ 0, TNS = 0, FEP = 0

■■ Clock Definitions

Example Constraints (TCL): create_clock -name CLK -period 10 [get_ports clk] set_clock_latency 1.5 [get_clocks CLK] set_clock_uncertainty 0.5 [get_clocks CLK] Clock parameters: Period, Latency, Uncertainty, Transition.

■■ Timing Path Analysis

Path = Startpoint (Launch FF) → Logic → Endpoint (Capture FF) Delays = Cell Delay + Net Delay (RC parasitic)

■ Timing Exceptions

• set_false_path – Ignore invalid paths • set_multicycle_path – Multi-cycle operations • set_case_analysis – Mode-specific timing

■ Key Takeaways

■ Fast, exhaustive, and vectorless analysis. ■ Early feedback for large designs. ■■ Beware of over-constraining, missing exceptions, or incorrect clocks.

■■ STA Flow

1. Read design (netlist + libs) 2. Apply constraints (SDC) 3. Run analysis (report_timing) 4. Check WNS/TNS violations 5. Fix and optimize