Roll No.:

NATIONAL INSTITUTE OF TECHNOLOGY JAMSHEDPUR

AUTUMN SEMESTER 2023-24

Department of Computer Science & Engineering

MID SEMESTER EXAMINATION (OCTOBER 2023)

Course Code: 3102 Course Title: Computer Organization & Architecture

Day: Wednesday

Date: 18.10.2023

Course Instructor (Name of the Faculty): Dr. A. K. Mehta

Max. Marks: 30

Duration: 02 Hours

INSTRUCTIONS:

1) All questions are compulsory.
2) All questions are of equal value. Candidates have to answer all parts of a particular question at one place.
3) The figures in the right hand margin indicate full marks.

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1. (a) Perform the following subtractions of binary numbers using 2's complements: [2]
   (i) $101 - 0.11$ (ii) $0.11 - 0.101$
   (b) An 4 bit input word 1101 on transmission is received as 1001. How the SEC code if used can rectify the error? [3]
   (c) Realize other logic operations using NAND gates. [2]
   (d) Simplify the Boolean function F together with the don't-care conditions d in (i) sum-of-products form and (ii) product-of-sums form. [3]

$$F(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 10)$$
$$d(A, B, C, D) = \sum(5, 6, 11, 15)$$

2. (a) Explain the following: [4]
   (i) Full Adder (ii) 2's Complement Adder-Subtracter
   (iii) Multiplexer (iv) Decoder
   (b) Distinguish between D Latch built using NOR gates and NAND gates. [2]
   (c) Explain bidirectional shift register. [4]

3. (a) Discuss the working of JK flip-flop. [5]
   (b) If $\overline{Q}$ output of a D flip-flop is connected to D input, what is the output? [2]
   (c) Clock and input D is given in Fig. 1, draw the output of D flip-flop. [3]

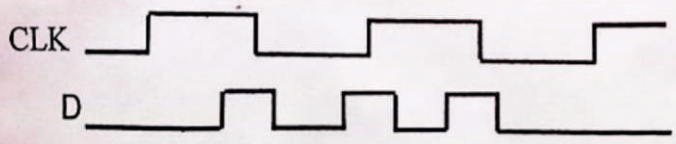

Fig. 1.

Roll No.: 2022PGCSCA 103

NATIONAL INSTITUTE OF TECHNOLOGY JAMSHEDPUR

AUTUMN SEMESTER 2022-23

Department of Computer Science & Engineering

MID SEMESTER EXAMINATION (OCTOBER 2022)

Course Code: 3102 Course Title: Computer Organization & Architecture

Date: 20.10.2022 Day: Thursday

Course Instructor (Name of the Faculty): Dr. A. K. Mehta

Duration: 02 Hours Max. Marks: 30

INSTRUCTIONS:

1) All questions are compulsory.
2) All questions are of equal value. Candidates have to answer all parts of a particular question at one place.
3) The figures in the right hand margin indicate full marks.

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1. (a) Convert the following numbers as per instructions against each: [2]

$(375.25)_{10} = (?)_2 = (?)_8 = (?)_{16}$

(b) An 8 bit input word 01011011 on transmission is received as 01010011. How the SEC code if used can rectify the error? [3]

(c) Explain one application of XOR & XNOR gates each. [1]

(d) Simplify the following Boolean function in product-of-sums form by means of a four-variable map.

$F(A, B, C, D) = \sum(2, 3, 4, 5, 6, 7, 11, 14, 15)$ [2]

Draw the logic diagram with

(i) OR-AND gates (ii) NOR gates [2]

2. (a) Explain the following: [4]

(i) Controlled Inverter (ii) 2's Complement Adder-Subtracter

(iii) Multiplexer (iv) Full Adder using two Half Adders

(b) Distinguish between D Latch built using NOR gates and NAND gates. [2]

(c) Explain bidirectional shift register. [4]

3. (a) Discuss the working of edge-triggered D flip-flop. [5]

(b) If $\overline{Q}$ output of a D flip-flop is connected to D input, what is the output? [2]

(c) Clock and input D is given in Fig. 1, draw the output of D flip-flop. [3]

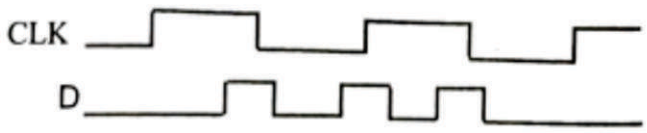

Fig. 1.

MID-SEM 2022

NATIONAL INSTITUTE OF TECHNOLOGY JAMSHEDPUR

AUTUMN SEMESTER 2021-22

Department of Computer Applications

MID SEMESTER EXAMINATION (NOVEMBER 2021)

Course Code: 3102 Course Title: Computer Organization & Architecture

Date: 26.11.2021 Day: Friday

Course Instructor (Name of the Faculty): Dr. A. K. Mehta

Duration: 02 Hours Max. Marks: 30

INSTRUCTIONS:

1) All questions are compulsory.
2) All questions are of equal value. Candidates have to answer all parts of a particular question at one place.
3) The figures in the right hand margin indicate full marks.

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1. (a) Perform the following subtractions of binary numbers using 2's complements: [2]
   (i) $101 - 0.11$ (ii) $0.11 - 0.101$
   (b) An 4 bit input word 1101 on transmission is received as 1001.
   How the SEC code if used can rectify the error? [3]
   (c) Realize other logic operations using NOR gates. [2]
   (d) Simplify the Boolean function F together with the don't-care conditions d in (i) sum-of-products form and (ii) product-of-sums form.
   $F(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 10)$
   $d(A, B, C, D) = \sum(5, 6, 11, 15)$ [3]

2. (a) Explain the following: [6]
   (i) Full Adder (ii) 2's Complement Adder-Subtracter
   (iii) Multiplexer (iv) Decoder (v) PAL (vi) PLA
   (b) Distinguish between D Latch built using NOR gates and NAND gates. [2]
   (c) Explain the role of PRESET and CLEAR in flip-flops. [2]

3. (a) Discuss the working of JK flip-flop. [5]
   (b) If $\overline{Q}$ output of a D flip-flop is connected to D input, what is the output? [2]
   (c) Clock and input D is given in Fig. 1, draw the output of D flip-flop. [3]

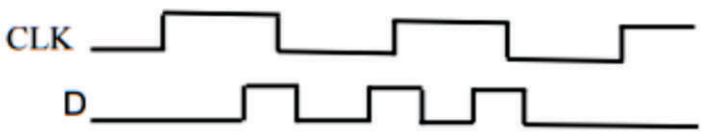

Fig. 1.

Roll Number: _____ Name of student:

NATIONAL INSTITUTE OF TECHNOLOGY, JAMSHEDPUR

Department of Computer Applications

Autumn End Semester Examination, April, 2021

MCA (I Year): I[st] Semester

Course Code: CA 3102

Course Name: Computer Organization and Architecture

Date of Exam: 19/04/2021

Time: 3 Hours, M. Marks: 50

Name of Faculty: Dr. Mudassir Rafi

Note: Attempt any ***five*** questions. Each question carries ***ten*** marks. Marks distributions for questions are visualized at extreme right.

Question 1:

a) Convert the following numbers into corresponding base: **(3)**

$(242)_{10} = (?)_{16}$

$(121)_8 = (?)_{16}$

$(?)_2 = (E3)_{16}$

b) Justify the use of parity bit check for error detection? convert $(0110)_{BCD}$ to Excess-3. **(2+1)**

c) Simplify the following boolean functions using four variable K map and design the corresponding combinational circuit.

$F(A, B, C, D) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ **(4)**

Question 2:

a) Discuss how a flip flop is different from a logic gate. Convert a D flipflop into T flipflop, write all the conversion steps clearly. **(3 + 3)**

b) How you can resolve the race around condition in a JK flipflop. Find the output frequency of a decade counter which is applied with a clock frequency of 10 Mhz. **(2.5 + 1.5)**

Question 3:

a) Define a Machine instruction. What are the various instruction formats? **(2+2)**

b) Evaluate x=(a+b)*(c+d) using zero address instruction and one address instruction. **(3+3)**

Question 4:

a) Define pipelining A 5-stage pipelined processor has the stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any

instruction. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Operand forwarding is used in the pipeline (for data dependency, OF stage of the dependent instruction can be executed only after the previous instruction completes EX). What is the number of clock cycles needed to execute the following sequence of instructions?

MUL R2, R10, R1
DIV R5, R3, R4
ADD R2, R5, R2
SUB R5, R2, R6

(2+3)

b) Differentiate between RISC and CISC architecture. **(3+2)**

Question 5:

a) Memory Hierarchy in the computer system increases the efficacy of the system, Justify this statement? **(5)**

b) What is the average memory access time for a machine with a cache hit rate of 80% and cache access time of 5 ns and main memory access time of 100 ns, consider hierarchical access of memory? **(3)**

c) Differentiate between Cache and Main memories. **(2)**

Question 6:

a) Comment on the need of Full adder circuit over Half adder circuit. Design a circuit for 4-bit parallel adder. **(2+3)**

b) Describe the role of flip flop in making registers. Write a short note on the two-type classification of registers. **(2+3)**

Question 7:

a) Describe Triggering with clock? **(4)**

b) What is an interrupt. Describe DMA. **(3)**

c) Consider an instruction pipeline with four stages with the stage delays 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. The delay of an inter-stage register stage of the pipeline is 1 nsec. What is the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation? **(3)**

END-SEM 2021