A

Mini Project Report on

DESIGN OF AREA EFFICIENT AND LOW POWER 4-BIT MULTIPLIER BASED ON FULL - SWING GDI TECHNIQUE

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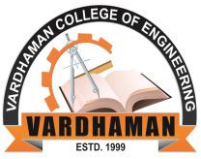

Department of Electronics and Communication Engineering

VARDHAMAN COLLEGE OF ENGINEERING, HYDERABAD

an autonomous institute affiliated to JNTUH

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CERTIFICATE

This is to certify that the mini project report work entitled **"Design of Area Efficient and Low Power 4-Bit Multiplier Based on Full- Swing GDI Technique "** carried out by **Seetaram Oruganti**, Roll Number 17881A0443, **Sahithi Poloju** , Roll Number 17881A0433, **Vamshi Ponugoti**, Roll Number 17881A0454, submitted to the department of Electronics and Communication Engineering, in partial fulfillment of the requirements for the award of degree of **Bachelor of Technology** in **Electronics and Communication Engineering** during the year 2020-21.

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ABSTRACT

This paper presents a design of 4-bit multiplier using full adder cell based on full swing gate diffusion input technique. The proposed adder design consists of 18 transistors and compared with different logic styles for full adders through cadence virtuoso simulation based on TSMC 65nm models at a supply voltage of 1v and frequency 250MHz. The simulation results showed that the proposed full adder design dissipates low power while improving the area and provides full swing output voltage among all the designs taken for comparison. The proposed full adder used to design Array, Braun and Baugh Wooley multipliers, Energy and Transistor count of these multipliers improved compared to CMOS. As we have don't have the required 65nm technology in infrastructure. we have first implemented in 180 nm, 90 nm and 45 nm with transistor width of 120 nm which was default and the outputs when observed are very good in 45nm when compared to remaining technologies.so we have proceeded with 45 nm. The outputs can be made clearer and more accurate by altering the width of transistor.

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ABBREVATIONS

GDI	Gate Diffusion Input
PDA	Personal Digital Assistant
VLSI	Very Large-Scale Integration
FS	Full Swing
CMOS	Complementary Metal Oxide Semiconductor
TG	Transmission Gate
PTL	Pass Transistor Logic
SOI	Silicon On Insulator
DPL	Double Pass transistor Logic
WCDMA	Wireless Code Division Multiple Access
OFDM	Orthogonal Frequency Division Multiplexing
CSA	Carry Save Adder
FA	Full Adder
DSP	Digital Signal Processing
TSMC	Taiwan Semiconductor Manufacturing Company

CHAPTER 1

INTRODUCTION

Due to the heavy interest in usage of digital integrated circuits for portable devices such as cellular communications, phones, battery, laptops and personal digital assistant (PDAs), etc., the need for small chip circuits, power consumption and speed are vital factors should be taken into consideration while choosing the VLSI design with high performance.

1.1 Importance of GDI Technique:

An addition is a basic arithmetic operation heavily demanded in VLSI design such as multiplier and accumulator (MAC), microprocessor, digital signal processing applications, so the system performance will be affected by the performance of full adder. A full adder is essential in arithmetic operation such as division, subtraction addition, and multiplication. Enhancing energy will influence the whole system so energy must be improved. This can be achieved by GDI technique. The aim of this work is to design 4-bit multiplier using a full adder circuit based on full-swing GDI to reduce power consumption, delay and area, in addition, to achieve full-swing output with high performance.

Most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication, and multiply and accumulate (MAC) are examples of the most commonly used operations. The 1-bit full-adder cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of larger circuit. For such submicron CMOS technology area, topology selection, power dissipation and speed are very important aspect for high. speed and low power application. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. Several optimization techniques for full adder design are reported in the literature [1-10]. Among Gate Diffusion Input (GDI) is a lowest power design technique which offers improved logic swing and less static power dissipation. Using this technique several logic functions

can be implemented using less number of transistor counts. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to TG and CMOS).

To reduce the power consumption different logic design techniques like CMOS complementary logic, Pseudo nMOS, Dynamic CMOS, Clocked CMOS logic (C2 MOS), CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed [2-4]. Although Static CMOS Logic has been the most popular design approach for the past three decades, many attempts have been made to propose a better alternative to achieve lower power dissipation, smaller area and better performance reported in [11-12]. Circuit designed with transmission gate (TG) solves the problem of low logic level swing by using PMOS as well as NMOS but this implementation needs true and complemented control signal and requires more area than pass transistor logic. Pseudo-NMOS is simple and fast but reduces noise margins and increases power consumption. Pass-transistor logic is good for certain classes of circuits (MUX/adders). On the other hand, PTL implementations of logic gates such as NANDs and NORs were found to be slower and consume more power than CMOS implementations mainly because of the reduced output swings due to the threshold drop across a single-channel pass transistor. The main contribution of this paper presents the design of modified primitive cells and five different topologies for full adders at circuit level implemented based on the GDI technique. The modified GDI primitive cells are constructed and its significant variation between CMOS and conventional GDI are compared. Though GDI technique offers low power, less transistor count and high speed, the major challenges occurs in the fabrication process. The GDI technique requires twin-well CMOS or Silicon on Insulator (SOI) process to realize a chip which increases the complexity as well as the cost of fabrication.

1.2 Gate Diffusion Input Technique

This technique consumes a small silicon area, it can achieve complex function using only two transistors as listed in table I, However, this technique was suggested for manufacturing in twin-well CMOS process and silicon on insulator. It improved power consumption and propagation delay.
low power GDI technique and small silicon area of VLSI digital circuit as an alternative to complementary metal oxide semiconductor (CMOS) logic design. As illustrated in fig. 1.1 primitive GDI cell.

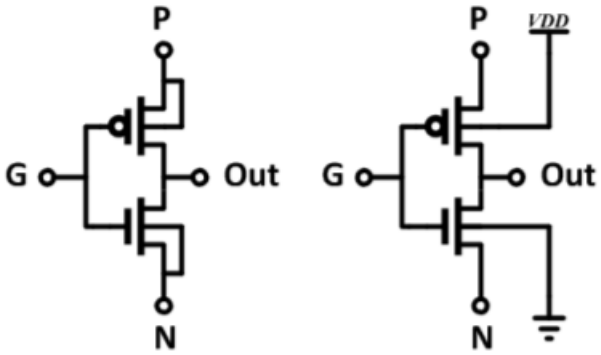


Fig 1.1 Basic GDI cell and Modified GDI Cell

Unfortunately, this logic style suffered from some limitation such as non-full swing output voltage due to threshold drop which means that output either high or low deviate from VDD or GND by the threshold voltage for PMOS or NMOS.

1.3 Basic GDI Functions

At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

N	P	G	OUT	Function
0	B	A	$\overline{A}$B	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT
$\overline{B}$	B	A	$\overline{A}$B+A$\overline{B}$	XOR
B	$\overline{B}$	A	$\overline{A}$ $\overline{B}$+AB	XNOR

Table 1.1 Basic Gates Realization Using GDI Cell

1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

Most of the designed circuits were based on the F1 and F2 functions. The reasons for this are as follows. 1) Both F1 and F2 are complete logic families (allows realization of any possible two-input logic function). 2) F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased. 3) When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOS.

Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method.

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table 1.2 Various Logic Functions of GDI Cell For different input Configurations

bulks to Out are directly polarized and there is a short between N and P, resulting in static power dissipation and . This causes a drawback for OR, AND, and MUX implementations in regular CMOS with configuration. The effect can be reduced if the design is performed in floating-bulk SOI technologies, where a full GDI library can be implemented. In that case, floating-bulk effects have to be considered. As can be seen, the GDI cell structure is different from the existing PTL techniques, reviewed in Section I, and has some important features, which allow improvements in design complexity level, transistor count, and power dissipation. Understanding of GDI cell properties demands a deeper operational analysis of the basic cell in different cases and configurations.

CHAPTER 2

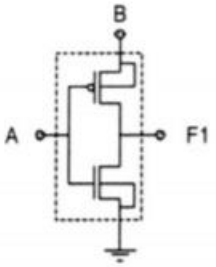
ANALYSIS OF GDI CIRCUITS

2.1 Operational Analysis of GDI Cell

One of the common problems of PTL design methods is the low swing of output signals because of the threshold drop across the single-channel pass transistors. In existing PTL techniques, additional buffering circuitry is used to overcome this problem.

To understand the effects of the low swing problem in a GDI cell, we suggest the following analysis, based on the example of F1 function, and can be easily extended to use in other GDI functions. Table II presents a full set of logic states and related functionality modes of F1.

As can be seen from Table II, the only state where low swing occurs in the output value is $A = 0, B = 0$. In this case, the voltage level of F1 is V_{Tp} (instead of the expected 0 V) because of the poor high-to-low transition characteristics of the pMOS pass transistor . It is obvious that the only case (among all the possible transitions) where the effect occurs is the transition from $A = 0, B = V_{DD}$, to $A = 0, B = 0$.



A	B	Functionality	F1
0	0	*pMOSTrans Gate*	V_{Tp}
0	1	*CMOSInverter*	1
1	0	*nMOS Trans Gate*	0
1	1	*CMOSInverter*	0

Table 2.1 Input logic state versus functionality and output swing of F1 function

The fact that demands special emphasis is that in about 50% of the cases (for $B = 1$), the GDI cell operates as a regular CMOS inverter, which is widely used as a digital buffer for logic-level restoration. In some of these cases, when V_{DD} **= ' 1 '.**without a swing drop from the previous stages, a GDI cell functions as an inverter buffer and recovers the voltage swing. Although this feature allows a self-swing restoration in certain cases, in this paper the worst case is assumed and additional circuitry is used for swing restoration in the implemented circuits.

2.2 Modified GDI Technique

This logic style is suitable for fabrication in a standard CMOS process; as well realize improvement in output voltage, power and power delay product compared to basic GDI logic. Although the threshold drop problem, not fully resolved, and the output voltage still degrades.

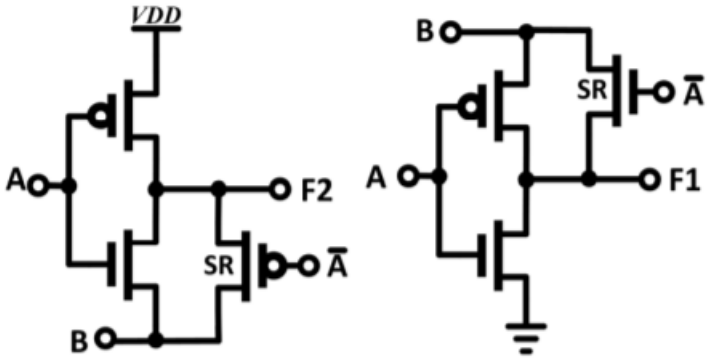


Fig 2.2(a) FS GDI cell(F2) Fig 1.2(b)FS GDI cell(F1)

The threshold drop problem was solved and the output swings degradation, improved by using the full swing GDI technique. This new approach for design utilizes only swings restoration transistor (SR) to produce full swing operation for F1 and F2 functions as shown in fig. 2 (a) and (b). One of two functions F1 or F2 or a combination of both can be used to realize many logical functions. This approach utilizes more transistors than standard GDI, however, as compared to complementary metal oxide semiconductor (CMOS), swing restoration complementary pass transistor logic (SR-CPL), double pass transistor logic (DPL) and Hybrid CMOS logic style, it utilizes a fewer number of transistors and achieves full swing output, consumes low power, energy efficient and smaller area.

CHAPTER 3

MULTIPLIER

3. MULTIPLIER

The multiplier is heavily demanded in a microprocessor, digital signal processing to perform the high computational operation in image processing and video coding and computer sector like wireless code division multiple access (WCDMA), carrier synchronizers and orthogonal frequency division multiplexing (OFDM) based wireless devices.

There are many architectures of multiplier using different algorithms to perform a multiplication operation [12]. There are three steps to realize multiplying operation: partial product generation, partial product addition, and the final adding process. The basic components of multipliers are AND gates, Full Adders, and Half Adders. To improve the performance of the system these circuits should be optimized. The different multipliers are Array, Barun and Baugh Wooley multiplier.

While the multiplier can be used to produce thousands of volts of output, the individual components do not need to be rated to withstand the entire voltage range. Each component only needs to be concerned with the relative voltage differences directly across its own terminals and of the components immediately adjacent to it.

Typically a voltage multiplier will be physically arranged like a ladder, so that the progressively increasing voltage potential is not given the opportunity to arc across to the much lower potential sections of the circuit.

Note that some safety margin is needed across the relative range of voltage differences in the multiplier, so that the ladder can survive the shorted failure of at least one diode or capacitor component. Otherwise a single-point shorting failure could successively over-voltage and destroy each next component in the multiplier, potentially destroying the entire multiplier chain.

3.1 Array Multiplier

Array multiplier is the simplest structure of parallel multiplier. This multiplier using the standard add and shift operation based on 'add and shift' algorithms to perform a multiplication operation. The structure of 4-bit array multiplier is presented in fig. 3. The partial products generator consists of n number of 'AND' gates to multiply the multiplicand with each bit of the multiplier and then

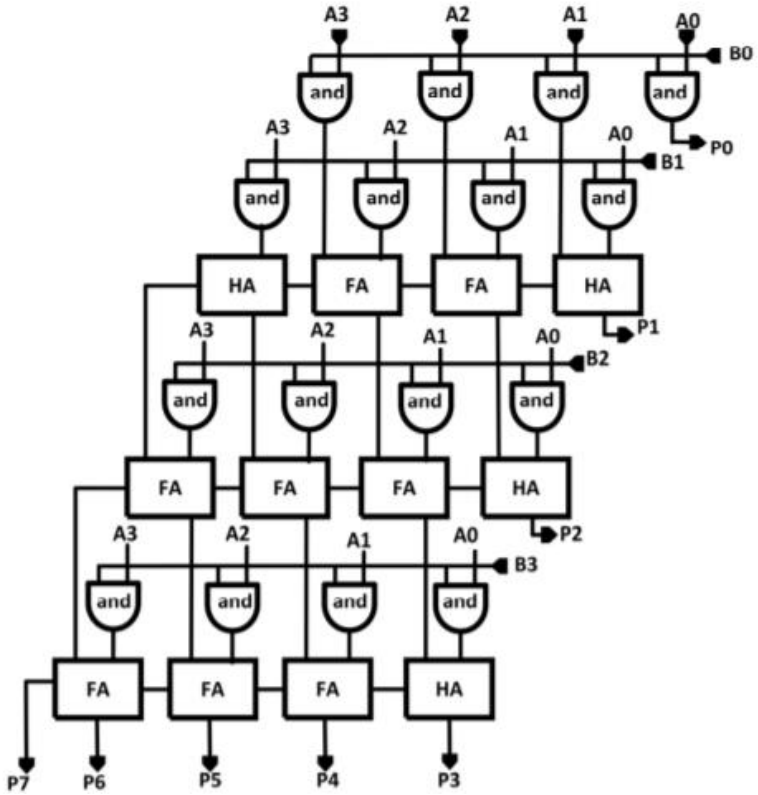


Fig 3.1 4 X 4 Array Multiplier

3.2 Barun Multiplier

Barun multiplier is a linear multiplier, which has a regular structure and known as carry-save array multiplier. This multiplier operate based on the fact that not add immediately "the carry bits" that are outputs of the first stage but are saved for the next addition stage. As shown in fig. 4. 4x4 Braun multiplier, which consists of (4-1) rows of carry-save adders (CSAs) and a (4-1) bit ripple-carry adder in the last row and each row contains (4-1) full adder (FAs). The main advantage of Barun multiplier that it has only one critical

path rather than many paths found in the array multiplier and this is the most widely used in DSP applications due to consuming low power.

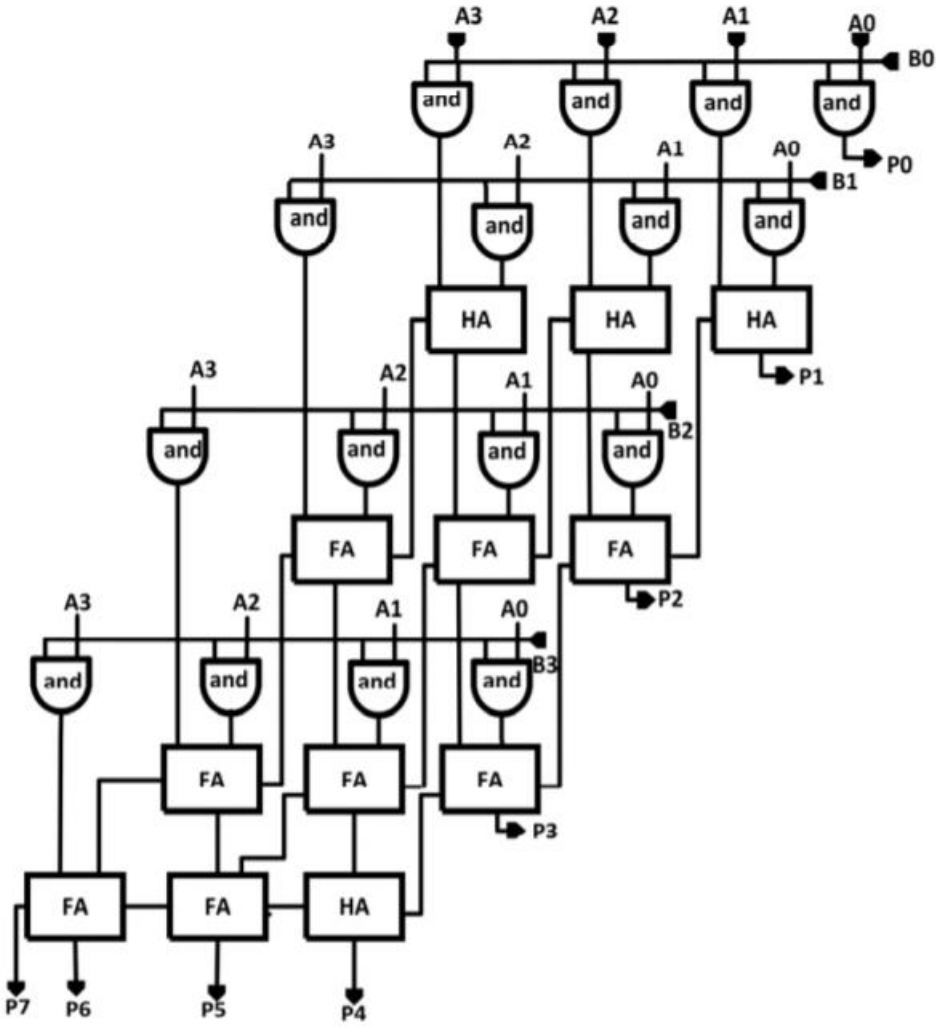


Fig 3.2 4X4 Barun Multiplier

3.3 Baugh Wooley Multiplier

A Baugh Wooley multiplier based on parallel array architecture. This multiplier is used for both unsigned and signed number multiplication. Signed number operands which are represented in 2's complemented form to make sure that the signs of all partial products are positive. The 4x4 Baugh Wooley

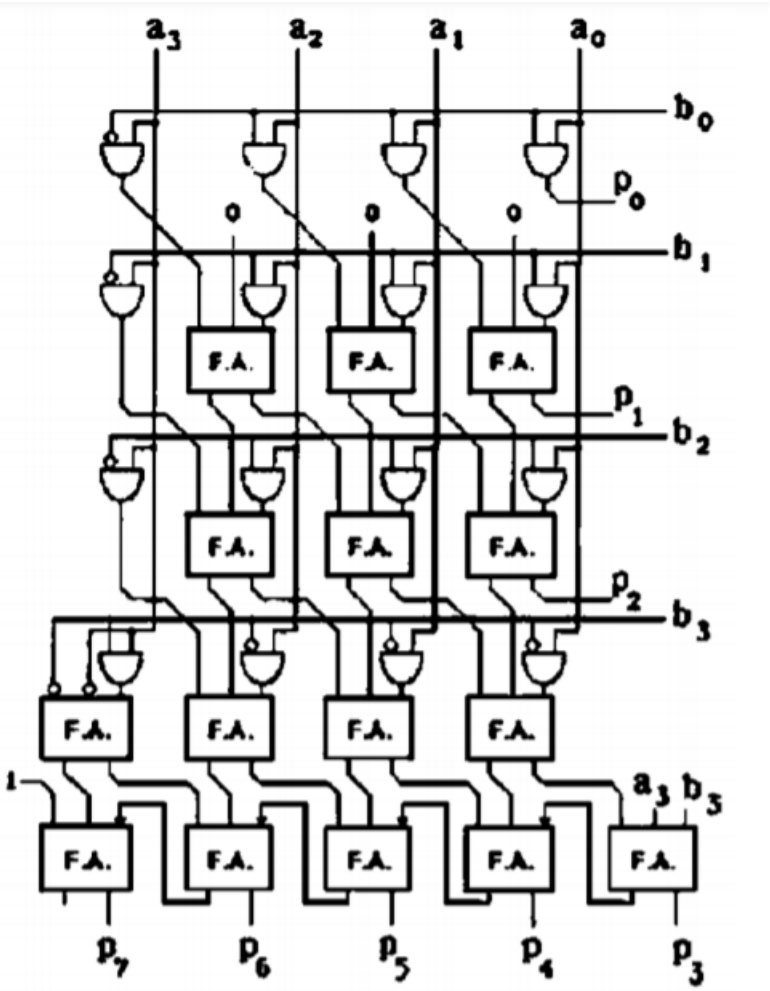


Fig 3.4 4X4 Baugh Wooley Multiplier

CHAPTER 4
FULL ADDER

4.FULL ADDER

4.1 Block Diagram of Full Adder

A full adder is a combinational circuit that performs many arithmetic operations of 3 logic bits. It is consists of 3 blocks (XOR, XOR, and MUX) the block diagram of full adder shown in fig. 6. According to Previous studies, the best implementation for Block 1 was discussed. block 1 was built by logical design: a XNOR-XOR gate to obtain expressions (A ⊕ B) and A ⊕ B. The total power consumption and propagation delay of the full adder circuit affected by the delay and the voltage swing of the XNOR - XOR signal and its complement created within the cell.

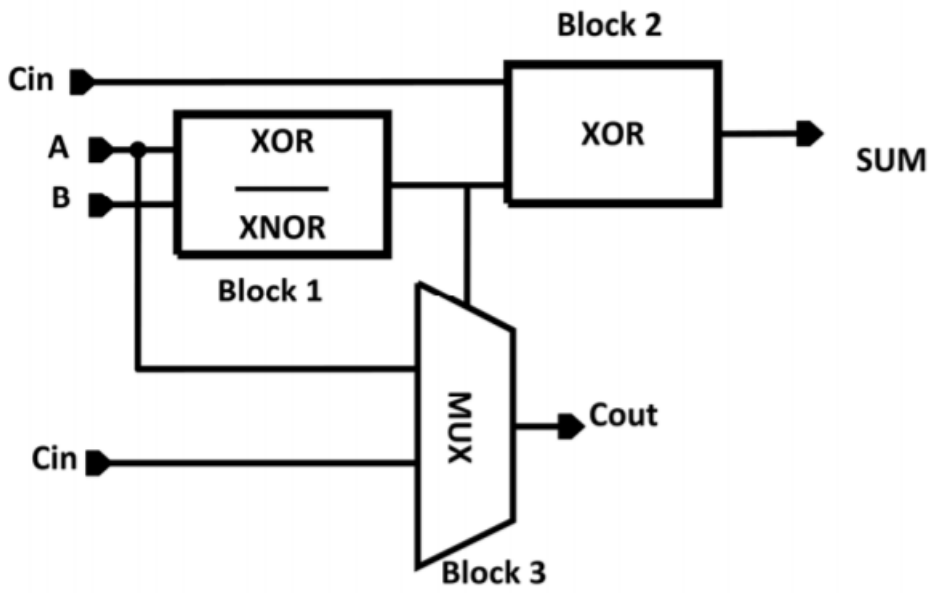


Fig 4.1 Block Diagram of Full Adder

XOR Gate XOR gate is the basic building block for the realization of various digital circuits such as a multiplier, comparator, adder, decoder, and compressor. The expression of the XOR function presented in equation 1

$$A \oplus B = A'B + AB' \quad \ldots\ldots(1)$$

4.1 XOR – XNOR circuit

A low power XOR and XNOR (LP XOR-XNOR) using 4 transistors, Which consumes low power, but suffers from non-full swing outputs voltage at XOR logic when input signal AB=00 all PMOS transistor switched on and passes weak logic 0, and at XNOR gate all NMOS transistor switched on and passes weak 1 and no drive capability, Ming Wang enhanced that by using CMOS inverter [7]. Transmission gate logic style proposed to design low power [8], high-speed module and small area but has degradation in output voltage.

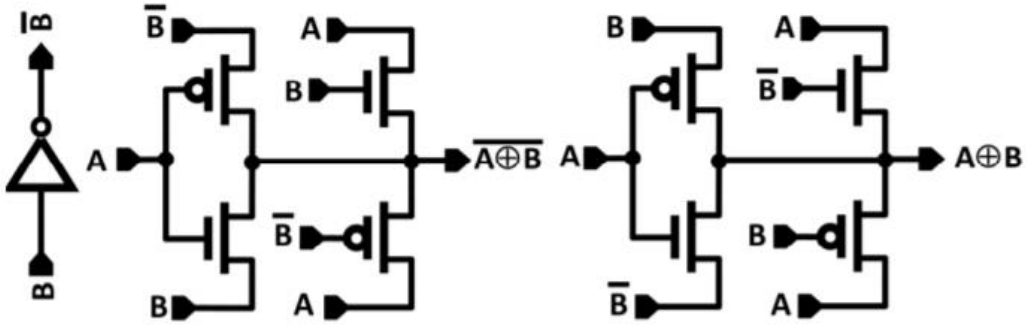


Fig 4.2 (a) XNOR realization (b) XOR realization Using GDI technique

The Above Circuits When Implemented in GPDK 180, 90 and 45 nanometers The outputs are comparatively good in GPDK 45nm .but not so efficient to increase the efficiency making the circuit in more Compressed Technologies gives good outputs and by also changing the transistors width . as we doesn't have lower technologies at facility we have decided to move to take another module of XNOR -XOR circuit form the paper []. The following is the XNOR- XOR module that is replaced with below circuit.

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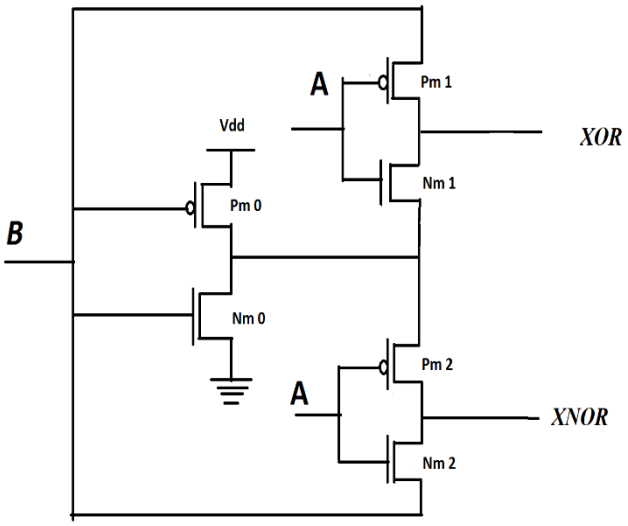

Fig 4.3 Non-full swing XOR-XNOR circuit based on GDI cell.

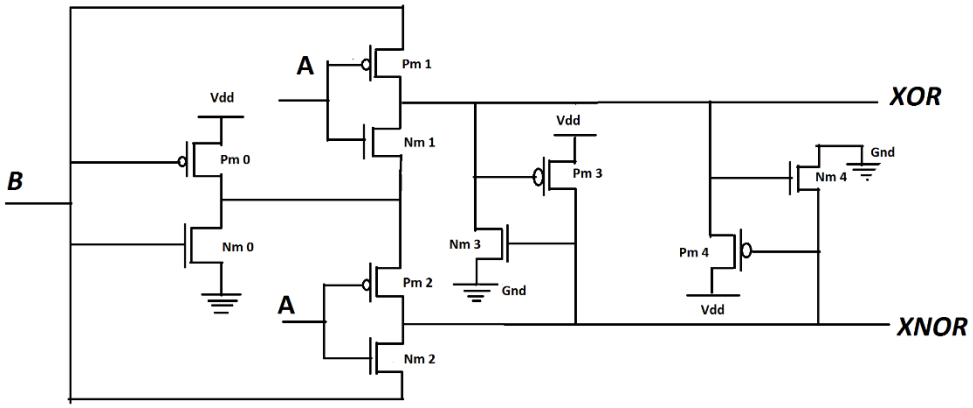

Fig 4.4 Full swing XOR-XNOR circuit based on GDI Cell.

4.2 Multiplexer (Module3)

The basic multiplexer (MUX) has a number of input lines and one output line. A multiplexer chooses the output from inputs based on a select signal [11]. The circuit in figure .6 presents GDI MUX uses only 2 transistors, but the main disadvantage it generates non-full swing output. Morgenstein solved this problem by using two cells of GDI MUX [4], whereas the function as presented in expression (2) achieved and full swing output obtained as shown in fig. 8 2×1 Multiplexer consists of 6 transistors.

$$MUX = S'A + SC \text{ ……..(2)}$$

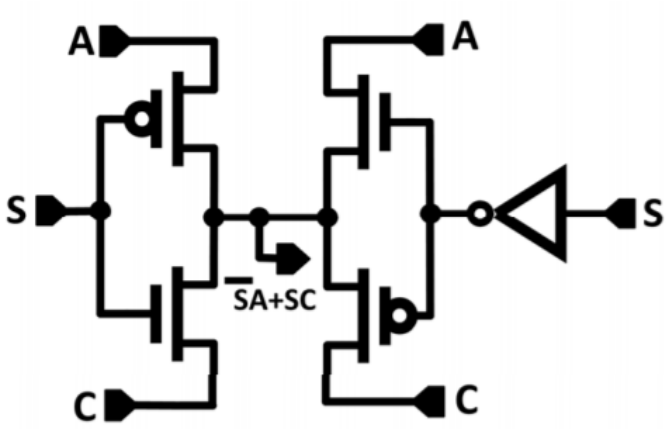

Fig 4.5 FS GDI MUX

4.3 Design of Full Adder

The proposed design consists of 18 transistors to implement 1-bit full adder as shown in fig. 9. The first function summation of 3 inputs A, B, and the carry out from the previous stage called implemented by module 1 using XNOR-XOR and module2 using XOR. Module 1 has an inverter to generate the function B through 2 transistors Mp1 and Mn1, while Mn2 and Mp2 implement A $\oplus$ B and full swing output achieved by swing restoration transistors Mn3 and Mp3. XNOR Function generated by transistors Mp4 and Mn4 and full swing output achieved by swing restoration transistors Mn5 and Mp5 instead of an inverter that used in ref [10] to generate XNOR function which consumes more power, this function drive the second module in the circuit. Module 2 generate the final output of the summation function as presented in equation (3) Carry out generated by module 3 which consists of 4

transistors. When (A ⊕ B) equals 1 then Cin passes through Mn9 and Mp8 to carry out, but if it equals 0, input

$$SUM = A \oplus B \oplus C \ldots\ldots\ldots\ldots\ldots\ldots (3)$$
$$C_{out} = A(A \oplus B) + C_{in}(A \oplus B) \ldots (4)$$

A pass through Mp9 and Mn8 to carry out to realize the carry resulting of summation as presented in expression (4). The truth table of the 1-bit full adder is given in Table II.

A	B	Cin	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4.1 Full Adder Truth Table

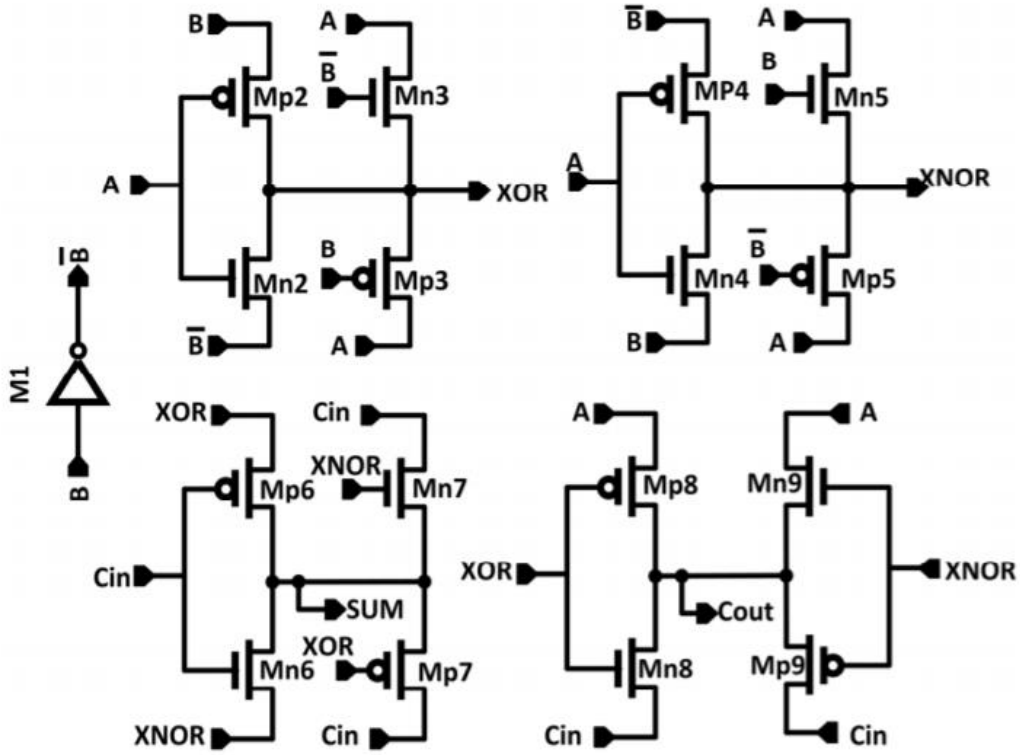

Fig 4.6 Schematic Diagram of Exiting Circuit

CHAPTER 5

RESULTS

EXECUTION FLOW

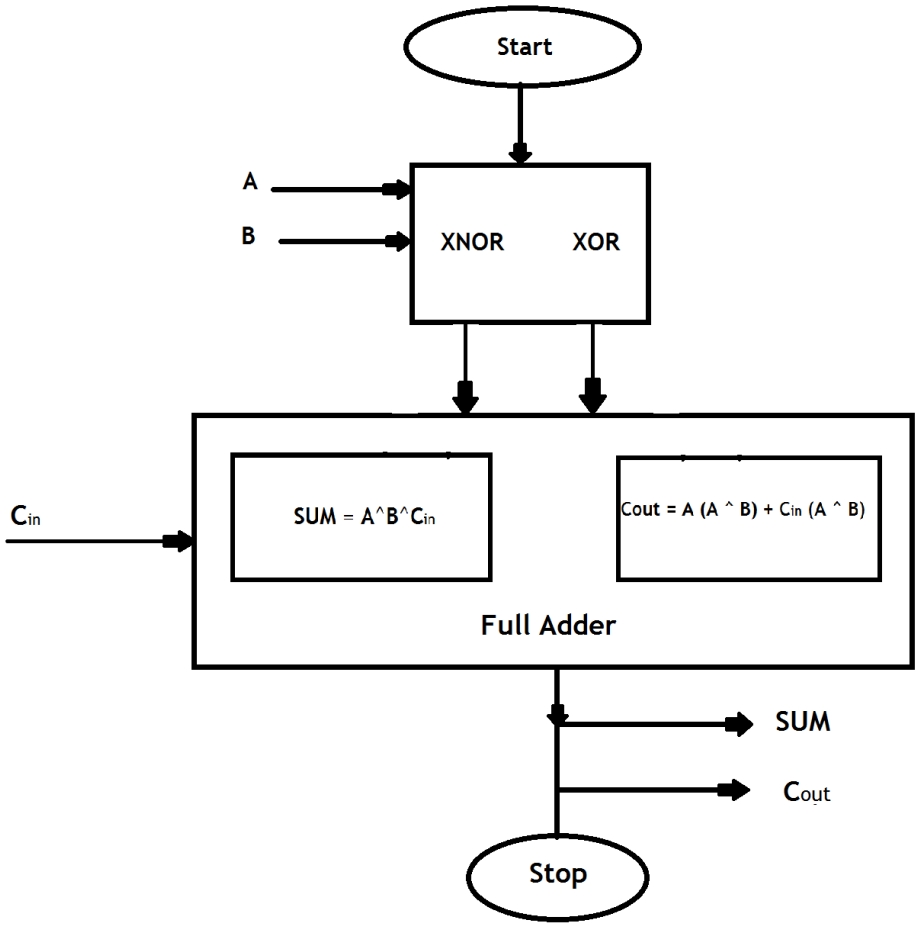

Fig 5.1 Execution flow

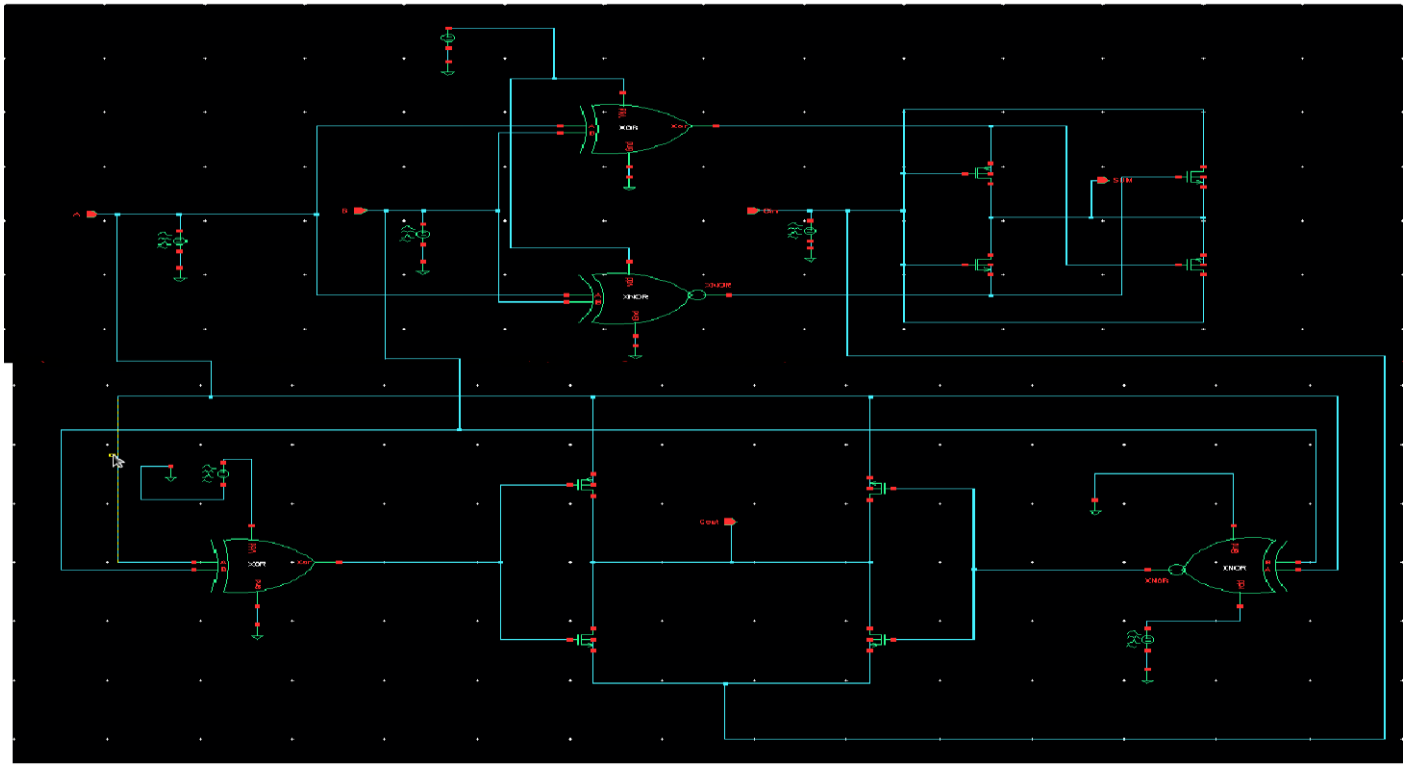

Fig 5.2 Design using Existing Circuit

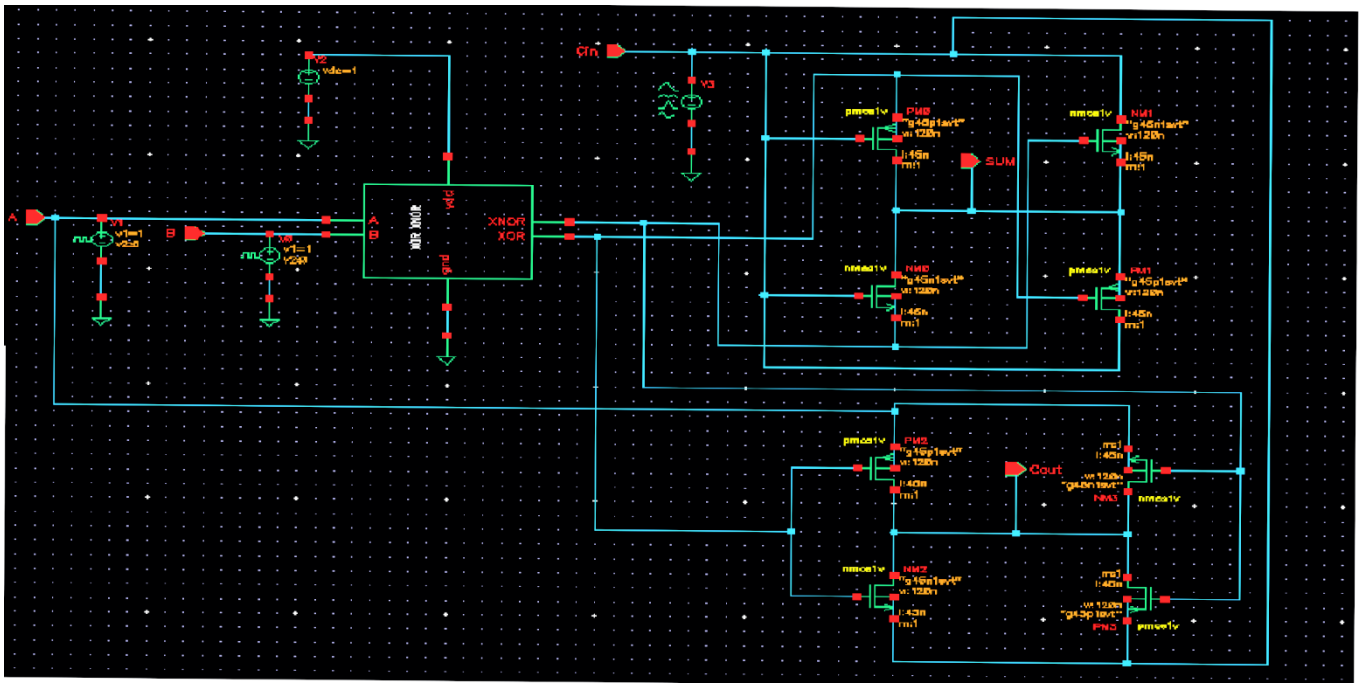

Fig 5.3 Design using Modified Circuit

SIMULATED GRAPHS

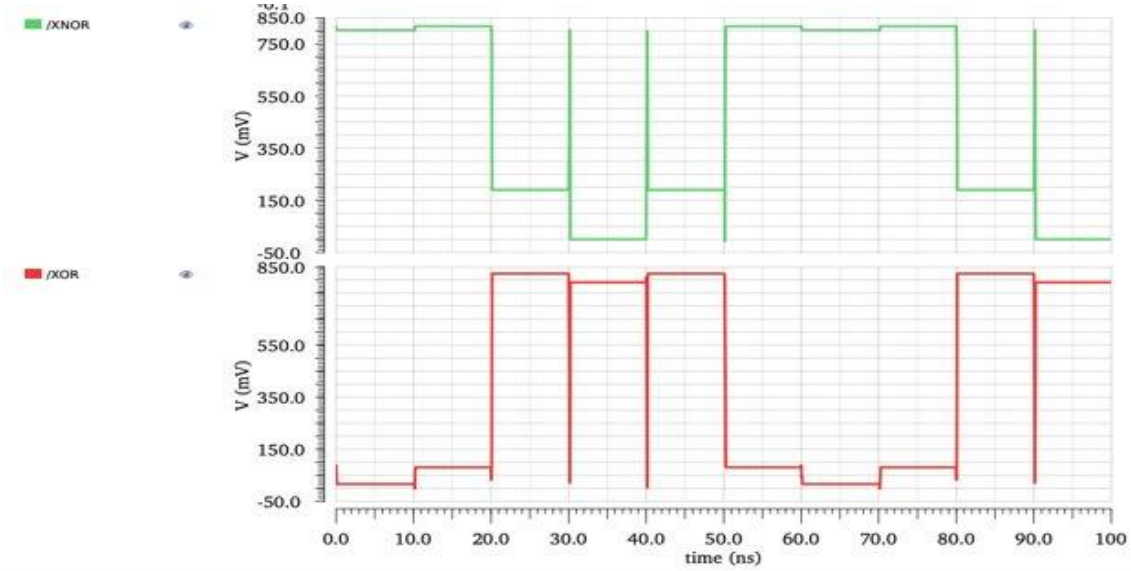

Fig 5.4 Modified XOR-XNOR Circuit Graph

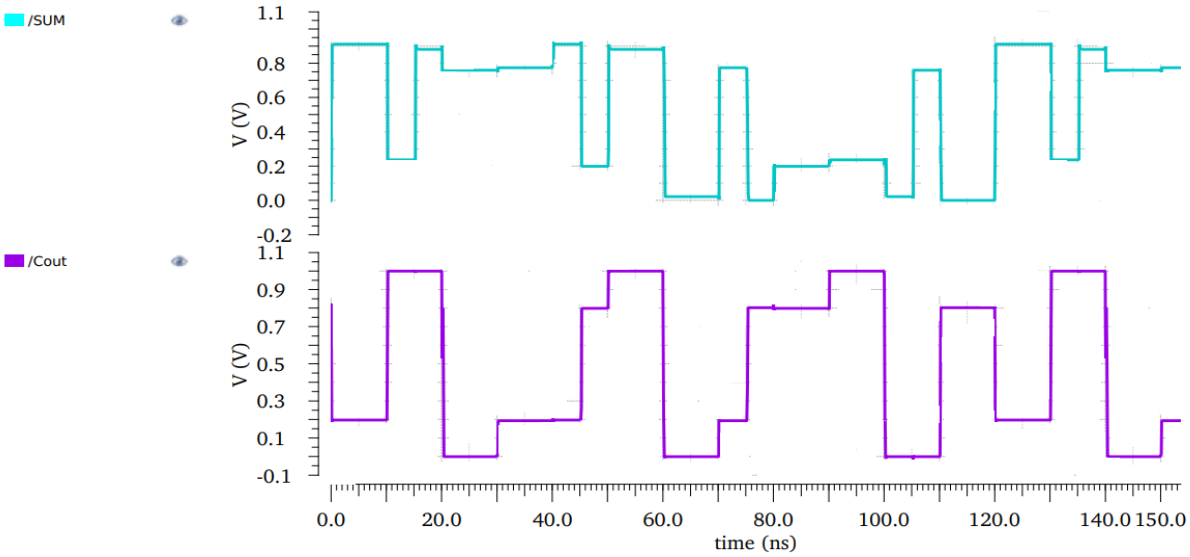

Fig 5.5 1-Bit Full Adder Output

SIMULATION RESULTS AND COMPARISON

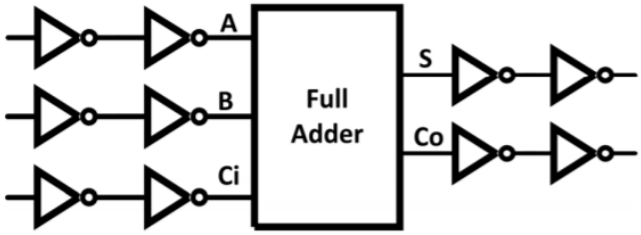

Fig 5.6 Full Adder Test Bench

The Simulation of the proposed 1-bit Full Adder design, alongside with C-CMOS, CPL, DPL, TG, Hybrid, Hybrid CMOS, Mirror, SR-CPL, and GDI designs was carried out using TSMC 65nm technology process. Inputs (A, B. C_{in}) are loaded with buffers before they are fed to the adder cell, outputs Sum and C_{out} also loaded with buffer. The XOR gate and different type of multiplier also tested using the same method. This simulation setup is shown in fig. 10.

It provides a similar situation to realistic conditions where the cell has both a driving circuit and a driven circuit. Simulations were done using The Spectre based Cadence Virtuoso simulator with a power supply of 1V and frequency 250MHz, the size of PMOS is twice the NMOS transistor size Wp/L=240/60, Wn/L=120/60 (PMOS and NMOS) respectively to achieve the best power and delay performance. Figures (11) and (12) shows the waveform of non-full swing output and full swing GDI XOR gate, respectively, the results of FS-GDI XOR compared with different logic styles shown in Table IV, Energy is less by 56% the SRCPL. The results of the proposed full adder compared with the previous logic styles utilized in the internal structure of full adder in terms of power, delay and energy (PDP) as shown in Table V.

Design	Power (uW)	Delay (pS)	PDP (e-18J)	No.of Transistors
CPL[14]	6	63.8	382	38
C-CMOS [15]	4.1	65.75	269.5	28
(TG) [7]	4.4	40	189	18
Mirror [16]	4.8	39	187.2	28
GDI[11]	6.4	80	512	18
SR-CPL[6]	4.43	31	137.33	26
DPL[6]	5.3	35	172.25	28
(Hybrid)[16]	4.2	43	180.6	18
TG+GDI[17]	4.3	48.6	209	21
(Hybrid-CMOS) [18]	4.2	84.5	203.7	24
PROPOSED	4	37.5	150	18

Table 5.1 Simulation result of different multiplier architecture In TSMC 65 NM CMOS process Technology at 250 MHz

Design	Power (uW)	Delay (pS)	PDP (e-18J)	No.of Transistors
Array Multiplier-CMOS	53.8	146	7854.8	400
Array Multiplier-GDI	109	159	17331	296
Array Multiplier-FSGDI	44	133	5852	260
Barun Multiplier-CMOS	48.5	133.5	6474.7	400
Barun Multiplier-GDI	78.9	189	14912	296
Barun Multiplier-FSGDI	38.5	230	8855	260
Baugh Wooley Multiplier-CMOS	55	160	8800	532
Baugh Wooley Multiplier-GDI	121	187	22627	382
Baugh Wooley Multiplier-FSGDI	47	145	6815	366

Table 5.2 Comparison of Multiplier's Implemented by Different Techniques

CHAPTER 6

CONCLUSION

An adder is one of the most important and fundamental unit in arithmetic operation which is used widely in any digital systems, such as digital signal processing (DSP) and microprocessor. 1-bit full adder is a building block of adder operation, used in the critical path of complex arithmetic for multiplication, division and so on. Therefore, reducing power consumption in full adders would reduce the overall power consumption of the whole system.

This work presents an 18T Full Adder designed in 65nm TSMC process using the Full-Swing GDI technique and simulated using the Cadence Virtuoso simulator. The computational Simulation results showed improvement in terms of power consumption, delay and transistor count while maintaining Full-Swing operation as compared to other approaches. It has been shown 35% improvement in energy for the proposed array multiplier, 34% improvement in energy for the proposed barn multiplier and 32 % improvement in energy for the proposed Baugh Wooley multiplier As compared to CMOS and reports better results than GDI multipliers in terms of power, delay, and energy. In future, this work will suitable to design filters for DSP applications.

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