

Glassless

Updated Report

11/22/2019

Updated Description:

The circuit we will create will simulate a lightsaber for exploratory purposes. The lightsaber will have ~~an ALU~~ **a way** to control the length of the lightsaber (in feet **meters**), the color of the lightsaber, and the power level of the lightsaber. ~~The circuit will also have a seven segment display to display the power remaining in the lightsaber.~~ The circuit will have other components to control the lightsaber's on and off state, configuration state including blade style, power up mode, and ~~color settings~~ **power draining and recharging.**

Updated Member Tasks List:

Giakhanh Hoang: ~~Draw the circuit and program verilog code for the seven segment power display and state configuration for the lightsaber.~~ **Combined and reformatted the power drain and recharge diagrams, blade mode, and color circuit diagram and verilog code.**

Brice May: ~~Draw the circuit and program verilog code for length of the lightsaber and color of the lightsaber, contain ways to take inputs from other parts of the code.~~ **Control unit and blade length circuit diagram and verilog code.**

Patrick Soisson: ~~Draw the circuit and program verilog code for lightsaber state (attack mode, defense mode, etc.), this will work with lightsaber length and color.~~ **Created the recharging diagram, made verilog code for the recharging module, and also worked on the report.**

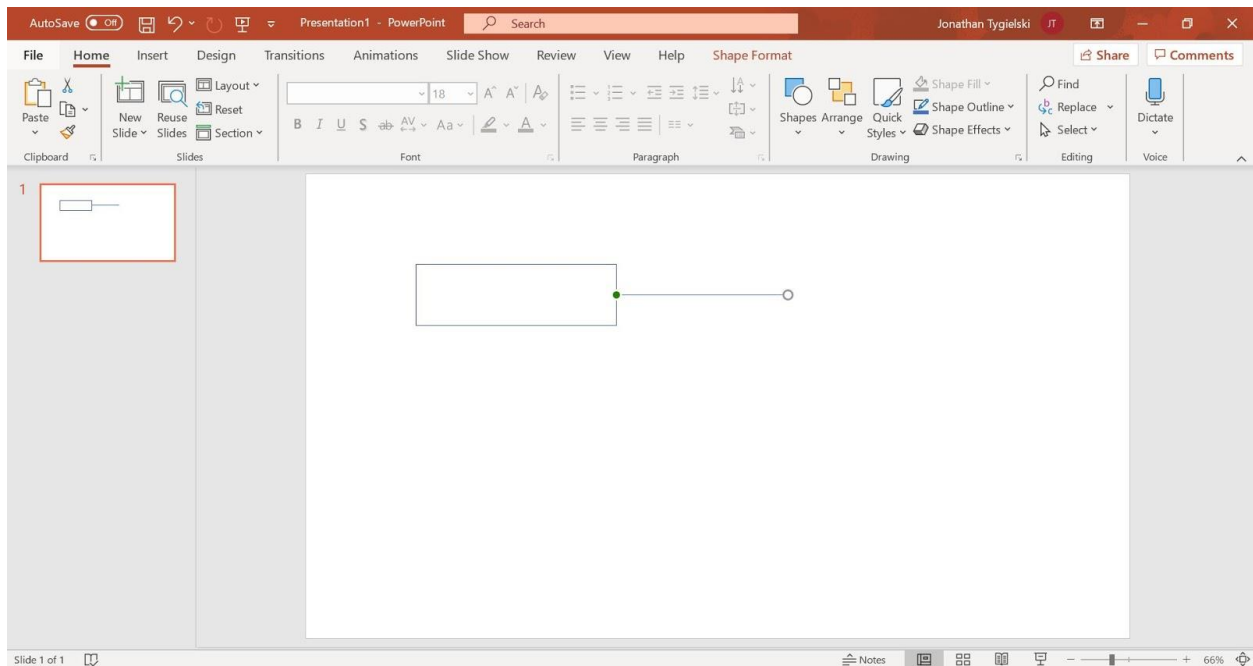
Nathan Stewart: ~~Draw the circuit and program verilog code for powering up the lightsaber with extra Kyber Crystals. Changes the power level of the lightsaber as well as size, however power drain increases.~~

Created the power draining diagram and helped work on the report.

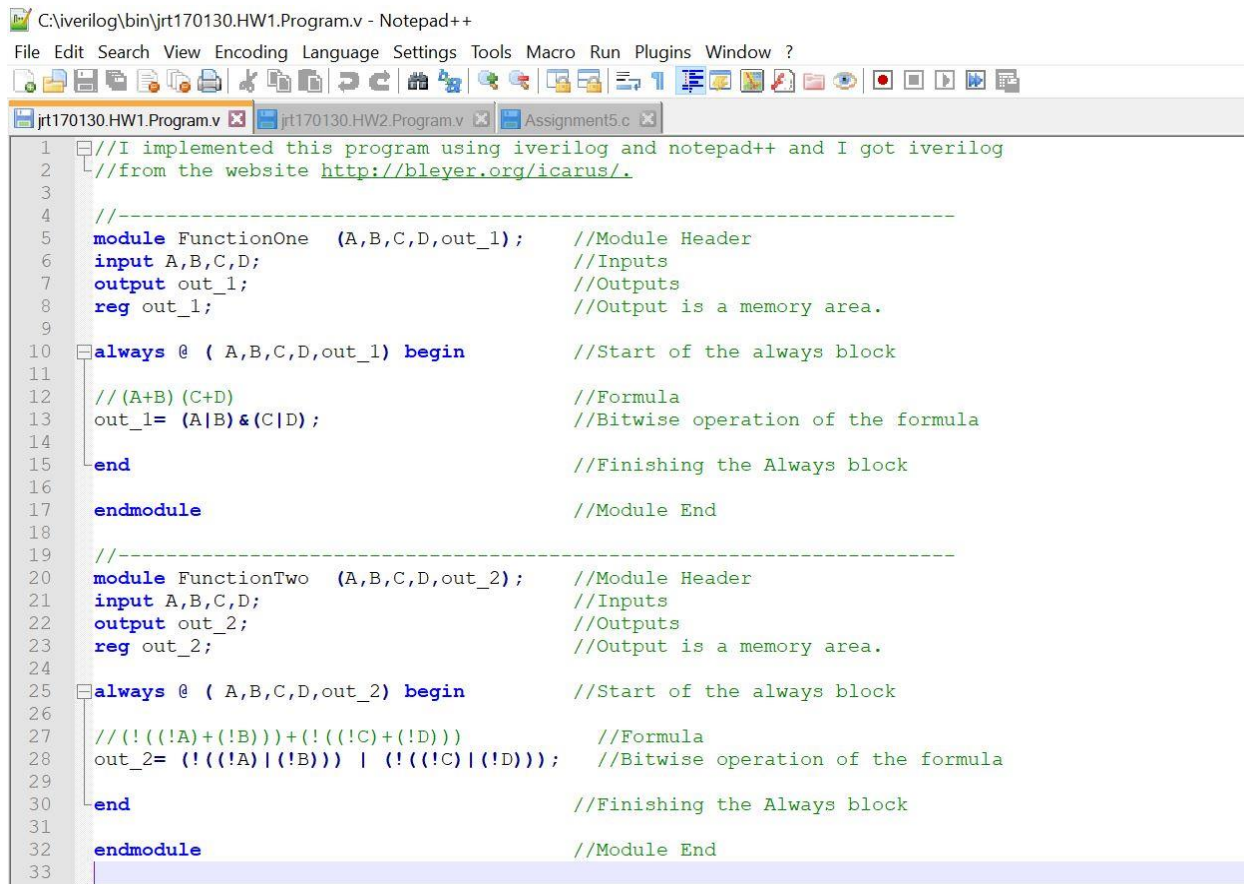
Jonathan Tygielski: ~~Draw the circuit and program verilog code for the seven segment power display for the lightsaber and state configuration of the lightsaber.~~ **Worked on the warning state in both the verilog and circuit diagrams. Also helped work on the final report.**

Updated Software Discovery:

We decided we will use Microsoft PowerPoint 2019 for our circuit drawing as it is available to us for free as students. PowerPoint provides intuitive design features such as snapping a line to the midpoint on a quadrilateral which helps create a neat circuit design. Furthermore, the powerpoint can be shared between members and updated live for everyone to see. This will make it easier to work together on the circuit design and check each other's work. We can also use individual slides to show a more detailed version of each part of the circuit. So we can focus on the logic for each part of the lightsaber. This makes it easier to divide up work between each other.



We will use Icarus Verilog version 11, August 9 2019 for Windows as our Hardware Design Language for simulating the circuit components for the lightsaber. Access to Professor Becker's sample code will make it easier to get a basic layout for our design. Also since we have been using it in class we have some background knowledge of how verilog code works.

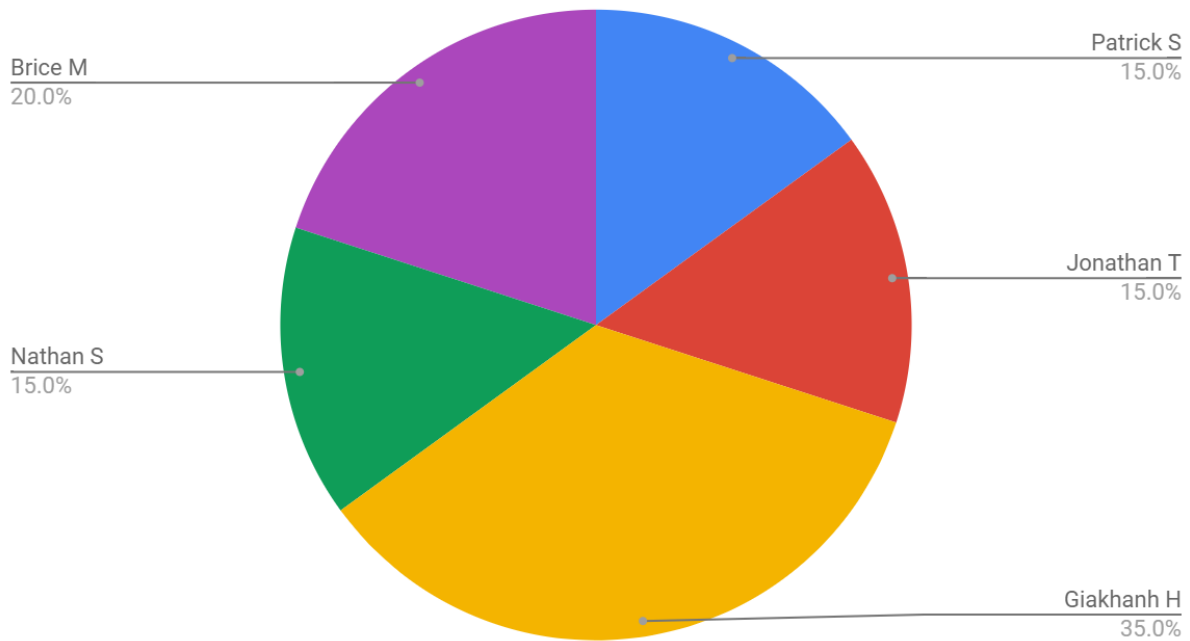


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C:\iverilog\bin\jrt170130.HW1.Program.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

jrt170130.HW1.Program.v jrt170130.HW2.Program.v Assignment5.c
1 //I implemented this program using iverilog and notepad++ and I got iverilog
2 //from the website http://bleyer.org/icarus/.
3
4 //-----
5 module FunctionOne (A,B,C,D,out_1); //Module Header
6 input A,B,C,D; //Inputs
7 output out_1; //Outputs
8 reg out_1; //Output is a memory area.
9
10 always @ ( A,B,C,D,out_1) begin //Start of the always block
11
12 // (A+B) (C+D) //Formula
13 out_1= (A|B)&(C|D); //Bitwise operation of the formula
14
15 end //Finishing the Always block
16
17 endmodule //Module End
18
19 //-----
20 module FunctionTwo (A,B,C,D,out_2); //Module Header
21 input A,B,C,D; //Inputs
22 output out_2; //Outputs
23 reg out_2; //Output is a memory area.
24
25 always @ ( A,B,C,D,out_2) begin //Start of the always block
26
27 //(!((!A)+(!B)))+(!((!C)+(!D))) //Formula
28 out_2= (!((!A)|(!B))) | (!((!C)|(!D))); //Bitwise operation of the formula
29
30 end //Finishing the Always block
31
32 endmodule //Module End
33
```

Updated Participation Census:

Participation



~~Everyone has kept up to date with the project and has contributed evenly.~~