

STUDENTS' SPACE ASSOCIATION
THE FACULTY OF POWER AND AERONAUTICAL ENGINEERING
WARSAW UNIVERSITY OF TECHNOLOGY



PRELIMINARY DESIGN REVIEW

ELECTRICAL POWER SYSTEM

Phase B of PW-Sat2 student satellite project

May 2015

Abstract

The following document is a part of the Preliminary Design Review – a paper describing the Phase B of student satellite project called PW-Sat2.

This document has been prepared by the EPS (Electrical Power System) team of the PW-Sat2 project.

Revisions

Date	Changes		Responsible
30.04.2015	First Issue of the document.		Piotr Kuligowski (team leader)
	The “Microcontroller selection” chapter added.		Grzegorz Gajoch
	The “Preliminary Radiation analysis” chapter added.	First version of the “Preliminary Radiation analysis” chapter.	Tomasz Mazewski
		First revision of the “Preliminary Radiation analysis”: - SPENVIS charts added, - New TID analysis added.	Piotr Kuligowski
	English correction.		Tom Rybarski (advisor)
23.05.2015	Small editorial changes.		Dominik Roszkowski

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

Table of contents

1	Introduction	12
2	Requirements for the system	13
2.1	Detailed requirements for the EPS	13
2.1.1	Possibility of connection of 4 solar panels	14
2.1.2	MPPT tracking	14
2.1.3	Energy storage.....	14
2.1.4	Redundancy of critical sections.....	15
2.1.5	Possibility of supplying subsystems directly from solar panels	15
2.1.6	Possibility of manually disconnection of accumulators using RBL.....	15
2.1.7	Deployment switch.....	16
2.1.8	Two controllers for redundancy	17
2.1.9	LCL for each subsystem.....	17
2.1.10	Creating voltages 3.3V, 5V and ACC	17
2.1.11	Required voltages for each subsystem	17
2.1.12	LCLs and voltages for subsystems	18
2.1.13	Summary supplied power by 3.3V, 5V and ACC lines.....	27
2.1.14	Execution of main task in spite of failure.....	28
2.1.15	Emergency disconnection when low battery.....	28
2.1.16	Running in space environment	28
2.1.17	Currents and voltages monitoring	29
2.1.18	Communication with OBC.....	29
2.2	Requirements for the PCB	29
2.2.1	Dimensions of the PCB	29
2.2.2	PCB design.....	31
2.2.3	PCB assembling and cleanroom facilities	31
2.2.4	PCB procurement	32
2.3	Electromagnetic compatibility.....	33
2.3.1	Line impedance stabilization network.....	33
2.3.2	Inrush current	34
2.3.3	Differential and common mode conducted emission	35
3	General System design	38
3.1	Solar panels	38
3.1.1	Availability of individual solar cells and assembled modules.....	38
3.1.2	Assembly method.....	40
3.1.3	Connections between the solar cells.....	40
3.1.4	The opening angle of the solar wings.....	42
3.2	MPPT topology	45

	PW-Sat2	Preliminary Design Review	 PW-SAT2
	2015-05-23		
	Phase B	Electrical Power System	

3.2.1	MPPT controlled DCDC converter	47
3.2.2	MPPT algorithm.....	49
3.3	Solar power summing.....	51
3.4	External power for pre-launch testing	51
3.5	Main power bus	52
3.6	Energy storage	53
3.6.1	Charging and discharging cycles during the mission	56
3.6.2	Extending li-ion battery life	56
3.6.3	Charging method.....	57
3.6.4	Charging and discharging controllers.....	58
3.7	Input filter design for DCDC converters	59
3.7.1	Stability problem of DCDC converters due to input filters	61
3.8	Frequency response of the regulation loops.....	61
3.9	The RBL circuit.....	62
3.9.1	Inrush-current limiters for the RBL and the deployment switches.....	64
3.10	The deployment switch.....	65
3.11	The Access Port	65
3.12	DCDC converters for 3.3V and 5V lines.....	66
3.13	Grounding scheme	67
4	Preliminary radiation analysis	68
4.1	General background.....	68
4.2	Radiation effects on electronics	68
4.3	South Atlantic Anomaly	68
4.4	Absorbed TID level calculation	71
4.5	Methods of protection from radiation effects	71
5	Components selection	73
5.1	Low power and thin film SMD Resistors	73
5.2	SMD ceramic capacitors.....	74
5.3	Solid tantalum SMD capacitors	74
5.4	Ideal diode controller.....	75
5.4.1	Requirements for ideal diode controller	75
5.4.2	Ideal diode controller selection	76
5.4.3	MOSFET for ideal diode controller	76
5.5	Boost converter.....	78
5.6	Buck-boost converters	80
5.7	DCDC converters for 3V3 and 5V lines	81
5.8	LCL for ACC and 5V lines.....	83
5.9	LCL for 3V3 and 5V lines – low current applications.....	84
5.10	High-side current-sense amplifier.....	85

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.11	Small LDO regulator	86
5.12	Reset supervisors	88
5.13	Reset supervisors with watchdog.....	89
5.14	Small power Schottky rectifier diode	90
5.15	General purpose ADC converter	91
5.16	DAC converter for MPPT.....	93
5.17	Microcontroller selection.....	94
5.17.1	Requirements.....	94
5.17.2	Part selection	95
5.17.3	Radiation effect analysis in ATMega	97
5.17.4	ATMega selection conclusion	99
5.17.5	Programming ATMega microcontroller.....	99
6	Final block diagram of the system	100
6.1	Power Summing CH0, CH1, CH2	100
6.2	CM Filters.....	102
6.3	Measurements CH0	102
6.4	MPPT boost converter	103
6.5	MPPT buck-boost converters	103
6.6	Controllers	104
6.7	The MPB bus.....	105
6.8	The distribution module.....	106
7	Development schedule	107
8	Appendix A	108

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

Abbreviated terms

2U	2-Unit
ACC	ACC power bus
ADC	Analogue-to-Digital Converter
ADCS	Attitude Determination and Control System
CAM	Cameras
CAN	Controller Area Network – CAN bus
CC-CV	Constant Current – Constant Voltage
COMM	Communication System
COTS	Commercial off-the-shelf
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analogue Converter
DCDC	DC-to-DC converter. It converts one voltage level to another
DoD	Depth of Discharge factor
DT	Deployment Team
ECC	Error-Correcting Code
ECSS	European Cooperation for Space Standardization
EGSE	Electrical Ground Support Equipment
EM	Engineering Model
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interferences
EPS	Electrical Power System
ESA	European Space Agency
ESD	Electrostatic Discharge
FBK	Feedback
FDIR	Fault Detection, Isolation and Recovery
FM	Flight Model
FRAM	Ferroelectric Random-Access Memory
GND	Ground - the reference point in an electrical circuit
GS	Ground Station
I ² C	Inter-Integrated Circuit bus
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
ISP	In-system programming
JAXA	Japan Aerospace Exploration Agency
JTAG	Joint Test Action Group - IC debug port
LCL	Latch-up Current Limiter
LDO	Low-Drop-Out regulator
LEO	Low Earth Orbit
LET	Linear Energy Transfer Threshold
LISN	Line Impedance Stabilization Network
LPF	Low Pass Filter
MA	Mission Analysis
MBS	Main Power Bus

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

MLI	Multi-Layer Insulation
MP	Military Plastic grade (Linear Technology)
MPB	Main Power Bus
MPPT	Maximum Power Point Tracking
NASA	National Aeronautics and Space Administration
NC	Normal Closed (a contact of a switch)
NO	Normal Open (a contact of a switch)
OBC	On-board Computer
P&O	Perturb & Observe algorithm is used for maximum point tracking in PV systems
PCB	Printed Circuit Board
PE	Local earthing system
PFM	Proto-flight Model
PLD	Payload PCB
PSA	Parts Stress Analysis
PWM	Pulse Width Modulation
QM	Qualification Model
RAM	Random-Access Memory
RBL	Remove Before Launch
RLC	Resistor-inductor-capacitor circuit
SAA	South Atlantic Anomaly
SADS	Solar Array Deployment System
SEE	Single Event Effects
SEL	Single Event Latch-up
SEU	Single Event Upset
SKA	Students' Space Association (pl. Studenckie Koło Astronautyczne)
SoC	State of Charge
SP	Solar Panel
SPDT	Single Pole Double Throw – it is a kind of switch
SPG	Single Point Grounding
SPI	Serial Peripheral Interface bus
SRAM	Static Random Access Memory
SSO	Sun-Synchronous Orbit
SunS	Sun Sensor as main payload
TCS	Thermal Control System
TID	Total Ionization Dose
UVLO	Under-Voltage Lockout circuit
WCA	Worst Case Analysis

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

List of figures

Figure 2-1. Functional block diagram of the system	13
Figure 2-2. An example of the RBF – KySat1 from Kentucky Space	15
Figure 2-3. Placement for deployment switches – source [3]	16
Figure 2-4. Deployment switch - surce TISAT-1	16
Figure 2-5. ISIS UHF downlink / VHF uplink Full Duplex Transceiver module	18
Figure 2-6. Electrical characteristics of the COMM1 module	19
Figure 2-7. LCL lines for the COMM1 module	19
Figure 2-8. Pin-out of the COMM1	19
Figure 2-9. ISIS deployable UHF/VHF antennas module	20
Figure 2-10. Selected ADCS module	21
Figure 2-11. Pin-out of the ADCS module	22
Figure 2-12. Pin-out of the Payload module	24
Figure 2-13. The OBC module from the Createch Instruments company	26
Figure 2-14. Pin-out of the OBC module	26
Figure 2-15. Top and side view of the PCB	30
Figure 2-16. Bottom view of the PCB	30
Figure 2-17. 3G Flex EPS from the ClydeSpace company	31
Figure 2-18. Cleanroom facilities at Createch Instruments S.A.	32
Figure 2-19. LISN schematic – source [11]	34
Figure 2-20. LISN impedance – source [11]	34
Figure 2-21. Inrush current: measurement setup – 5.4.4 from [10]	35
Figure 2-22. Common mode conducted emissions – measurement setup	36
Figure 2-23. Differential mode conducted emission – measurement setup	36
Figure 2-24. Common mode conducted emission limit – source [10]	37
Figure 2-25. Differential mode conducted emission limit – source [10]	37
Figure 3-1. Solar cell from AzurSpace company - AzurSpace website	38
Figure 3-2. Assembled solar module from GOMSpace company - GOMSpace website	39
Figure 3-3. PT1000 temp. sensor, vacuum sputtered onto a ceramic substrate- TME.eu website	40
Figure 3-4. Internal connections inthe SP3 Y- (when closed) single-side solar wing	40
Figure 3-5. When the opening angle of the solar wings is equal to 90 deg	43
Figure 3-6. Opening angle of the solar wings calculations – axis definition	43
Figure 3-7. The harvested power when the opening angle is equal to 90 deg	44

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Figure 3-8. The harvested power when the opening angle is equal to 60 deg	45
Figure 3-9. Battery charge and discharge options in PPT architecture, [12]page 77	46
Figure 3-10. Simple scheme of the MPPT, including charging and discharging control	46
Figure 3-11. Controlled DCDC converter with MPPT	49
Figure 3-12. Perturb and Observe algorithm – [13] page 4	50
Figure 3-13. Incremental Conductance algorithm – [13] page 5	50
Figure 3-14. Summing of the solar power	51
Figure 3-15. External supply	52
Figure 3-16. Main Power Bus	52
Figure 3-17. Special connections of the capacitors on the MPB	53
Figure 3-18. NanoPower BP4 from GOMSpace company	53
Figure 3-19. Discharge characteristics of the 3.7V 2600mAh cell – GOMSpace specification	54
Figure 3-20. Charge characteristics of the 3.7V 2600mAh cell – GOMSpace specification	55
Figure 3-21. Charging and discharging paths	58
Figure 3-22. Charging and discharging controllers design	59
Figure 3-23. Parallel damped input filter – source [17]	60
Figure 3-24. Series damped input filter – source [17]	60
Figure 3-25. Separation of impedances – source [17]	61
Figure 3-26. Stability test of the regulation loop	62
Figure 3-27. The RBL as the inrush-current limiter for the deployment switch	62
Figure 3-28. The RBL for the battery pack	63
Figure 3-29. The RBL switch - Saia-Burgess F4T7Y1 - source TME.eu	63
Figure 3-30. Remove Before Launch label	64
Figure 3-31. The RBL circuit	64
Figure 3-32. The deployment switch - Saia-Burgess F4T7Y1 - source TME.eu SPDT	65
Figure 3-33. Harwin M80-8411242 for pre-launch testing	65
Figure 3-34. Block diagram of the Access Port	66
Figure 3-35. DCDC 5V and 3V3 topology	66
Figure 4-1. Trapped protons flux above 1MeV on 700km SSO orbit– SPENVIS software from ESA	69
Figure 4-2. Trapped electrons flux above 1MeV on 700km SSO orbit – SPENVIS software from ESA	69
Figure 4-3. Averaged spectra of trapped protons on 700km SSO orbit – SPENVIS software from ESA	70
Figure 4-4. Averaged spectra of trapped electrons on 700km SSO orbit – SPENVIS software from ESA	70
Figure 4-5. Radiation dose as a function of shielding thickness for the PW-Sat2 mission	71
Figure 5-1. LTC4412 from Linear Technology - typical application	76

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Figure 5-2. Vth relative variation of the IRF7416 – source [19]	77
Figure 5-3. Rds relative variation of the IRF7416 – source [19]	78
Figure 5-4. LT3580 converter from Linear Technology - typical application	79
Figure 5-5. LTC3115 converter from Linear Technology - typical application	81
Figure 5-6. TPS5430 from Texas Instruments - simplified schematic	82
Figure 5-7. Radiation analysis for the TPS5420 – source [22]	82
Figure 5-8. FPF270xMX from Fairchild Semiconductor – typical application	83
Figure 5-9. Radiation analysis of the FPF2700 – IEEE [23]	84
Figure 5-10. TPS2551 from Texas Instruments - typical application	85
Figure 5-11. MAX4372 from Maxim - typical application	86
Figure 5-12. Summary of radiation tests of MAX4372 – source [24]	86
Figure 5-13. LT1761 from Linear Technology - typical application	87
Figure 5-14. TPS3836 from Texas Instruments - typical application	88
Figure 5-15. ADC128S022 from Texas Instruments - block diagram	92
Figure 5-16. ADC124S021 from Texas Instruments - block diagram	92
Figure 5-17. DAC121S101 from Texas Instruments - typical application	94
Figure 5-18. SEE in 2048 bytes of SRAM – source [30]	98
Figure 6-1. Block diagram - Power Summing CH0	100
Figure 6-2. Block diagram - Power Summing CH1	101
Figure 6-3. Block diagram - Power Summing CH2	101
Figure 6-4. Block diagram - Temp. Sensor Interface	101
Figure 6-5. Block diagram - CM Filter CH0 A	102
Figure 6-6. Block diagram - Measurements CH0	102
Figure 6-7. Block diagram - MPPT boost converter	103
Figure 6-8. Block diagram - MPPT CH2	104
Figure 6-9. Block diagram - Controller CH1	104
Figure 6-10. Block diagram - Controller CH2	105
Figure 6-11. Block diagram - the MPB bus	105

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

List of tables

Table 2-1. Required voltages for each subsystem	18
Table 2-2. Electrical characteristics of the ANT1 module	20
Table 2-3. LCL lines for the ANT1 module	21
Table 2-4. Electrical characteristics of the ADCS module	22
Table 2-5. LCL lines for the ADCS module	23
Table 2-6. Electrical characteristics of the Payload module	24
Table 2-7. LCL lines for the PLD module	25
Table 2-8. Electrical characteristics of the OBC	26
Table 2-9. LCL lines for the OBC module	27
Table 2-10. Power consumption on 3.3V, 5V and ACC lines for each subsystem	28
Table 2-11. Summary power consumption on 3.3V, 5V and ACC lines	28
Table 2-12. PCB stack layers from the Techno Service company	33
Table 3-1. Solar cells – offers from providers when order of 30 pieces	38
Table 3-2. Currently offers for assembled modules	39
Table 3-3. Parameters of solar panels for SP3 Y- and SP1 Y+	41
Table 3-4. Parameters of solar panels for SP5 X- and SP2 X+	42
Table 3-5. Requirements for MPPT controlled DC/DC converters	47
Table 3-6. Ready-made DC/DC converters, which implements the MPPT algorithms	48
Table 3-7. Configurations of the accumulators for NanoPower BP4	54
Table 3-8. Specification of the NanoPower BP4 pack	55
Table 3-9. Cycle life vs DoD – BU-808 from [16]	57
Table 3-10. Cycle life vs charge voltage level – BU-808 from [16]	57
Table 3-11. Requirements for charging controller	58
Table 3-12. Requirements for discharging controller	59
Table 5-1. CRCW series resistors from Vishay company	73
Table 5-2. CRCW resistors from Vishay - part numbers	74
Table 5-3. KEMET COTS ceramic capacitors - ordering information	74
Table 5-4. Solid tantalum COTS capacitors from Vishay – ordering information	75
Table 5-5. Parameters of the IRF7416 from datasheet – International Rectifier company	77
Table 5-6. Requirements for boost converter	79
Table 5-7. Requirements for buck-boost converters	80
Table 5-8. Requirements for DCDC converters for 3V3 and 5V lines	82

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Table 5-9. Requirements for high-side current-sense amplifiers	85
Table 5-10. Requirements for LDO regulator	87
Table 5-11. Requirements for reset supervisors	88
Table 5-12. Requirements for reset supervisors with watchdog	89
Table 5-13. TPS3813 from Texas Instruments - typical application	89
Table 5-14. Requirements for Schottky rectifier diodes	90
Table 5-15. STPS340 from STMicroelectronics - absolute ratings	90
Table 5-16. Requirements for external ADC converters	91
Table 5-17. Requirements for DAC converters	93
Table 5-18. An example of ATMega part code	95
Table 5-19. ATMEGA164P-B15AZ – automotive series	96
Table 5-20. ATMega16 review	96
Table 5-21. ATMega164 review	96
Table 5-22. ATMega168 review	96
Table 6-1. Block diagram – MPPT CH0 boost converter - ICs	103
Table 6-2. Block diagram – MPPT CH2 boost converter - ICs	104
Table 7-1. Development schedule	107

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

1 INTRODUCTION

Electrical Power System is responsible for power conversion from solar panels, energy storage in battery and power distribution to other subsystems. It is designed and it will be built by the EPS team of the PW-Sat2 project.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

2 REQUIREMENTS FOR THE SYSTEM

The EPS shall be designed to consist of the following functions: power harvesting, energy storage, power conditioning and distribution. Functional block diagram of the system:

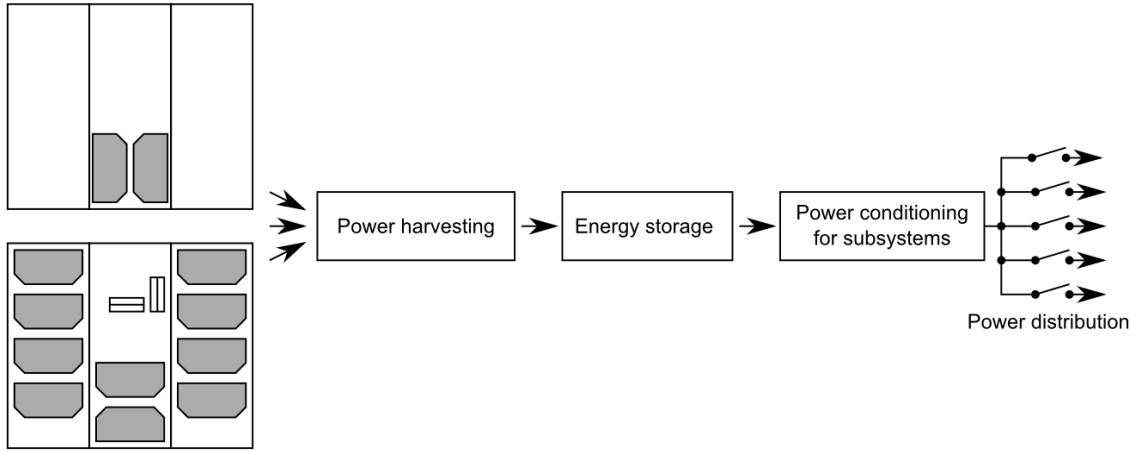


Figure 2-1. Functional block diagram of the system

To generate electrical power from sunlight, we will use 12 pieces of space qualified triple-junction solar cells. And then the electrical power shall be harvested by a corresponding circuit. To store energy a lithium-ion battery will be used.

Some subsystems need regulated and protected lines. It is 3.3V and 5V lines. Unregulated lines shall also be protected.

The system should be as reliable as possible and simultaneously low cost is required. To meet these requirements the COTS components and redundancy of critical sub-circuits will be used. Some electronic components should be examined for radiation.

2.1 DETAILED REQUIREMENTS FOR THE EPS

The following chapter contains detailed requirements for the EPS.

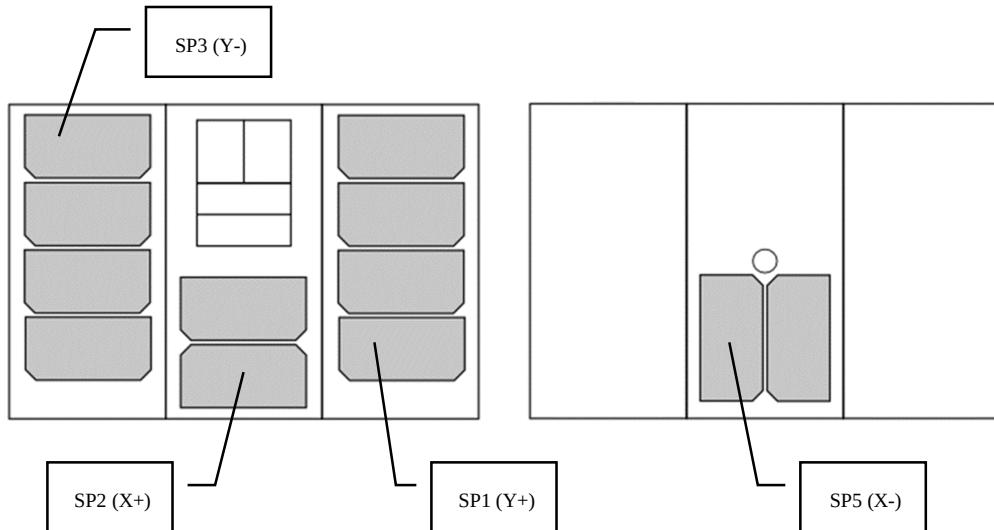
The requirements are expressed in conformance with 8.3.2 in [1]. For example verbal form “shall” will be used whenever a provision is a requirement. Next, the verbal form “should” will be used whenever a provision is a recommendation. The verbal form “may” will be used whenever a provision is a permission. The verbal form “can” will be used to indicate possibility or capability.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Restricted formats from 8.3.3 in [1] are not used in this document.

2.1.1 POSSIBILITY OF CONNECTION OF 4 SOLAR PANELS

Location of solar panels is shown on pictures below:



During phase A double-side solar wings were selected. During phase B, because of high costs the double-side solar panels are rejected. For the sake of order, old numbering is respected.

On every surface the solar cells are connected in series. There will be 3-junction cells with efficiency about 30%. Maximal theoretical power from each of the cells is 1W-1.2W. Maximal power of 1 panel containing 4 cells is around 4W. Maximal voltage on a panel, containing 4 cells is about 10V. Maximal current is 0.5A per each panel. We expect 2 panels containing 4 cells each (wings) and 2 panels containing 2 cells each.

2.1.2 MPPT TRACKING

To increase efficiency of solar power conversion the MPPT algorithms are required. The main idea is: one MPPT channel per one solar panel. To achieve high efficiency DCDC converters shall be used. In one moment only 3 surfaces can be lightened up, so one can limit the number of pulse converters to 3. To every one of them shall be connected opposite-sided panels.

2.1.3 ENERGY STORAGE

Possibility of energy storage in a battery pack. It shall be assembled with li-ion cells. To achieve high reliability the battery pack shall be ordered from a space company.

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

We cannot design the battery pack. We must adapt our power budget to the ordered battery.

2.1.4 REDUNDANCY OF CRITICAL SECTIONS

Redundancy of basic, critical sections of the power system. For example: charger modules or redundant pulse converters for supplying different subsystems. We decided to use one battery pack. There is no redundancy of the battery pack.

There are three kinds of redundancy: cold, warm and hot. The right kind of redundancy shall be selected. Some proper reliability practices are described in NASA's documents (for example [2]).

2.1.5 POSSIBILITY OF SUPPLYING SUBSYSTEMS DIRECTLY FROM SOLAR PANELS

Possibility of supplying subsystems directly from solar panels is required. There must be such a solution, because it will allow executing the mission even if the accumulators were damaged. But if the accumulators will be damaged, then executing the mission during eclipse is not possible.

If damage of the accumulators is detected, a special procedure will be executed. This special procedure is planned.

2.1.6 POSSIBILITY OF MANUALLY DISCONNECTION OF ACCUMULATORS USING RBL

Possibility of manually disconnection of accumulators using RBL (also called RBF – Remove Before Flight) according to 2.3.4 of [3]. The RBL will be switched-on close to the launch of the rocket.

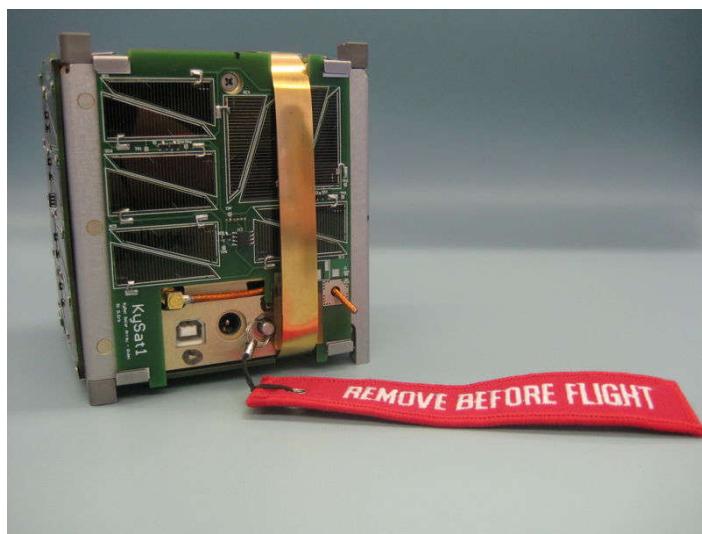


Figure 2-2. An example of the RBF – KySat1 from Kentucky Space

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

2.1.7 DEPLOYMENT SWITCH

The EPS shall include at least one deployment switch (also called kill-switch or separation-switch) according to 2.3.2 of [3]. Batteries shall be fully deactivated during launch or launch with discharged batteries according to 2.3 of [3]. The deployment switch will be switched-on immediately after separation from the rocket.

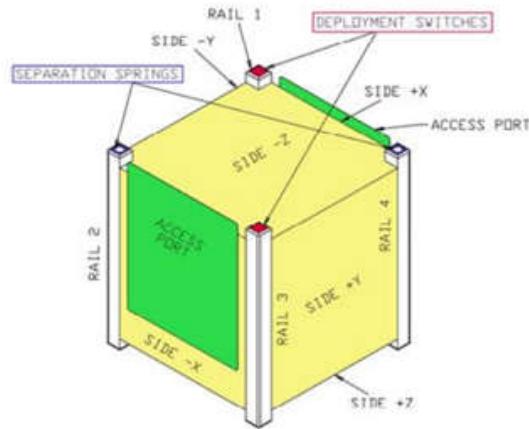


Figure 2-3. Placement for deployment switches – source [3]

We will use two deployment switches for redundancy. The switches will be placed on rails of the PW-Sat2 satellite. An example of the deployment switch:

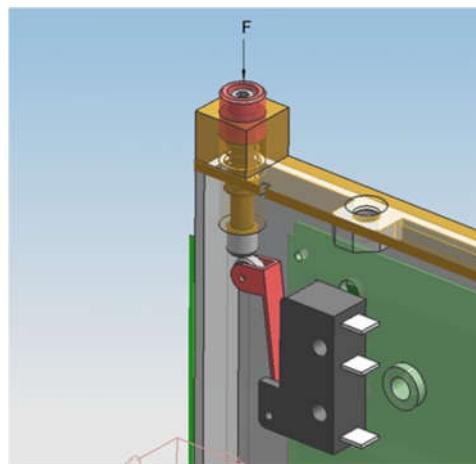


Figure 2-4. Deployment switch - source TISAT-1

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

2.1.8 TWO CONTROLLERS FOR REDUNDANCY

The EPS shall contain two redundant controllers. Each one can turn on or turn off all subsystems. If one of them is broken (any kind of failure), the mission cannot be compromised.

2.1.9 LCL FOR EACH SUBSYSTEM

Possibility of supply disconnection for every subsystem will allow saving more energy. Keys (electronic switches) turning on supply voltage shall be located on buses 3.3, 5V and 6.5-9V. Every one of them shall have over-current protection (also named LCL – Latch-Up Current Limiter) and has to be controlled from OBC. Communication module COMM1 and OBC may be disconnected only when an emergency situation appears, so they have to have their own hardware protection.

2.1.10 CREATING VOLTAGES 3.3V, 5V AND ACC

Creating voltages 3.3V, 5V and possibility for supplying directly from accumulator package (ACC line). All the power lines shall be protected by an LCL.

2.1.11 REQUIRED VOLTAGES FOR EACH SUBSYSTEM

Required voltages for each subsystem are listed below:

No.	Abbreviation	Full name	Switches
1	COMM1	ISIS UHF downlink / VHF uplink Full Duplex Transceiver	2x ACC
2	ANT1	Deployable UHF and VHF antennas from ISIS company	2x 5V (redundancy)
3	BATTERY	Accumulator package - NanoPower BP4 from GOMSpace company	2x ACC (for heaters supply)
4	EPS	Electrical Power System	Internal
5	ADCS	Attitude Determination and Control System - ISIS Magnetorquer Board (iMTQ)	Actuators: 1x 5 V Sensors and electronics: 1x 3.3V
6	PLD	Payload electronics	SunS: 1x 5V
			Photodiodes: 1x 5V
			TCS: 1x ACC

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

			Magnetometers: 1x 3.3V
			Sail: 2x ACC (redundancy)
			SADS: 2x ACC (redundancy)
7	OBC	On-board Computer from Creotech Instruments S.A.	2x ACC (redundancy)

Table 2-1. Required voltages for each subsystem

2.1.12 LCL'S AND VOLTAGES FOR SUBSYSTEMS

All required voltages and LCL's for each subsystems are presented below.

2.1.12.1 Selected COMM1 module

UHF downlink / VHF uplink Full Duplex Transceiver module from ISIS company was selected.



Figure 2-5. ISIS UHF downlink / VHF uplink Full Duplex Transceiver module

All the necessary data from the ICD document and the Option Sheet document of the module are shown below:

Parameter	Value	Notes
Supply voltage	6.0 – 18V (ACC line)	DC from a PC-104 connector
Supply max current (at 7V)	65mA (0.5W)	Receiver only
Supply max current (at 7V)	310mA (2.2W)	Receiver and Transmitter

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Figure 2-6. Electrical characteristics of the COMM1 module

The COMM1 module will be connected to the ACC line. It is an unregulated supply line. The LCL protection should be set up on 0.6A, but on the same line the heater of the Battery Pack module is connected. The heater consumes about 3W, when it is turned-on and consumes 0W, when it is turned-off. Consequently the LCL protection should be set up on 1.5A.

LCL's ID	Line	Current	Notes
LCL_COMM1_0	ACC line	1.5A	<p>The LCL supplies both COMM1 module and heaters in the battery pack.</p> <p>Connected to the PC-104 connector – H2.46 and H2.45.</p> <p>Return lines: H2.29, H2.30 and H2.32.</p>
LCL_COMM1_1	ACC line	1.5A	Parallel connection to the LCL-COMM1-0. It is a redundant LCL.

Figure 2-7. LCL lines for the COMM1 module



Figure 2-8. Pin-out of the COMM1

The pins H1.41, H1.43, H1.44 and H2.50 are not used and they are disconnected.

2.1.12.2 Selected ANT1 module

Deployable UHF and VHF antenna module from ISIS company was selected:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

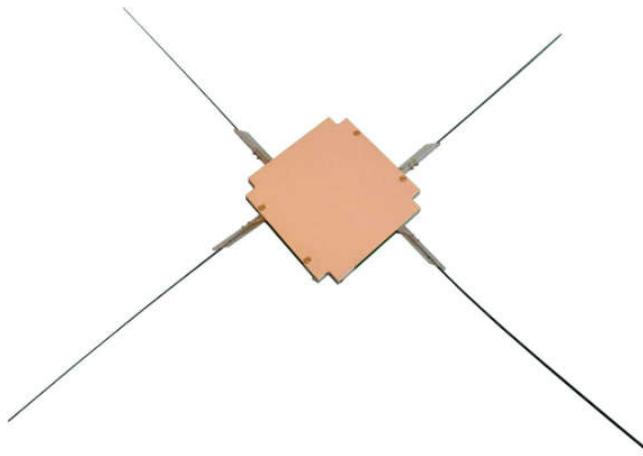


Figure 2-9. ISIS deployable UHF/VHF antennas module

All the necessary data from the ICD document and the Option Sheet document of the module are shown below:

Parameter	Value	Notes
Supply voltage	5V	DC from a miniature 9 pin OMNETICS connector
Power consumption during deployment	2W	max 20s at -40°C
Power consumption at nominal mode	<20mW	But the supply will be cutted-off-

Table 2-2. Electrical characteristics of the ANT1 module

LCL's ID	Line	Current	Notes
LCL_ANT1_0	5V line	1 A	Connected to the miniature 9 pin OMNETICS connector
LCL_ANT1_1	5V line	1 A	Connected to the miniature 9 pin OMNETICS connector. It is a redundant LCL.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Table 2-3. LCL lines for the ANT1 module

The miniature 9-pin OMNETICS connector shall be placed on the EPS board. The connector consists two I2C buses (redundant) and power lines. One of the I2C buses should be connected to a first controller of the EPS, but the second I2C bus should be connected to a second controller of the EPS. ANT1 module is turning on by the EPS after 30 min from separation from the P-POD. Then the OBC module will send a deployment command. After deployment, the ANT1 module will be turned off. The ANT1 module can be turned off by an LCL, because it has built-in I2C repeaters. They can prevent to block the I2C buses.

2.1.12.3 Selected battery pack

It will be selected in the next chapter.

2.1.12.4 Selected ADCS module

ISIS Magnetorquer Board (iMTQ) module was selected.

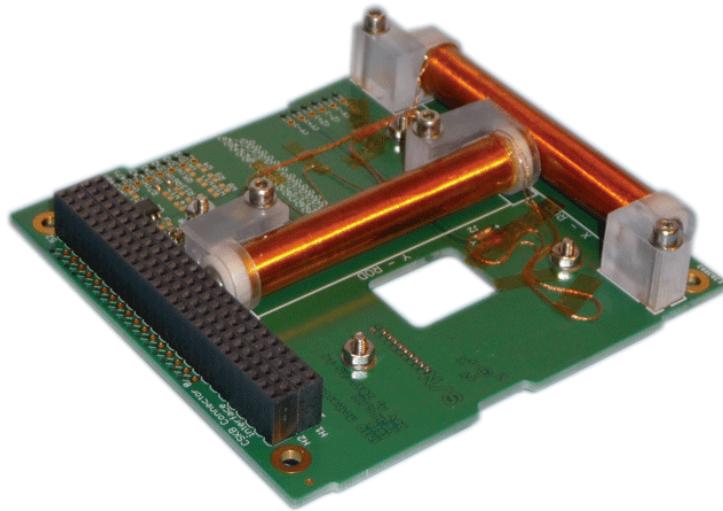


Figure 2-10. Selected ADCS module

All the necessary data from the ICD document and the Option Sheet document of the module are shown below:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Parameter	Value	Notes
Supply voltage for actuation (the module with a PWM driver was selected)	5V	Special option, which selected in the Option Sheet
Supply voltage for sensors and electronics	3.3V	-
Power consumption for actuation	Max 1W at detumbling mode	Predicted value. It can be changed.
Power consumption for sensors and electronics	Max 0.2W at detumbling mode	Predicted value. It can be changed.

Table 2-4. Electrical characteristics of the ADCS module

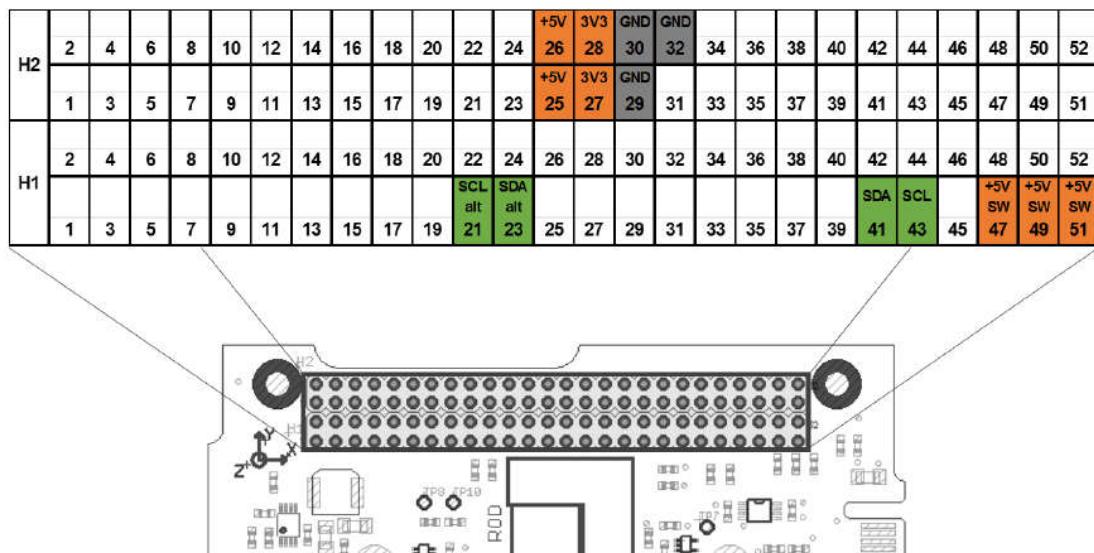


Figure 2-11. Pin-out of the ADCS module

The pins H1.41, H1.43, H1.47, H1.49 and H1.51 are not used and they are not connected.

LCL's ID	Line	Current	Notes
LCL_ADCS_0	5V line	0.5A	Connected to the PC-104 connector – pins

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

			H2.25 and H2.26. Return lines: H2.29, H2.30 and H2.32.
LCL_ADCS_1	3.3V line	0.2 A	Connected to the PC-104 connector – pins H2.27 and H2.28. Return lines: H2.29, H2.30 and H2.32.

Table 2-5. LCL lines for the ADCS module

2.1.12.5 Payload module

The payload module will be designed by the PW-Sat2 Team. It will consist of the SunS module, the TCS module, the photodiodes module, the TID meter module (designed by a part of team from Cracow) and the additional magnetometers module.

Parameter	Value	Notes
Supply voltage for the SunS	5V	-
Supply voltage for Photodiodes	5V	-
Supply voltage for TCS	ACC	-
Supply voltage for an additional magnetometer	3.3V	-
Supply voltage for Sail	ACC	-
Supply voltage for SADS	ACC	-
Power consumption for the SunS	1W	Predicted value (it can be lower than present)
Power consumption for Photodiodes	0.2W	Predicted value (it can be lower than present)
Power consumption for TCS	Max 3W	Predicted peak value
Power consumption for an additional magnetometer	0.2W	Predicted value (it can be lower than present)

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Power consumption for Sail	2W	Max 30s at -40°C. Predicted value. It can be changed.
Power consumption for SADS	2W	Max 30s at -40°C. Predicted value. It can be changed.

Table 2-6. Electrical characteristics of the Payload module

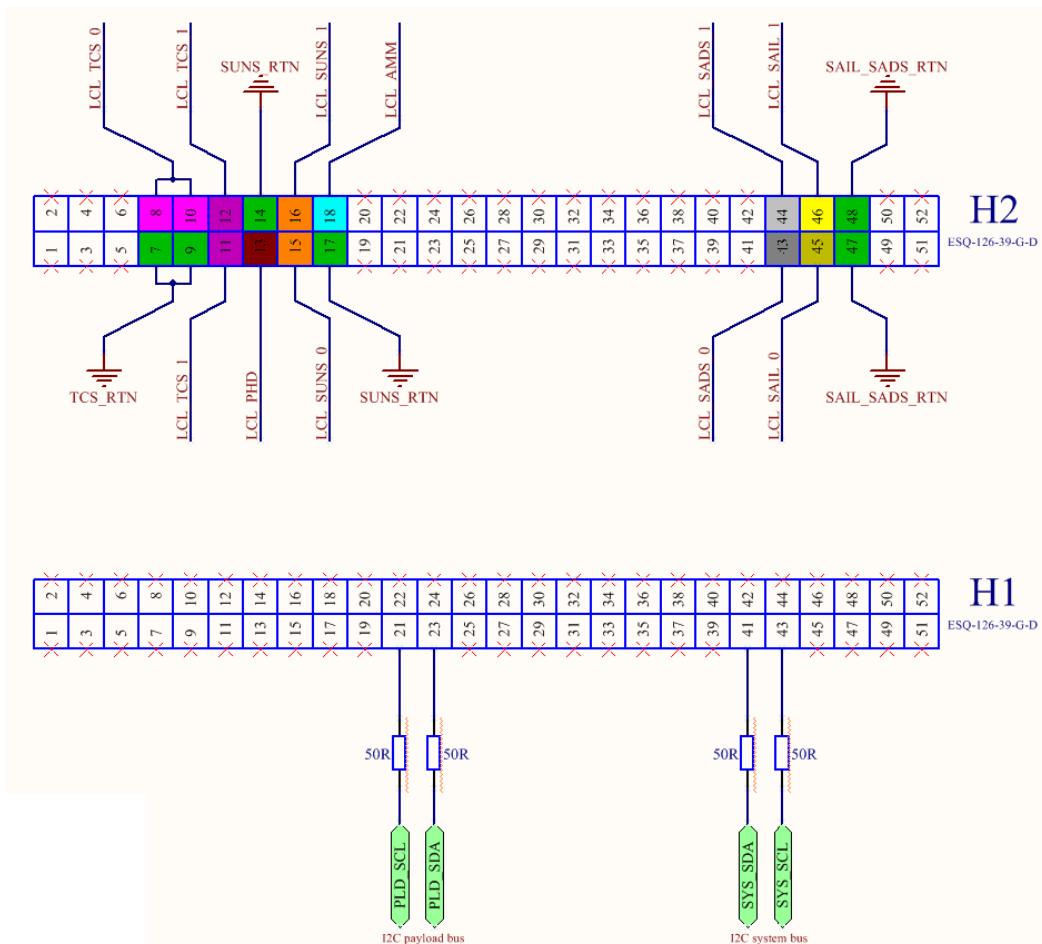


Figure 2-12. Pin-out of the Payload module

LCL's ID	Line	Current	Notes
LCL_SUNS_0	5V line	0.5A	5V line: H2.15

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

			Return lines: H2.14 and H2.17
LCL_SUNS_1	5V line	0.5A	5V line: H2.16 Return lines: H2.14 and H2.17
LCL_PHD	3.3V line	0.2A	3.3V line: H2.13 Return lines: H2.14 and H2.17
LCL_TCS_0	ACC line	1.5A	ACC line: H2.8 and H2.10 Return lines: H2.7 and H2.9
LCL_TCS_1	ACC line	1.5A	ACC line: H2.11 and H2.12 Return lines: H2.7 and H2.9
LCL_AMM	3.3V line	0.2A	3.3V line: H2.18 Return lines: H2.14 and H2.17
LCL_SAIL_0	ACC line	1A	ACC line: H2.45 Return lines: H2.47 and H2.48
LCL_SAIL_1	ACC line	1A	ACC line: H2.46 Return lines: H2.47 and H2.48
LCL_SADS_0	ACC line	1A	ACC line: H2.43 Return lines: H2.47 and H2.48
LCL_SADS_1	ACC line	1A	ACC line: H2.44 Return lines: H2.47 and H2.48

Table 2-7. LCL lines for the PLD module

On the PLD module both an access port, a Sail connector and a SADS connector are placed.

2.1.12.6 OBC module

The OBC module is designed by the Createch Instruments S.A. company. It will be supplied by the redundant ACC line (the redundancy will be placed in the EPS).

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

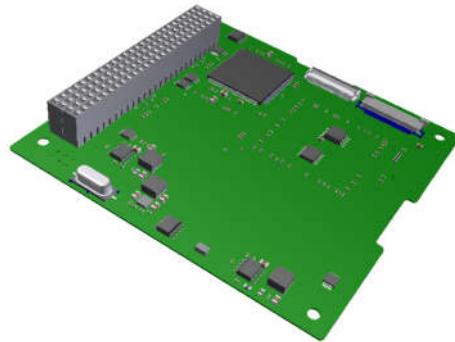


Figure 2-13. The OBC module from the Creotech Instruments company

Parameter	Value	Notes
Supply voltage	5.5-9V	-
Power consumption	2W	Predicted peak value (can be changed)

Table 2-8. Electrical characteristics of the OBC

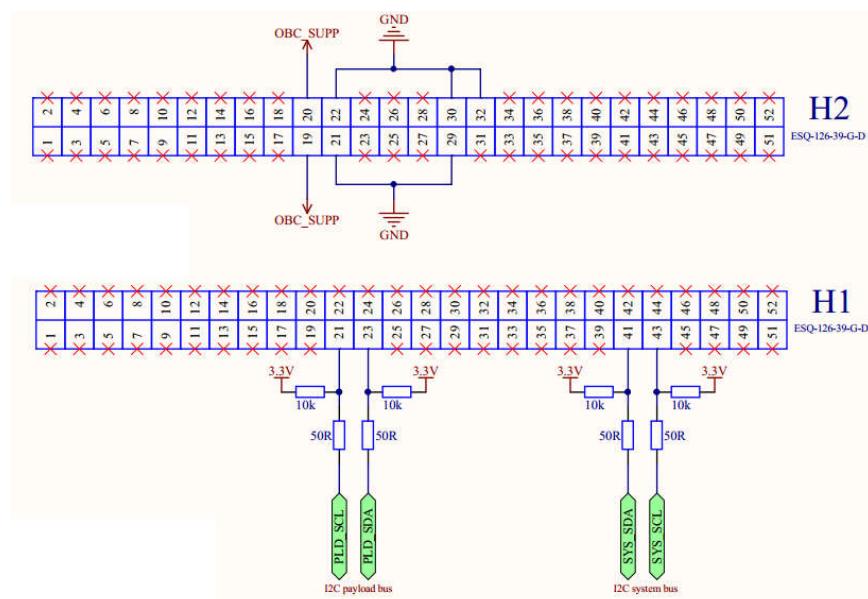


Figure 2-14. Pin-out of the OBC module

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

LCL's ID	Line	Current	Notes
LCL_OBC_0	ACC	0.5A	ACC: H1.19 and H1.20 Return lines: H2.29, H2.30 and H2.32.
LCL_OBC_1	ACC	0.5A	ACC: H1.19 and H1.20 Return lines: H2.29, H2.30 and H2.32.

Table 2-9. LCL lines for the OBC module

LCL_OBC_0 and LCL_OBC_1 are connected in parallel within the EPS. H1.19 and H1.20 are connected together within the EPS and within the OBC.

2.1.13 SUMMARY SUPPLIED POWER BY 3.3V, 5V AND ACC LINES

If all subsystems will be switched on, the EPS shall withstand with no permanent damages. This is not a normal situation but the EPS shall withstand. Summary power supplied by 3.3V, 5V and ACC lines are show below:

No.	Abbreviation	Full name	Voltage	Peak power
1	COMM1	ISIS UHF downlink / VHF uplink Full Duplex Transceiver	ACC	2.2W
2	ANT1	Deployable UHF and VHF antennas from ISIS company	5V	2W
3	BATTERY	Accumulator package - NanoPower BP4 from GOMSpace company	ACC	-
4	EPS	Electrical Power System	Internal	-
5	ADCS	Attitude Determination and Control System -	Actuators: 5V	1W
		ISIS Magnetorquer Board (iMTQ)	Sensors and electronics: 3.3V	0.2W
6	PLD	Payload electronics	SunS: 5V	1W
			Photodiodes: 5V	0.2W
			TCS: 2xACC (full redundancy)	2x3W

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

			Magnetometers: 3.3V	0.2W
			Sail: 2x ACC (full redundancy)	2x2W
			SADS: 2x ACC (full redundancy)	2x2W
7	OBC	On-board Computer from Createch Instruments S.A.	ACC	2W

Table 2-10. Power consumption on 3.3V, 5V and ACC lines for each subsystem

Bus	Summary power	Comment
3.3V	0.4W	Peak current: 0.15A
5V	4.2W	Peak current: 0.85A
ACC	18.2W	Peak current at 6V on MPB: 3A

Table 2-11. Summary power consumption on 3.3V, 5V and ACC lines

2.1.14 EXECUTION OF MAIN TASK IN SPITE OF FAILURE

Execution of main task – deploying deorbitation structure – in spite of failure of every other subsystem of the satellite, even the power supply. To make this possible, there shall be a time module which will measure the time from deploying deorbitation structure. The module should be independent from other parts of EPS and cannot be supplied from pulse converters. It imposes necessity of adding security modules connected directly to solar panels with its own real time clock. When it measures established time it would execute deorbitation procedure. Time counting shall not stop in shadow zone.

2.1.15 EMERGENCY DISCONNECTION WHEN LOW BATTERY

Emergency disconnection of subsystems from accumulators when deep discharge. The module should warn OBC before disconnecting in order to allow saving latest work results.

2.1.16 RUNNING IN SPACE ENVIRONMENT

Running in space environment:

- vacuum (no convection – problems with cooling). To prevent overheating of the EPS, parameters of components shall be derated in conformance with [4] standard and all heat dissipative spots shall be agreed by the TCS team.

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

- high temperature tolerance (-40 to at least 60°C),
- known tolerance for cumulative dose radiation,
- tolerance for damage of single integrated circuit by radiation or by ESD,
- tolerance for ambient plasma (in conformance with B.2 in [5]). We predict that the PW-Sat2 satellite will be launched on LEO orbit with inclination of around 98° (Sun-synchronous orbit). Dielectric surface can be charged and some electrostatic discharge can occur. All conductors shall be grounded on the whole spacecraft (for example conductive layers of the MLI). Floating insulators shall not be used on spacecraft surface - insulators shall be coated with conductive coating and shall be grounded.

To protect from latch-up damage due to radiation the LCL protections are necessary. Main integrated circuits should have radiation tests performed by NASA, ESA, TRAD, JAXA, IEEE or another well-known authority.

2.1.17 CURRENTS AND VOLTAGES MONITORING

Monitoring of currents and voltages of supply buses, accumulators and solar panels power, temperature measurements, etc.

2.1.18 COMMUNICATION WITH OBC

Communication with OBC through System I²C bus and Payload I²C bus (this one as a redundancy) shall be applied.

2.2 REQUIREMENTS FOR THE PCB

PCB of the EPS shall be designed in compliance with the mechanical PC-104 standard. This is a stackable family of embedded systems which define mechanical dimensions and electrical interfaces. The electrical interfaces of the PC-104 standard are not applicable for the PW-Sat2 mission. We will use a well-known electrical interface specification for Cubesats which are used both by the GOMSpace company, the ISIS company and the ClydeSpace company.

2.2.1 DIMENSIONS OF THE PCB

Mechanical dimension of the PCB is shown below (drawings [6] from Pumpkin company):

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

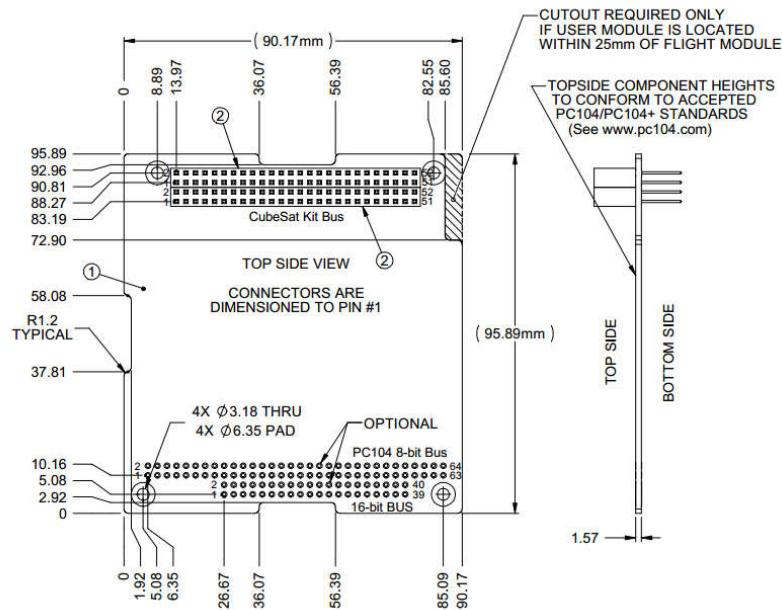


Figure 2-15. Top and side view of the PCB

PC-104 8-bit Bus is not applicable (holes are not drilled) for the PW-Sat2 mission.

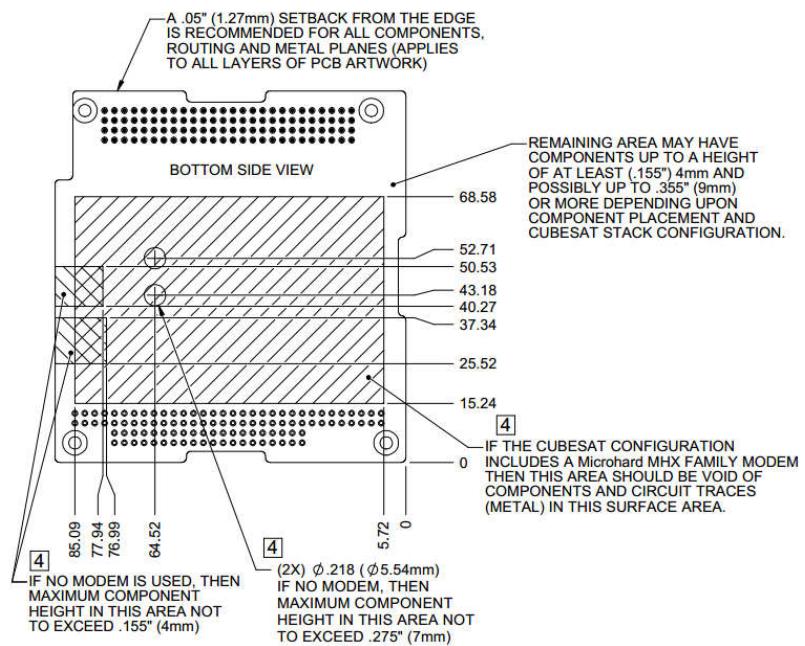


Figure 2-16. Bottom view of the PCB

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

An additional module (also called a daughter board) can be placed on the top side of the PCB. The additional module shall be within mechanical dimensions of the PC-104 standard. An example with the additional PCB which is placed on the top of the PCB (3G Flex EPS from ClydeSpace):

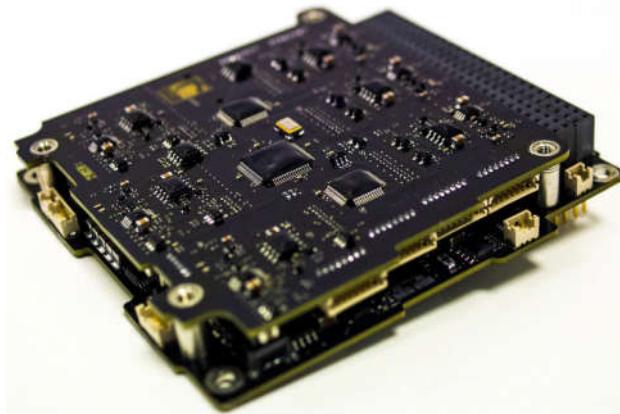


Figure 2-17. 3G Flex EPS from the ClydeSpace company

The 3G Flex EPS from ClydeSpace exceeds mechanical dimensions of the PC-104 standard. Our EPS should be within the PC-104 standard.

2.2.2 PCB DESIGN

PCB design process should be performed in conformance with [7]. The ECSS standard contains a lot of well PCB design rules, which are very useful.

2.2.3 PCB ASSEMBLING AND CLEANROOM FACILITIES

The PCB will be assembled in conformance with [8] and [9]. Now we have one member team, which has a certificate to perform conventional and surface-mount soldering operations in conformance with [8] and [9] (category 3 - operator). In the future may be more certificates. We have access to cleanroom facilities at Creotech Instruments S.A. company and a lot of employees' support. This will allow us to perform the assembling process with high quality.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

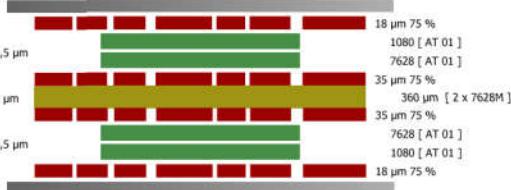


Figure 2-18. Cleanroom facilities at Creotech Instruments S.A.

During the design process we have to consider that the PCB will be assembled in accordance with [8] and [9].

2.2.4 PCB PROCUREMENT

The PCB of the engineering model of the EPS will be ordered from the Techno Service company. We can to use three kinds of PCB stack-ups:

Number of Cu-layers	Nominal thickness [mm]	Actual thickness [mm]	
4	1	0.979	

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

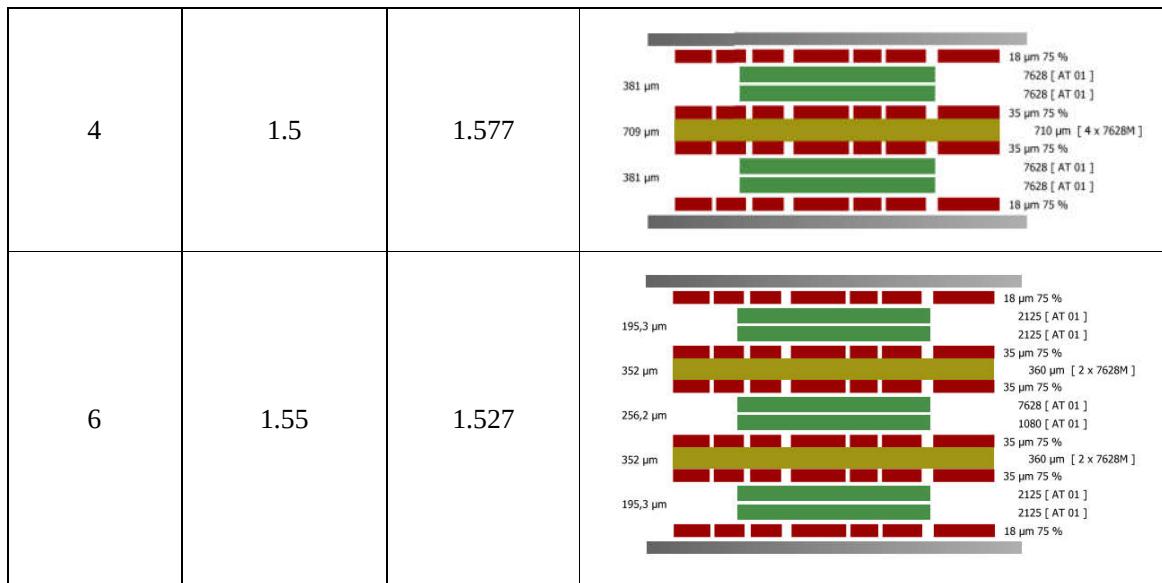


Table 2-12. PCB stack layers from the Techno Service company

The main EPS board should be designed with nominal thickness equal to 1.55mm (6-layers) or 1.5mm (4-layers). The daughter board (if it will be applied) should be designed with nominal thickness equal to 1mm (4-layers) or 1.5mm (4-layers).

We have to examine the PCB during the vacuum tests. If the tests will be successful then the flight PCB of the EPS can be ordered from the Techno Service company.

The PCB cannot be finished by a chemical gold coating or a HAL lead-free coating. The PCB shall be finished by a HAL SnPb coating (according to ECSS standards).

2.3 ELECTROMAGNETIC COMPATIBILITY

To maintain high quality and high reliability of the EPS some EMC tests should be performed. Some procedures from [10] can be applied.

2.3.1 LINE IMPEDANCE STABILIZATION NETWORK

The line impedance stabilization network (LISN) is a device, which is used in conducted and radiated radio-frequency emission tests. An example of a half LISN circuit from figure no. 6 in [11].

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

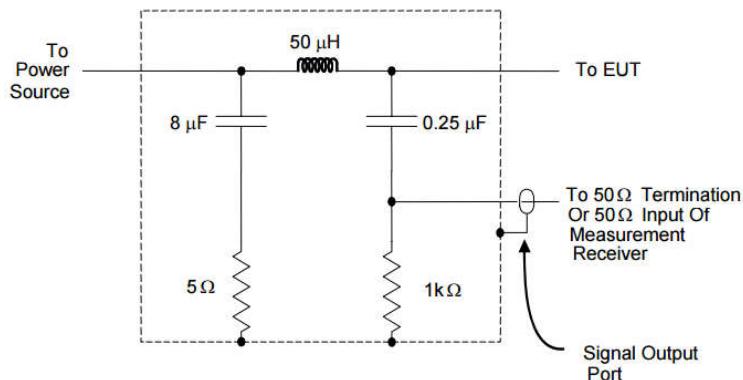


Figure 2-19. LISN schematic – source [11]

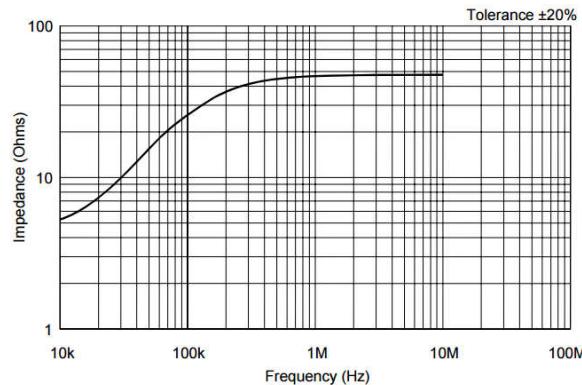


Figure 2-20. LISN impedance – source [11]

2.3.2 INRUSH CURRENT

Any inrush current within the EPS cannot exceed the specified requirements for a circuit. The inrush current can be present:

- when the deployment switch is switched on
- when the RBL switch is switched on
- when a LCL switch is switched on
- when an MPPT converter is switched on

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

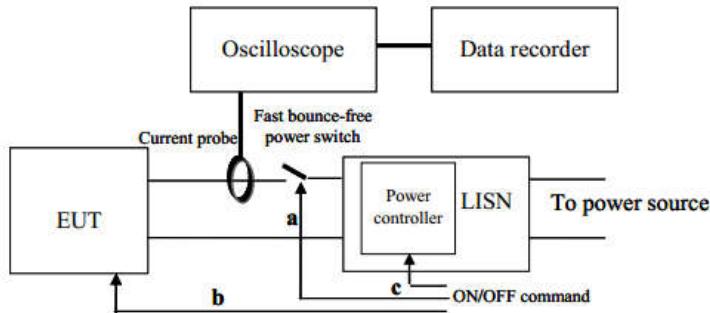


Figure 2-21. Inrush current: measurement setup – 5.4.4 from [10]

The LISN will be used as low pass filter, which is responsible for filtering noise directly from power source. At the output of the LISN the capacitor battery should be connected (then the LISN is constantly switched on). The capacitor battery should have a few hundreds of μF with low ESR.

During a test the fast bounce-free power switch is switched on. Then the current is rising up with a high $\frac{dI}{dT}$ factor. The pulse current is conducted directly from the capacitor battery to the EUT. If a state of the circuit is steady, then the constant current is conducted directly from a power source through the LISN. The inrush current shall be recorded and analysed.

The test method is used only for an MPPT converter. A test method for the LCL, the RBL and the deployment switch is completely different, because the switches are within the EPS.

2.3.3 DIFFERENTIAL AND COMMON MODE CONDUCTED EMISSION

Conducted noise emissions on any input and output power leads of the EPS emitted by the EPS should be measured. There are two kinds of conducted emissions: differential mode conducted emission and common mode conducted emission.

- At input of the MPPT converter. Measurement circuit is shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

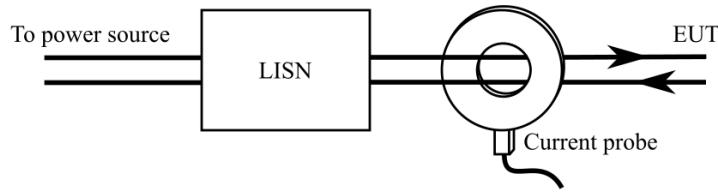


Figure 2-22. Common mode conducted emissions – measurement setup

- At output of the MPPT. The LISN is connected to the input of the MPPT converter but the current probe is connected at output of the MPPT converter.
- At input of all 3.3 and 5V DC/DC converters. The LISN is connected to the input of the MPPT converter but the current probe is connected at any input of 3.3 or 5V DC/DC converter.
- At outputs of all 3.3 and 5V DC/DC converters. The LISN is connected to the input of the MPPT converter but the current probe is connected at any output of 3.3 or 5V DC/DC converter.
- At output of ACC bus. The LISN is connected to the input of the MPPT converter but the current probe is connected at ACC bus.

Differential mode conducted emission should be measured:

- At input of the MPPT converter. Measurement circuits are shown below:

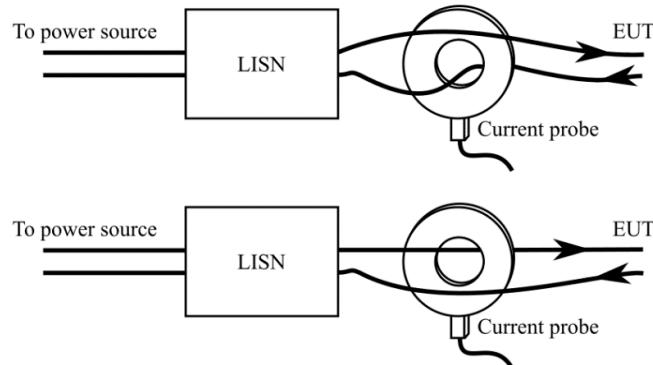


Figure 2-23. Differential mode conducted emission – measurement setup

- The measurement order is like for common mode conducted emission.

The current probe will be connected to an EMC spectrum analyzer.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

The common mode and differential mode conducted emission should be within [10] standard. Some deviations will be analyzed.

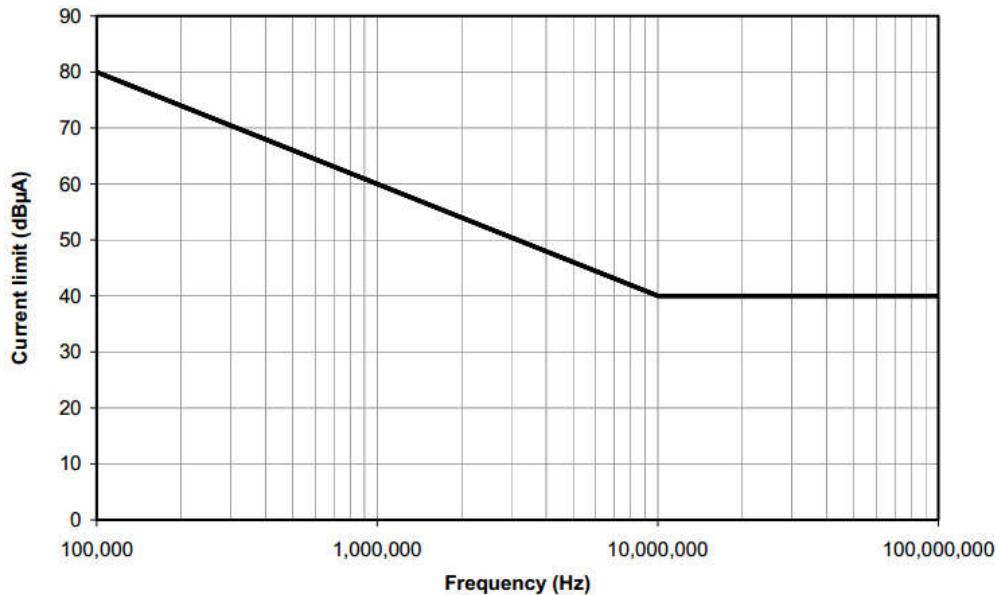


Figure 2-24. Common mode conducted emission limit – source [10]

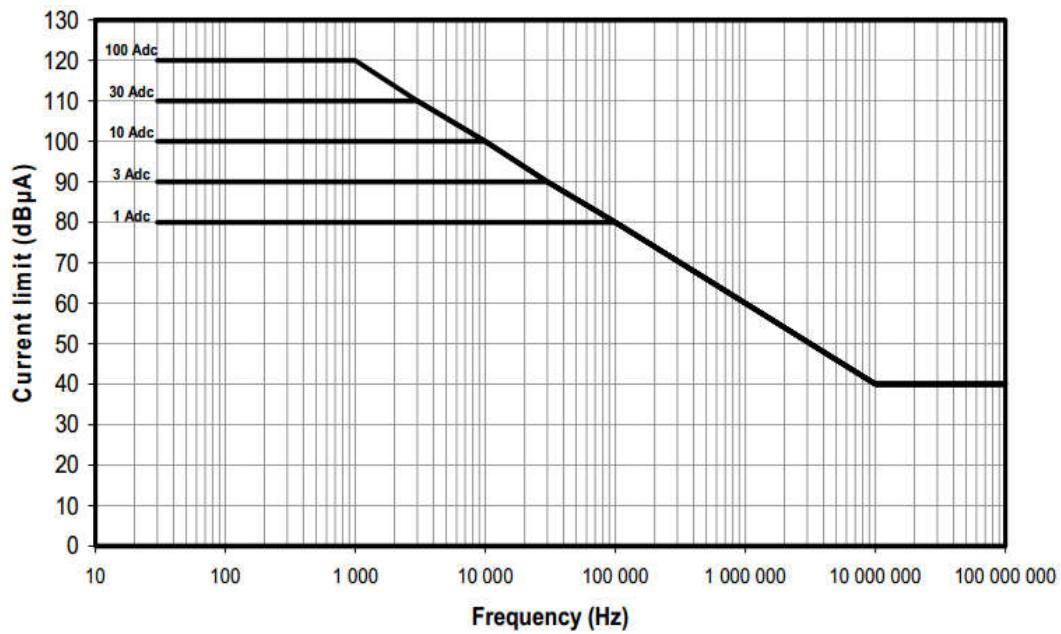


Figure 2-25. Differential mode conducted emission limit – source [10]

	PW-Sat2	Preliminary Design Review	 PW-SAT2
	2015-05-23	Electrical Power System	
	Phase B		

3 GENERAL SYSTEM DESIGN

There are some topologies of electrical power systems. First of all, photovoltaic system needs tracking of maximum power point (MPPT). Second, batteries needs charging/discharging circuits. Satellite's subsystems needs controlled, regulated/unregulated and protected power supply lines.

3.1 SOLAR PANELS

The following chapter contain detailed information about solar panels.

3.1.1 AVAILABILITY OF INDIVIDUAL SOLAR CELLS AND ASSEMBLED MODULES

We will use space qualified InGaP/GaAs/Ge on Ge substrate triple junction solar cells.

Single solar cells providers offer single panels when ordering 30 pieces:

Company	Characteristics	Price per unit
AzurSpace (Germany)	Efficiency 30%, dimensions 80x40mm	270€
CESI (Italy)	Efficiency 30%, dimensions 80x30mm	280€

Table 3-1. Solar cells – offers from providers when order of 30 pieces

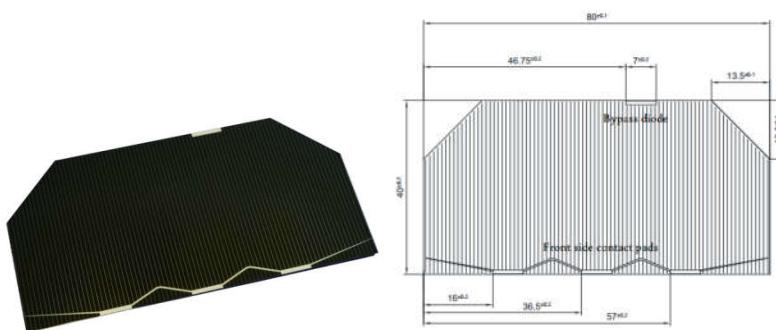


Figure 3-1. Solar cell from Azur Space company - Azur Space website

There is a possibility of making prepared modules of solar panels. On a picture below an example of prepared module of wall 1U from GOMSpace company (solar cells from AzurSpace company):

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

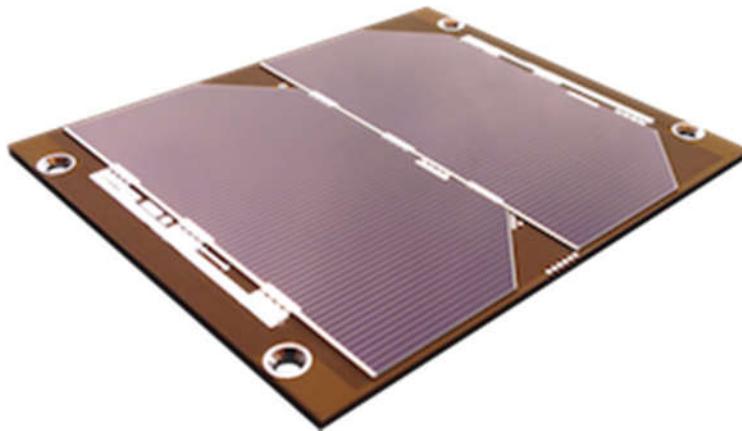


Figure 3-2. Assembled solar module from GOMSpace company - GOMSpace website

Solar panels are very fragile and it's very easy to damage them. We decided to buy prepared modules from space company. Currently we are negotiating with companies.

Solar panel no.	Company / model	Price [€]
SP2	GOMSpace P110A or P110B	2000
SP5	GOMSpace P110A or P110B	2000
SP1	we are negotiating (GOMSpace and others)	up to 5000
SP3	we are negotiating (GOMSpace and others)	up to 5000

Table 3-2. Currently offers for assembled modules

Despite that the solar modules (GOMSpace P110A or P110B) have temperature sensors, we will use external PT1000 temperature sensors. We have some experience with digital temperature sensors on the solar panel from PW-Sat. PT1000 will be more reliable (for example more resistant to high temperatures and thermal shocks), unlike digital temperature sensors. PT1000 sensors will be glued with a thermal conductive glue on the bottom side of the solar panels.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

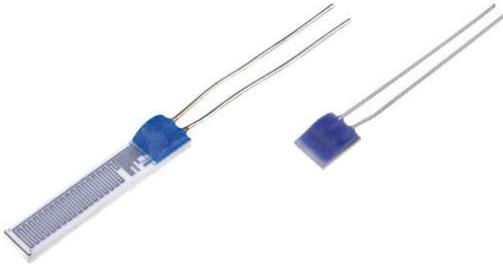


Figure 3-3. PT1000 temp. sensor, vacuum sputtered onto a ceramic substrate- TME.eu website

The second reason, to use PT1000 sensors, is: digital interfaces cannot have long wires. We have long path from solar wing to EPS.

And third: we are still negotiating with solar modules providers. Different providers have different temperature sensors. Glued PT1000 sensor is a universal solution.

Temperature sensors will be not redundant (it is not necessary): one sensor per one solar panel.

3.1.2 ASSEMBLY METHOD

There are two methods to assemble solar cells: soldering and gluing. Assembly method will depend on wings provider. Assembly of the solar cell will be outsourced to external provider.

3.1.3 CONNECTIONS BETWEEN THE SOLAR CELLS

Solar cells are connected in different circuits. It depends on the solar cell's location.

Four solar cells are placed on single-side of solar wing. They are shown below:

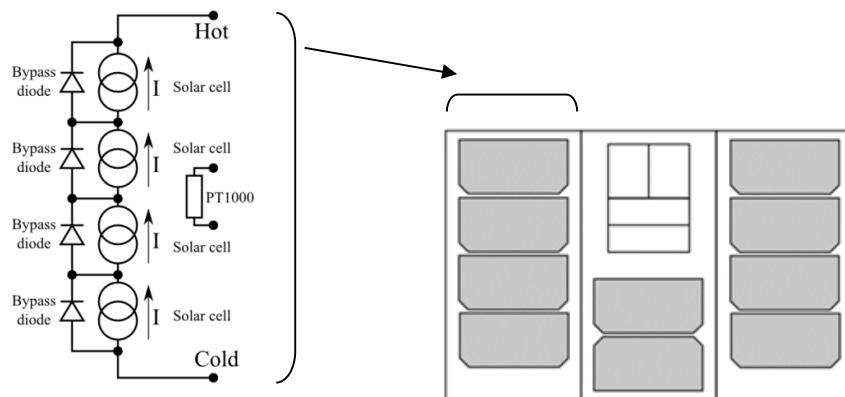


Figure 3-4. Internal connections inthe SP3 Y- (when closed) single-side solar wing

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

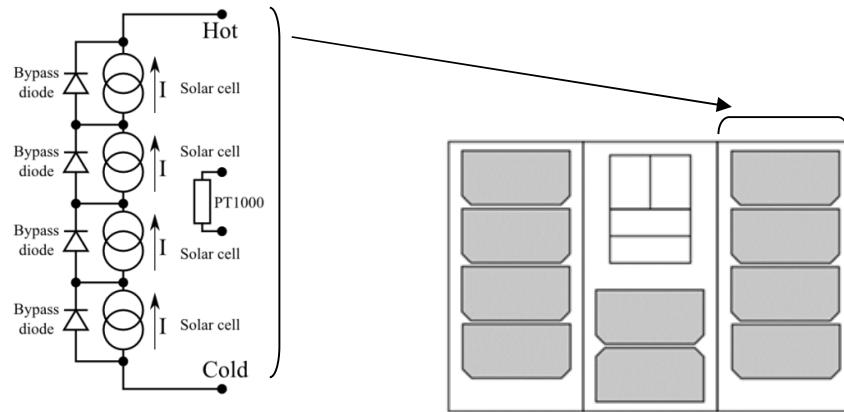


Figure 3-4. Internal connections in the SP1 Y+ (when closed) single-side solar wing

Parameters of assembled four-cell solar panels (based on AzurSpace single solar cell data for type: 3G28C) for SP3Y- and SP1Y+ are shown below:

Open Circuit V_{oc} [V]	10.7
Short Circuit I_{sc} [mA]	506
Voltage at max. Power V_{mp} [V]	9.5
Current at max. Power I_{mp} [mA]	487
Efficiency at 28°C [%]	~28

Table 3-3. Parameters of solar panels for SP3 Y- and SP1 Y+

Two connected solar cells are placed on the X+ and X- sides. They are shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

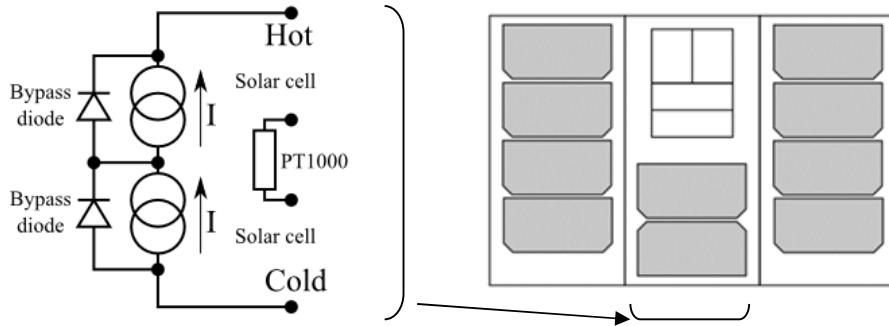


Figure 3-5. Internal connections of solar panel for SP2 X+

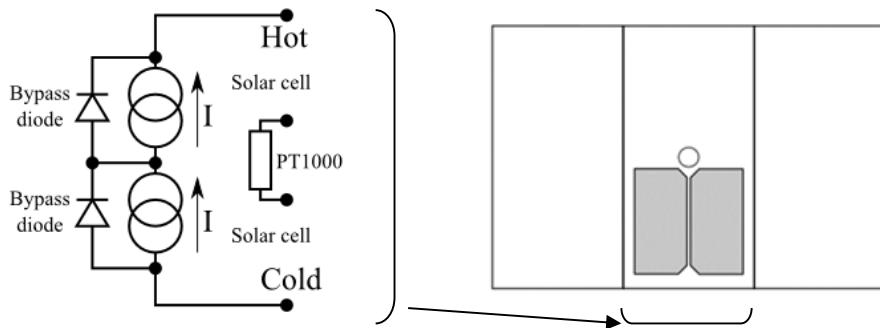


Figure 3-6. Connections of solar panel for SP5 X-

Parameters of assembled double-cell solar panels (based on AzurSpace single solar cell data for type: 3G28C) for SP5 X- and SP2 X- are shown below:

Open Circuit V_{oc} [V]	5.34
Short Circuit I_{sc} [mA]	506
Voltage at max. Power V_{mp} [V]	4.74
Current at max. Power I_{mp} [mA]	487
Efficiency at 28°C [%]	~28

Table 3-4. Parameters of solar panels for SP5 X- and SP2 X+

3.1.4 THE OPENING ANGLE OF THE SOLAR WINGS

If the SADS subsystem will be implemented, then there is possibility to open the solar wings at a right angle or another. To give a high resistance to failure the ADCS subsystem during the mission (when the solar wings are fully deployed), the opening angle should be another than a right angle. The SADS

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

mechanical subsystem is responsible for the opening solar wings. The DT team is responsible for the SADS subsystem and for an opening angle assurance of the subsystem.

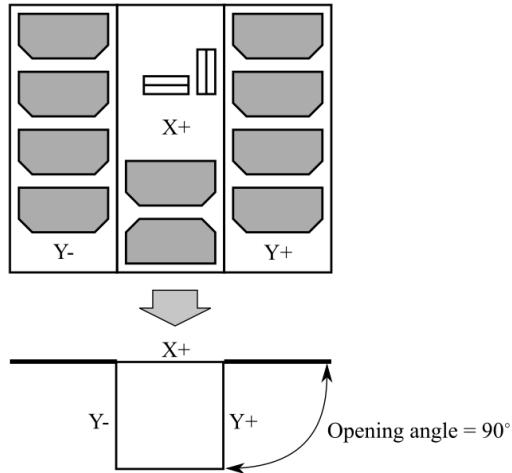


Figure 3-5. When the opening angle of the solar wings is equal to 90 deg

3.1.4.1 The opening angle of the solar wings calculation

Calculations of an optimal opening angle of the solar wings at Y- and Y+ sides are shown below. Because we have no influence on the Z+ and Z- sides (there are no solar panels), the calculations will be performed for one axis.

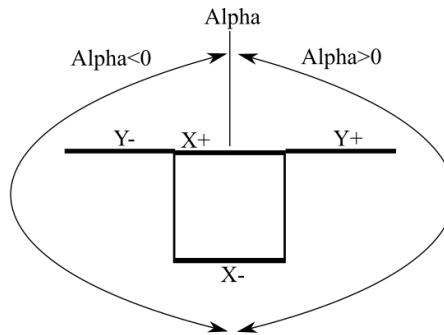


Figure 3-6. Opening angle of the solar wings calculations – axis definition

The satellite is rotated around the Alpha axis from -180° to $+180^\circ$. To decrease a probability when a harvested power from all solar panels drops to zero, the opening angle of the solar wings should be lower than 90° . Of course a peak power at sun-pointing mode will be lower if the opening angle is lower than 90° .

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

The harvested power when the opening angle is equal to 90 ° from the X+ solar panel (a red line), the X- solar panel (a cyan line), the Y+ solar panel (a green line), the Y- solar panel (a blue line). All of them are summed on a black dotted line. The chart is shown below:

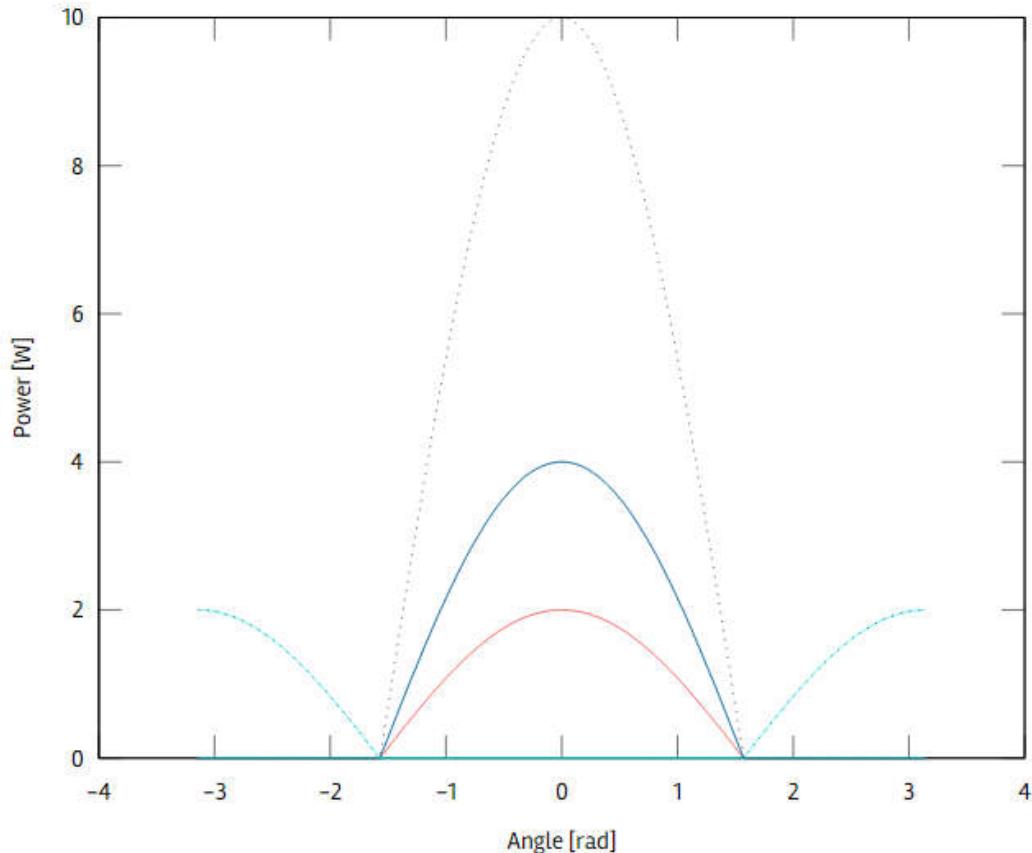


Figure 3-7. The harvested power when the opening angle is equal to 90 deg

As we can see, there are two angles when the power drops to zero. The lowest harvested power during rotating around the Alpha axis can be increased when the opening angle is lower than 90°. We assume that the lowest harvested power should be higher or equal around 1W.

The harvested power when the opening angle is equal to 60 ° from the X+ solar panel (a red line), the X- solar panel (a cyan line), the Y+ solar panel (a green line), the Y- solar panel (a blue line). All of them are summed on a black dotted line. The chart is shown below:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

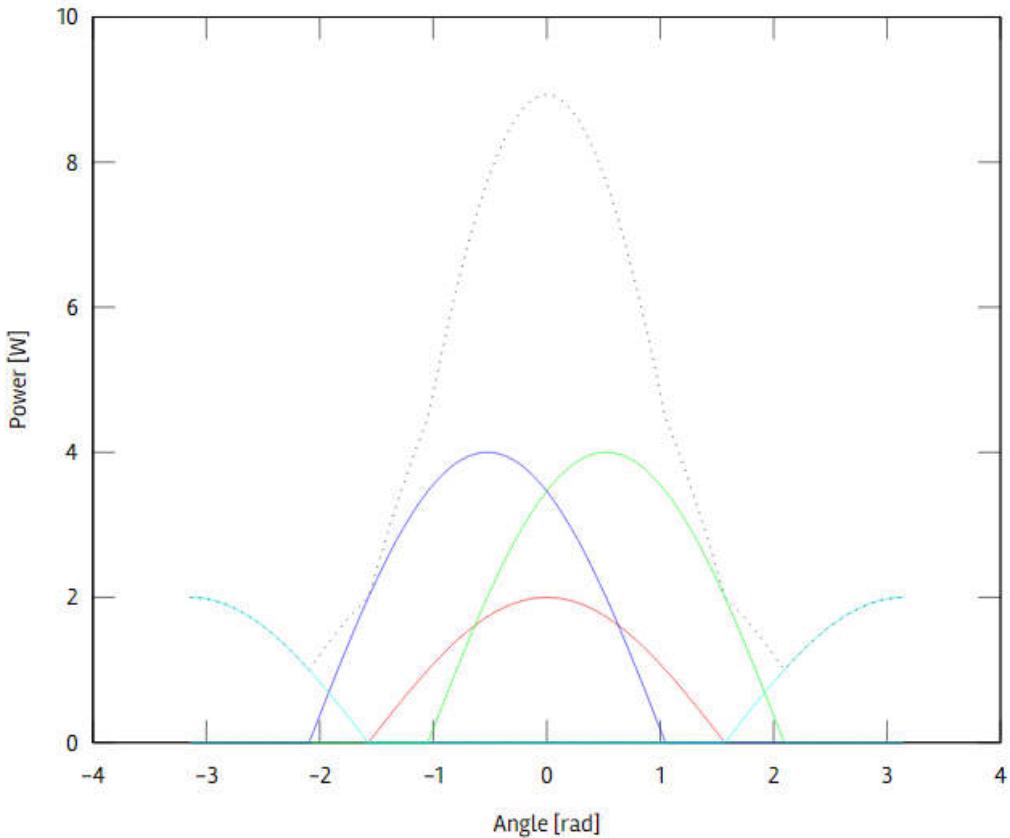


Figure 3-8. The harvested power when the opening angle is equal to 60 deg

If the opening angle is equal to 50°, the lowest harvested power is equal to 1.3W. The peak power is equal to 8.1W.

If the opening angle is equal to 60°, the lowest harvested power is equal to 1W. The peak power is equal to 8.7W.

If the opening angle is equal to 70°, the lowest harvested power is equal to 0.7 W. The peak power is equal to 9.5W.

Finally, the opening angle of the solar wings should be equal to 60° with tolerance +/- 10°.

If the ADCS subsystem will damage at the beginning of the mission (when the solar wings are closed), the solar wings should not be deployed.

3.2 MPPT TOPOLOGY

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

MPPT makes the maximum use of the incident solar energy (it gives very high efficiency in energy conversion). General topologies shown below are applicable to such area:

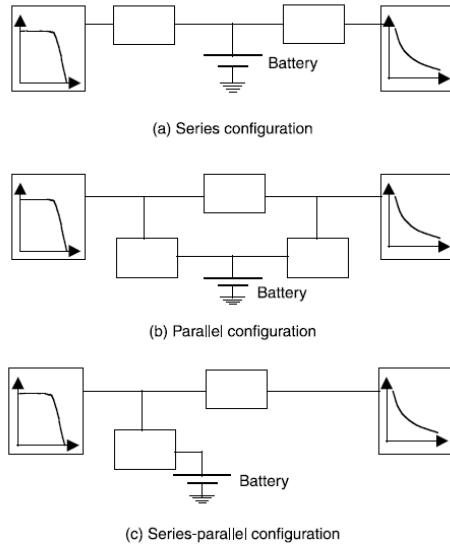


Figure 3-9. Battery charge and discharge options in PPT architecture, [12]page 77

During phase A of the project was chosen series configuration. This configuration gives high efficiency and it is simple to design.

To achieve high efficiency, the MPPT subsystem needs DC/DC pulse converters. Due to limited of PCB area, DC/DC converters should be as smallest as possible.

Simple scheme, including charging/discharging control and power conditioning, is shown below:

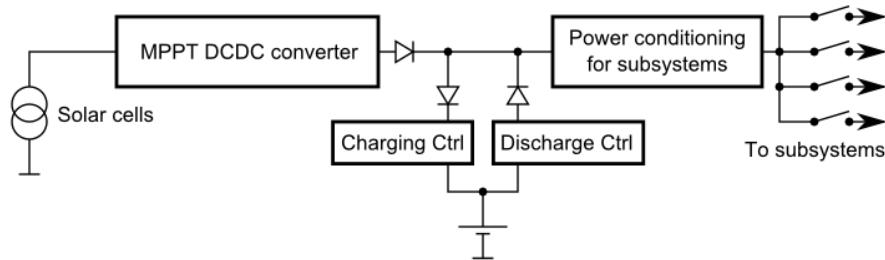


Figure 3-10. Simple scheme of the MPPT, including charging and discharging control

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

3.2.1 MPPT CONTROLLED DCDC CONVERTER

To perform maximum power point tracking a controlled DC/DC converter will be used. To achieve high efficiency, the DC/DC converter will be controlled by MPPT algorithms. There are two ways to obtain MPPT algorithm within a DC/DC converter:

- To buy a ready-made DC/DC converter, which implements the MPPT algorithms
- To build standard DC/DC converter driven by microcontroller, which implements the MPPT algorithms

Requirements for MPPT controlled DC/DC converters:

Requirement	Required value
Operating temperature range	At least -40°C to 85°C (industrial range), but should be wider
Package	DC/DC converter should be as small as possible, but not like DFN or QFN. Can be TSSOP, SOIC or other.
Input voltage range	For a two-cell solar panel: 0 - 6V
	For a four-cell solar panel: 0 - 12V
Input current range	At least 0 - 0.5A
Output voltage range	8.2V +/- 2% (worst case)
Output current	For a two-cell solar panel: 0 – 0.3A
	For a four-cell solar panel: 0 – 0.6A
Switching frequency	~500kHz
Converter topology	For a two-cell solar panel: boost converter
	For a four-cell solar panel: buck-boost converter

Table 3-5. Requirements for MPPT controlled DC/DC converters

For example, ready-made DC/DC converters, which implements the MPPT algorithms are shown below:

Part and manufacturer	Comments
SPV1020 from STMicroelectronics	Input voltage range: 6.5V to 45V Converter topology: boost

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

	Two-cell solar panel needs a boost converter with input voltage range from at least 3V to 6V. The converter is rejected.
SPV1040 from STMicroelectronics	Output voltage range: 2V to 5.2V The highest output voltage is too low. The converter is rejected.
SPV1050 from STMicroelectronics	Output voltage range: 2.5V to 5.3V The highest output voltage is too low. The converter is rejected.
LT3652 from Linear Technology	Due to buck-converter topology it is rejected.
LTM8062 from Linear Technology	Due to LGA package it is rejected.
BQ24650 from Texas Instruments	Due to synchronous-buck topology and input voltage regulation method (to achieve highest efficiency should be input power regulation method), it is rejected.
LT8490 from Linear Technology	Due to too big package –QFN 64, it is rejected.

Table 3-6. Ready-made DC/DC converters, which implements the MPPT algorithms

In conclusion, we cannot find a suitable ready-made DC/DC converter, which to meet the requirements. We decide to build standard DC/DC converter driven by microcontroller, which implements the MPPT algorithms.

DC/DC converter will be controlled by digital-to-analogue (DAC) converter. DAC will be driven by a microcontroller. Also we will check the PWM+LPF solution. PWM is much cheaper and simple than external DAC.

Finally, the MPPT DC/DC converter topology was selected and it is shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

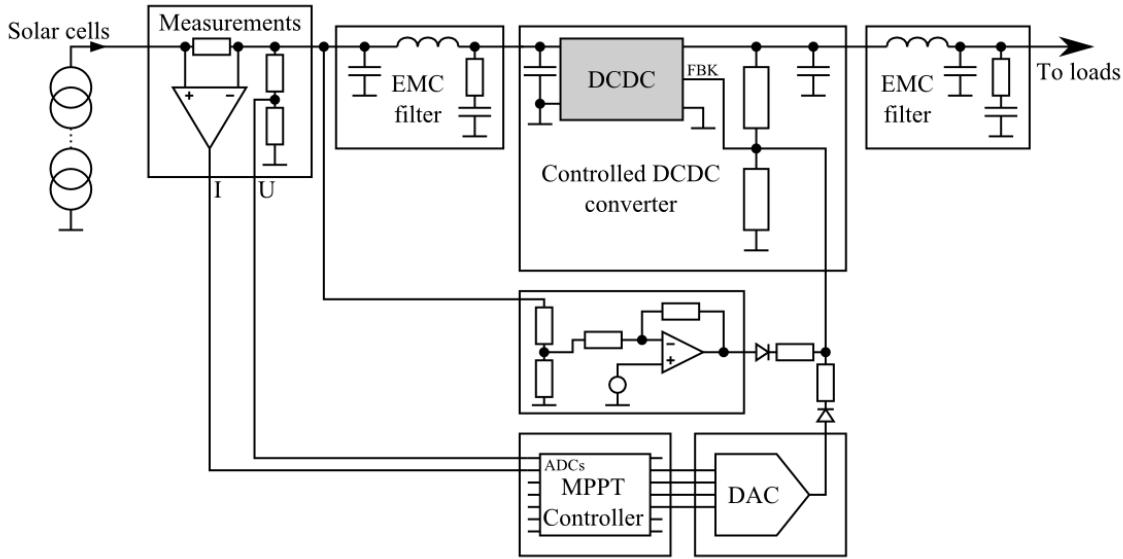


Figure 3-11. Controlled DCDC converter with MPPT

Despite the digital MPPT controller breaks down, the system is still working (but with lower efficiency). The advantage of this topology is very important to achieve high reliability.

If a solar panel is overloaded, then the output voltage of the solar panel is dropping. The voltage can drop below the operating voltage of the DCDC converter (and it can oscillate). Additional protection loop should be added to prevent this situation.

3.2.2 MPPT ALGORITHM

There are two algorithms for maximum power point tracking: Perturb & Observe (P&O) and Incremental Conductance.

The P&O algorithm introduces a perturbation in the panel operating voltage by modifying the output load (for example by introduce external DC voltage to FBK of the converter by a resistor – it changes the converter output voltage and this results in change in output load). If the panel operating voltage is modified, then the output power of the solar panel is observed. Depending on the $P_{\text{previous}} - P_{\text{actual}}$ equation outcome, in a next step the panel operating voltage will be decreased or increased. After achieving the maximum power point, the algorithm oscillates around the correct value.

The P&O algorithm needs to measure the panel voltage and current.

Of course, if an output load has constant power character and the load has higher power than the solar panel, the panel output voltage is dropping below the converter's operating level (and it is oscillating).

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

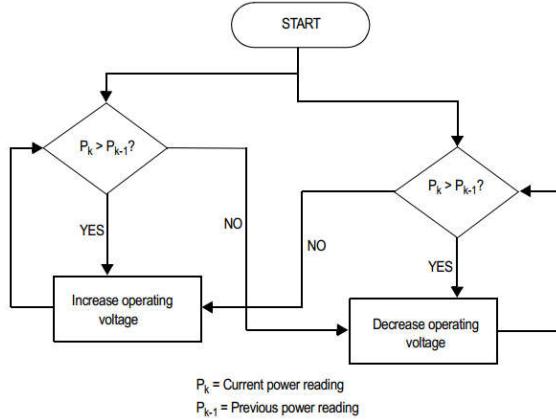


Figure 3-12. Perturb and Observe algorithm – [13] page 4

The Incremental Conductance algorithm is based on the incremental and instantaneous conductance of the solar panel. The power curve derivative vs. voltage is equal to zero at the maximum power point, negative on the right side and positive on the left side.

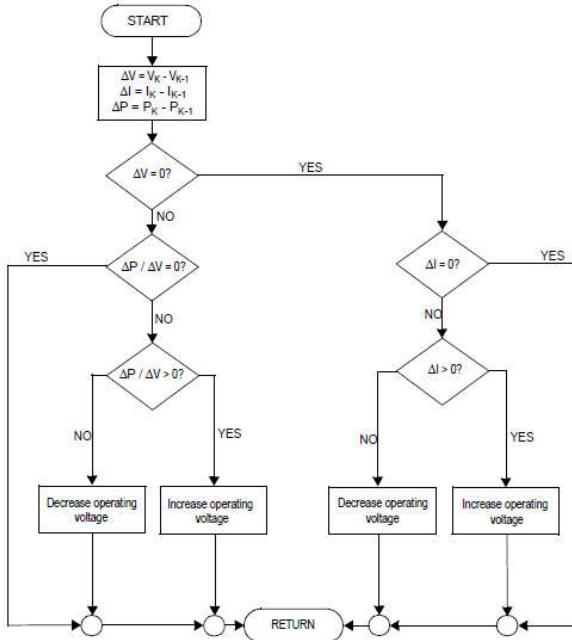


Figure 3-13. Incremental Conductance algorithm – [13] page 5

The P&O algorithm is quite simple in software, robust and most popular. The P&O algorithm was selected but the Incremental Conductance algorithm will be tested too (only for research).

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

3.3 SOLAR POWER SUMMING

The output power of the MPPT converters shall be summed on a power bus. To achieve high efficiency ideal diodes will be used for power summing.

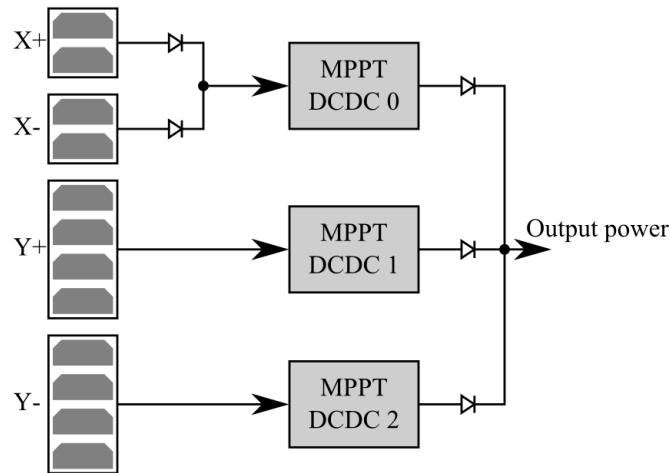


Figure 3-14. Summing of the solar power

There are five ideal diodes. It can be based on a P-channel MOSFET transistor driven by an integrated ideal diode driver.

Due to lack of space, we cannot implement two independent summing buses for redundancy (we have only two SPDT kill-switch, which are connected in parallel circuit – redundant power bus is not possible). There is only one summing power bus. Many student satellites had only one summing bus (for example SwissCube [14], ESTCube-1 [15]). It is simple to design but this solution requires more attention during design process. Consequently the sub-circuits, which are connected directly to the summing bus, should be as reliable as possible.

3.4 EXTERNAL POWER FOR PRE-LAUNCH TESTING

If the satellite will be within a P-POD, an external power is needed for pre-launch testing from an EGSE. The EPS has three independent MPPT converters. To achieve full coverage in the tests, the external power should be connected directly to the MPPT converters.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

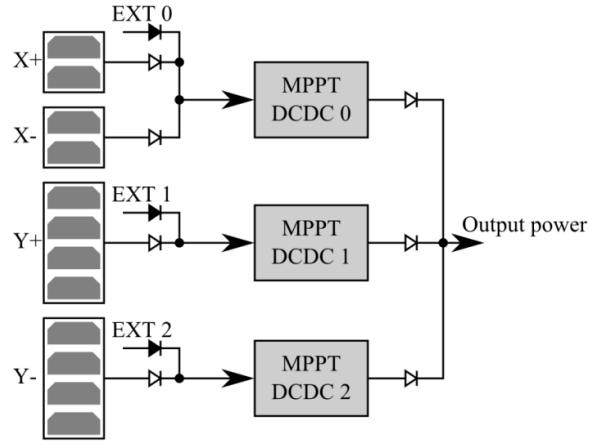


Figure 3-15. External supply

Now, there are seven ideal diodes for summing solar power. There are three Schottky diodes for summing external power.

3.5 MAIN POWER BUS

The Main Power Bus is an unregulated bus, which is used for power harvesting and distribution.

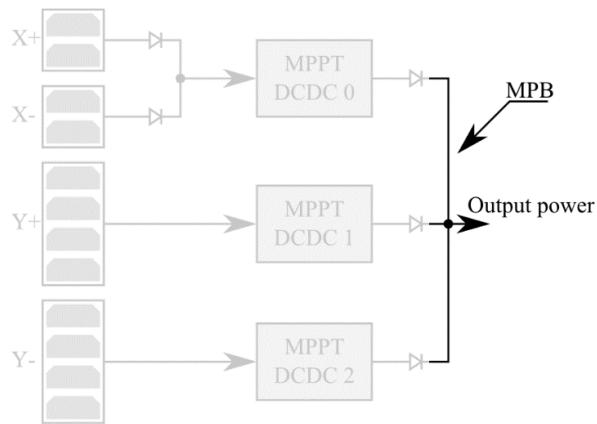


Figure 3-16. Main Power Bus

The MPB is very sensitive to damage. To prevent single points failure, all components, which are connected directly to the bus, should be as reliable as possible. For example, low quality tantalum capacitor (it has high failure rate level) can damage for the MPB. This tantalum capacitor can short circuit without any notice, even it is working within specification. High quality components with low failure rate level should be used. Special connections, pairs and series connections for example, can increase the reliability:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

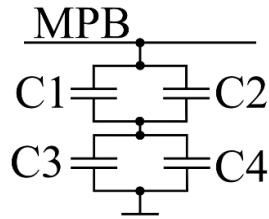


Figure 3-17. Special connections of the capacitors on the MPB

Voltage range on the MPB will be from 6.00V (low battery level) to 8.10V (open circuit voltage of the MPPT converter). These voltages have some tolerance.

3.6 ENERGY STORAGE

For energy storage we will use lithium-ion battery cells.

We have to use space qualified batteries. Standard batteries can explode during vacuum testing. We haven't any vacuum chamber, which can withstand explosion of the batteries. Our vacuum chamber is very fragile for any gases, which can escape from the battery.

We have chosen NanoPower BP4 package of li-ion accumulators from GOMSpace company:

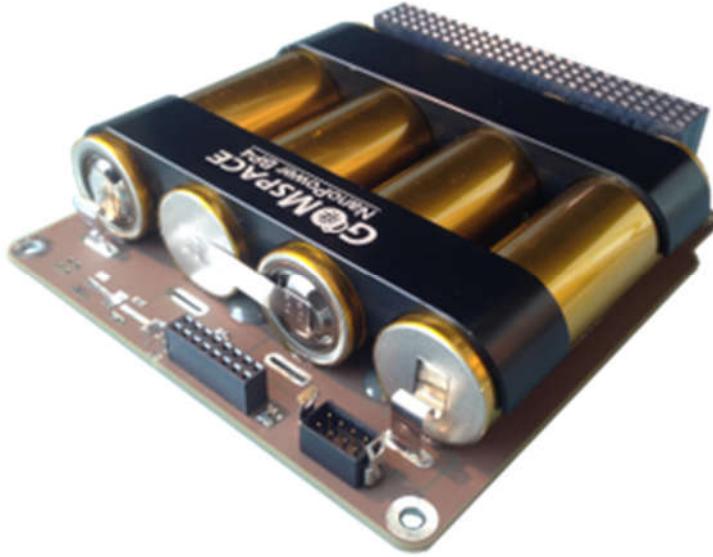


Figure 3-18. NanoPower BP4 from GOMSpace company

There are mounted 18650 li-ion accumulators. Possible configurations of the accumulators are shown below:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

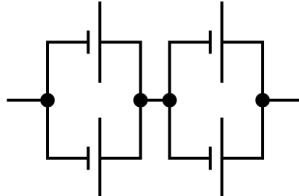
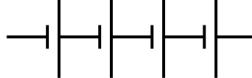
Configurations	Number of cells	Circuit	2600mAh cell(Nominal)
2P – 2S	4		38.5Wh 6 - 8.4V 5.2Ah
1P – 4S	4		38.5Wh 12 - 16.8V 2.6Ah

Table 3-7. Configurations of the accumulators for NanoPower BP4

Any other accumulator configurations requires additional testing by the GOMSpace company. It is very expensive (even over 15 000€).

Three different cells are available:

- 3.7V with 2600mAh – it was chosen,
- 3.7V with 1800mAh,
- 3.3V with 1100mAh.

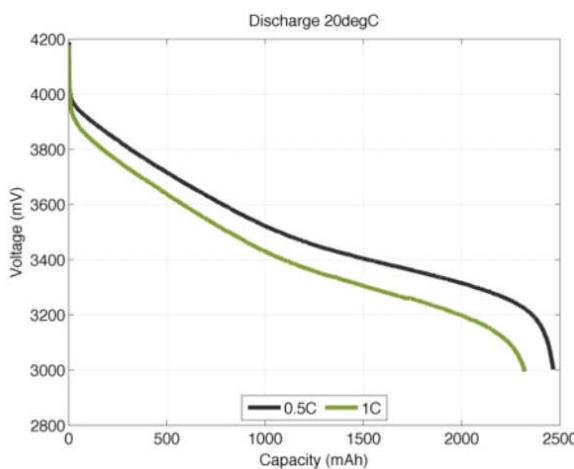


Figure 3-19. Discharge characteristics of the 3.7V 2600mAh cell – GOMSpace specification

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

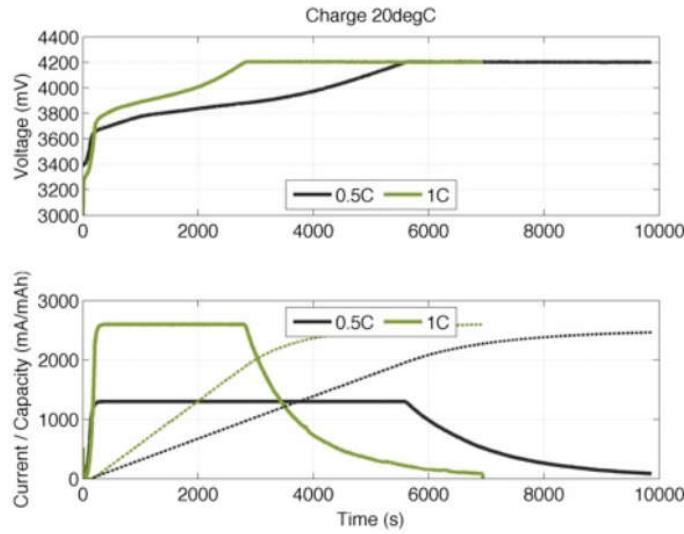


Figure 3-20. Charge characteristics of the 3.7V 2600mAh cell – GOMSpace specification

The 2P-2S configuration with heater was chosen. Cells are connected to a 16-pin dual row connector on the PCB. Heaters are driven by a P-MOSFET from 16-pin connector. Additional GND-break connector for kill-switch is available. Digital temperature sensors are placed on the PCB too.

Specification of the NanoPower BP4 pack:

Parameter	Value
Voltage range	6.0 – 8.4V
Capacity	5200mAh / 38.5Wh
Charge current	2500mA – 5000mA
Discharge current	0 – 7500mA
Mass	240g
Charge temperature	-5°C to 45°C
Discharge temperature	-20°C to 60°C
Internal impedance (2P 2S topology)	70mΩ
Cycle life (20% capacity loss) at 100% DoD	350

Table 3-8. Specification of the NanoPower BP4 pack

Price of the NanoPower BP4 pack: 1500€ + 800€ (heaters option) = 2300€.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

It is space qualified product and consequently, redundancy of the battery is not necessary. Second, due to lack of space we cannot place an additional battery pack.

3.6.1 CHARGING AND DISCHARGING CYCLES DURING THE MISSION

PW-Sat2 satellite will be launched on the LEO orbit. The orbit period time is about 90 minutes. The satellite will periodically come into the zone of the day and night. Each orbit means one charging cycle for the battery pack. Our mission is planned for about three months. This means:

$$24\text{h} / 1.5\text{h} = 16 \text{ orbits per 24h}$$

$$3 * 30 \text{ days} * 16 \text{ orbits} = 1440 \text{ orbits per the mission}$$

So, there are 1440 charging/discharging cycles for the mission. If the DoD=100% will be applied, then the battery pack can be destroyed. It can compromise the mission.

The battery pack should be specified for at least 2000 charge/discharge cycles at 20% capacity loss. This means, that the special tricks to prolong life of the battery pack should be applied.

3.6.2 EXTENDING LI-ION BATTERY LIFE

If the DoD=100% will be applied, then the li-ion battery withstands ~350 charge/discharge cycles with 20% loss of nominal capacity. To prolong life of the battery, the DoD factor should be decreased. Of course, temperatures and the charged voltage level are very important too.

All the necessary information about battery charging/discharging are available on the www.BatteryUniversity.com website and [16]. We would like to refer to this page in this chapter.

Partial discharge prolongs battery life, this means the DoD factor should be decreased:

DoD [%]	Discharge cycles at 20% capacity loss
100	300 - 500
50	1200 - 1500
20	2000 - 2500

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

10	3750 - 4700
----	-------------

Table 3-9. Cycle life vs DoD – BU-808 from [16]

Most of discharging/charging cycles should be with the DoD between 10-20%. Of course, a couple of cycles with the DoD over than 20% are not dangerous for the mission. During the power budget calculations we cannot forget about it.

Most li-ion cells are charged to 4.20V. If the charged voltage will be decreased, then the life cycle will be increased. The relationship is shown below:

Charge level per one li-ion cell [V]	Discharge cycles	Capacity at full charge [%]
4.20	300 – 500	100
4.10	600 – 1000	~86
4.00	1200 – 2000	~72
3.92	2400 - 4000	~58

Table 3-10. Cycle life vs charge voltage level – BU-808 from [16]

To prolong the life cycle, the charge voltage level should be set between 7.84V and 8.00V.

The end of charging cycle occurs when the current drops to three percent of the rated current [16]. For NanoPower BP4 pack it is about 150mA.

According to a discharge characteristic of selected li-ion cells, a charging cycle should begin when the voltage drops below 7V (equal to $2 \times 3.50V$). The voltage level is measured on the battery pack. This assumption should be verified during the tests.

Also to high and to low temperatures can decrease the life cycle. Over-temperature protection for charging and discharging control shall be applied. To protect from freezing, the heaters shall be mounted.

3.6.3 CHARGING METHOD

For charging the li-ion battery a correct method shall be selected. We will use the well-known CC-CV method. The CV level will be defined by the constant charging voltage level within the charging controller. Maximal CC level will be defined by a maximal power harvested from the solar panel. Actual CC level depends on an actual harvested power from the solar panels.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

3.6.4 CHARGING AND DISCHARGING CONTROLLERS

To protect the battery pack from damage due to over-voltage, over-current, over-temperature, the charging and discharging controllers with additional protections are required. Separation between charging and discharging paths makes it easier:

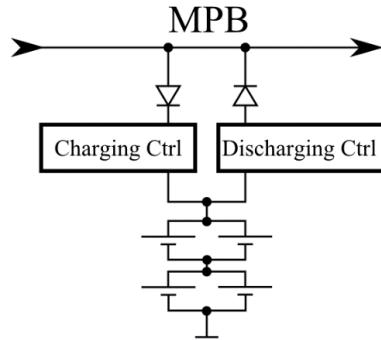


Figure 3-21. Charging and discharging paths

To increase efficiency ideal diodes shall be used.

Requirements for the charging controller:

Parameter	Value
Over-temperature protection	45°C with 5°C hysteresis
Charging voltage level	7.92V +/- 1% (WCA) at the battery pack - the voltage level shall be verified during the tests
Charging starts below	7.00V +/- 1% (or 7.20V) at the battery pack - the voltage level shall be verified during the tests
Short-circuit protection	2A +/- 20% (WCA) – the protection shall be verified during the tests
Charging process is stopping when the charging current drops below	150mA +/- 5% (or it can be 100mA) – the current should be verified during the tests

Table 3-11. Requirements for charging controller

Requirements for the discharging controller:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Parameter	Value
Short-circuit protection	2A +/- 20% (WCA)
Under-voltage protection	6.00V +/- 2% (WCA)

Table 3-12. Requirements for discharging controller

Charging and discharging controllers design:

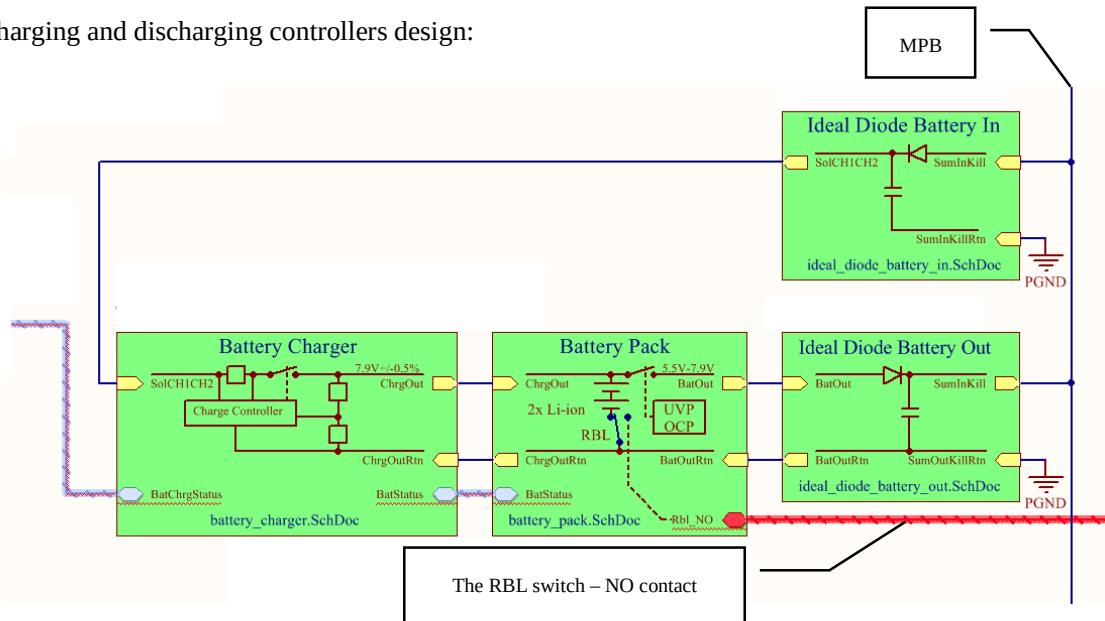


Figure 3-22. Charging and discharging controllers design

3.7 INPUT FILTER DESIGN FOR DCDC CONVERTERS

Each one of the DCDC power converters should have a well-designed input filter. We will use damped RLC filters. It prevents both electromagnetic interferences between power converters and it increase the stability of the system. The input filters will be designed according to [17].

The input filter suppress the differential mode noise.

There are three damping methods of an input LC filter. First damping method is shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

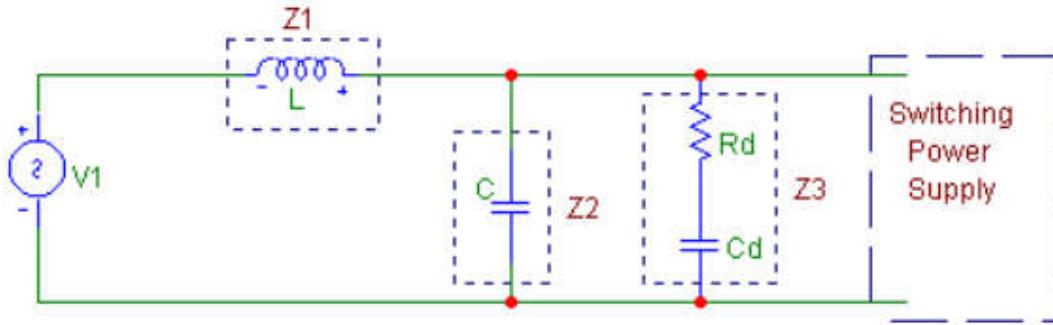


Figure 3-23. Parallel damped input filter – source [17]

The parallel damped method (R_d resistor is connected in series configuration with the C_d capacitor and the circuit is connected parallel to a damped filter) is very sensitive to large and rapid changes in voltage at the bus. When the voltage changes are rapid and large, the dissipated power at the R_d resistor is large.

Second damping method is shown below:

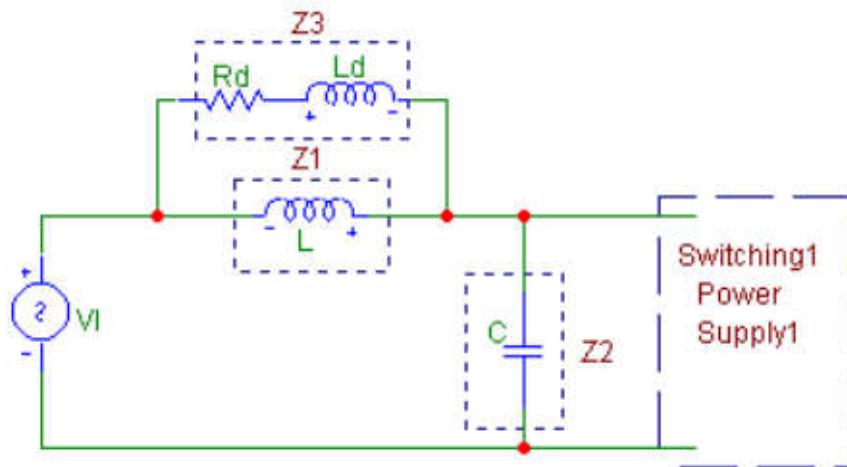


Figure 3-24. Series damped input filter – source [17]

The mixed method is present, when the series and the parallel damped methods are used simultaneously.

The series damping method was selected for both the MPPT and 3.3V/5V DCDC converters. If the output impedance of the filter will be too high, then the mixed method will be applied.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

The filters will be analysed using the LTSpice IV software from the Linear Technology company.

3.7.1 STABILITY PROBLEM OF DCDC CONVERTERS DUE TO INPUT FILTERS

Stability of any DCDC converter depends on both the input filter design and a feedback loop design. The input filter distorts the dynamic response of the DCDC converter. Effect of an input filter on the DCDC converter shall be both simulated and measured.

To achieve high stability of the DCDC converter, the output impedance of the input filter shall be lower than input impedance of the DCDC converter:

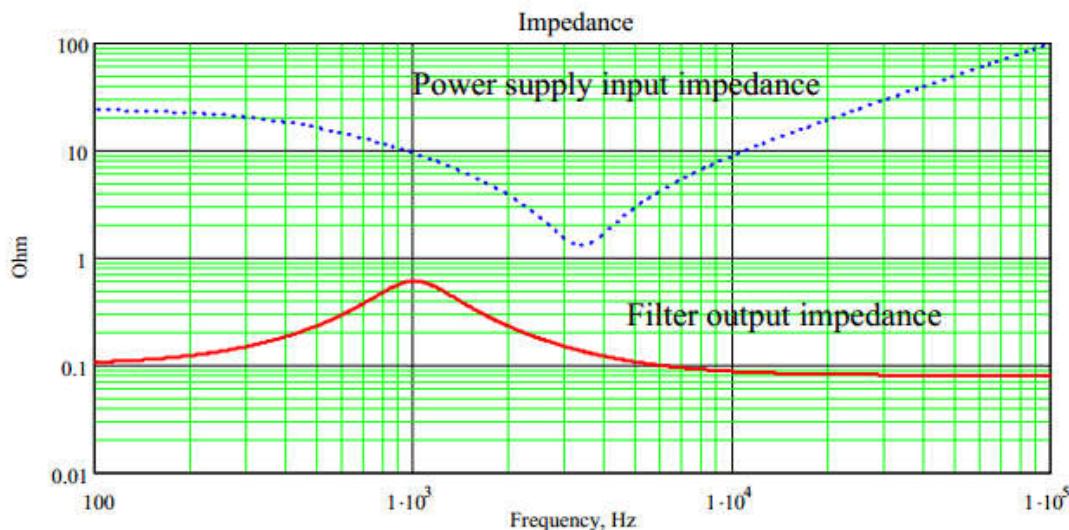


Figure 3-25. Separation of impedances – source [17]

Separation of these impedances is important for stability of the DCDC converter. The damped input filter makes it easier. Of course phase shift of the input filter is important and it will be analysed.

The impedance margins will be defined during the phase C.

3.8 FREQUENCY RESPONSE OF THE REGULATION LOOPS

The frequency response of the regulation loops of the all converters shall be both calculated and measured. The measurement setup is shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

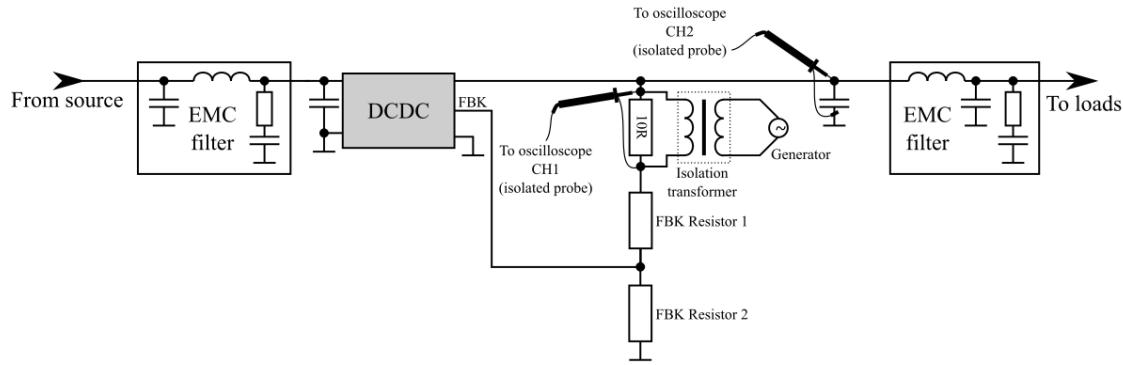


Figure 3-26. Stability test of the regulation loop

The gain margin and the phase margin of the regulation loops will be defined during the phase C.

To measure the frequency response we will use the AP300 Frequency Response Analyser from the Ridley company with the Differential Isolation Probes and the Ridley Universal Injector.

3.9 THE RBL CIRCUIT

The RBL circuit shall be able both to cut-off the battery pack and to cut-off the MPB from the output. The RBL circuit placed on the MPB can be used as the inrush-current limiter for the RBL switch and the deployment switch:

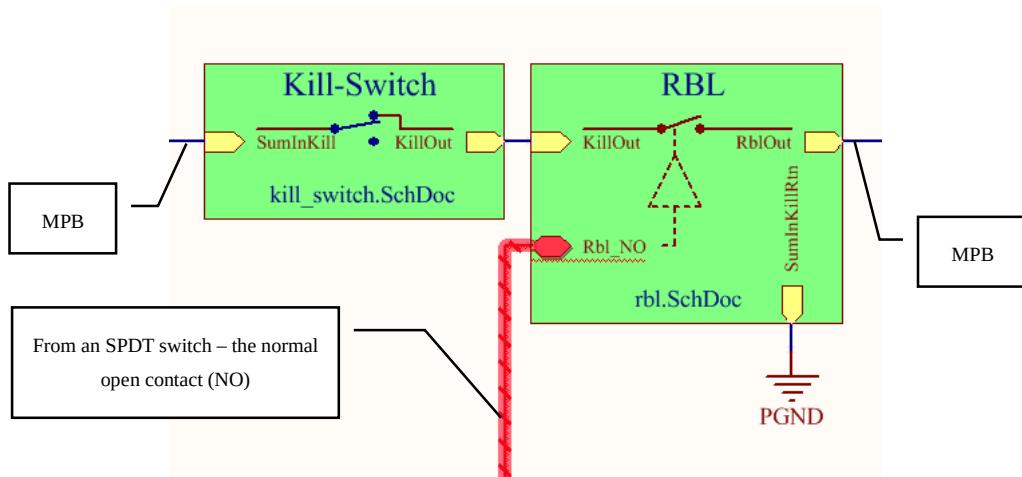


Figure 3-27. The RBL as the inrush-current limiter for the deployment switch

The part of the RBL which is responsible for to cut-off the battery pack is shown below:

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

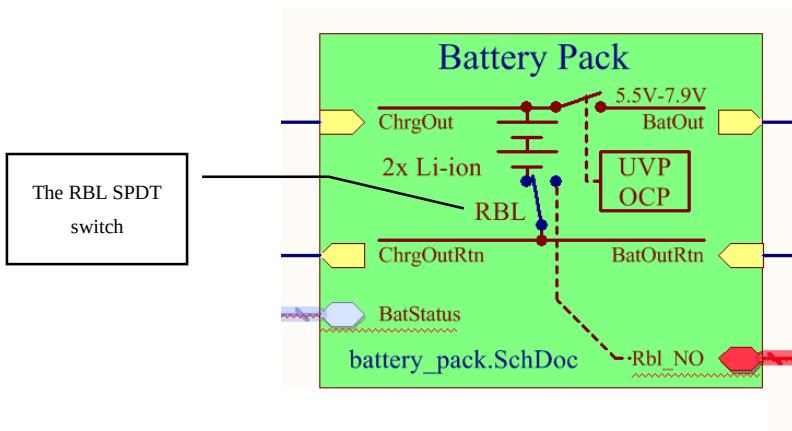


Figure 3-28. The RBL for the battery pack

The SPDT switch for the RBL circuit was selected and it is show below:



Figure 3-29. The RBL switch - Saia-Burgess F4T7Y1 - source TME.eu

The normal open contact (NO) of the switch will be connected to the MPB high-side switch, which is responsible to cut-off the MPB from the output. The normal close contact (NC) of the switch will be connected to the cold pin of the battery pack. The SPDT switch shall be redundant.

The cold pin of the battery is available on the battery pack PCB:

The inrush-current of the MPB and of the battery pack shall not exceed 5A. During the test of the system many on-off cycles of the RBL will be performed. Many cycles cannot damage for the SPDT switch.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

The RBL switch will be available at the Access Port on the X- side of the satellite. The RBL will be marked by the red label:



Figure 3-30. Remove Before Launch label

3.9.1 INRUSH-CURRENT LIMITERS FOR THE RBL AND THE DEPLOYMENT SWITCHES

The inrush-current limiters for the RBL and the deployment switches are necessary. The inrush-current limiter is placed within the RBL switch and it is shown below:

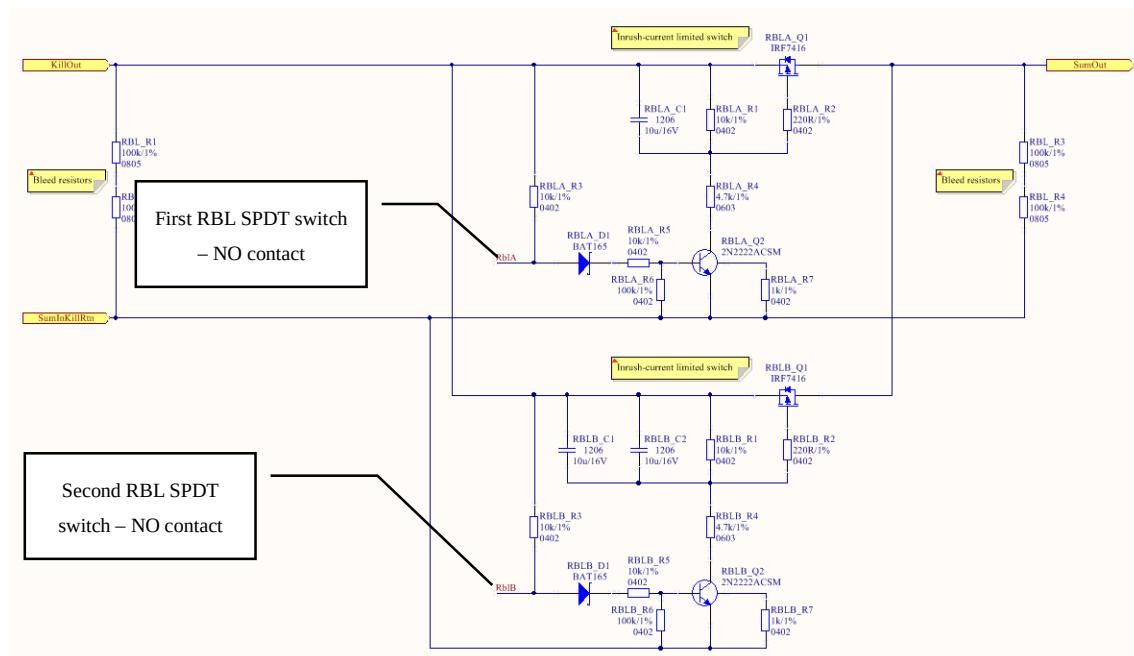


Figure 3-31. The RBL circuit

There are two separated inrush-current limiters. One of them is connected to first SPDT switch, second is connected to second SPDT switch.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

3.10 THE DEPLOYMENT SWITCH

The deployment switch is responsible for cut-off the MPB bus during the flight of the rocket. It is placed on the structure on rails. It will be realised by the SPDT switches. The SPDT switch is shown below:



Figure 3-32. The deployment switch - Saia-Burgess F4T7Y1 - source TME.eu SPDT

The switch will be redundant.

3.11 THE ACCESS PORT

The Access Port will be placed on the X- side of the satellite. At the Access Port will be available both the RBL switch and a connector for pre-launch testing. The connector for pre-launch testing will contain an external power and the internal I2C buses.

The proposed connector for pre-launch testing is shown below:

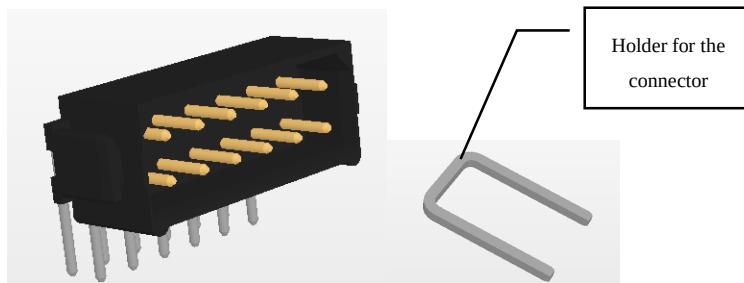


Figure 3-33. Harwin M80-8411242 for pre-launch testing

The Harwin M80-8411242 is a right angle, 2-rows, 12-ways connector. The connector will be placed on the Payload PCB and it will be available on the Access Port.

An electrical interface of the Access Port shall be short-circuit proof. The I2C interface shall be protected by an additional digital buffer.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

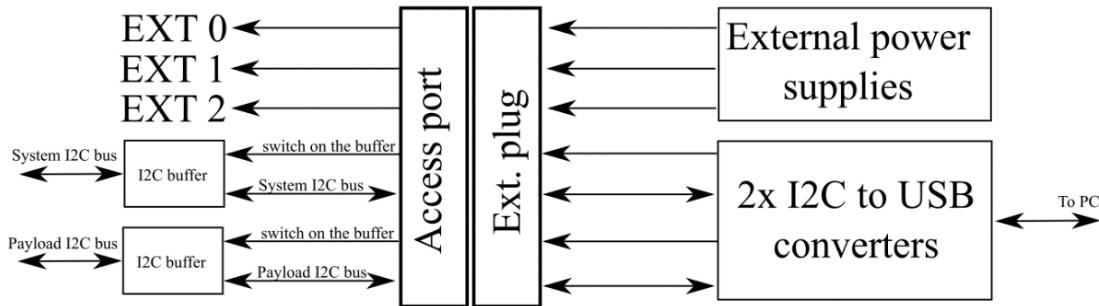


Figure 3-34. Block diagram of the Access Port

3.12 DCDC CONVERTERS FOR 3.3V AND 5V LINES

DCDC converters for the 3.3V and the 5V lines shall be placed within the EPS. The converters are responsible for supplying power for the satellite subsystems. The subsystems require protected and stabilized power lines. To protect the lines from the single point failure, the converters shall be redundant. Warm redundancy will be used.

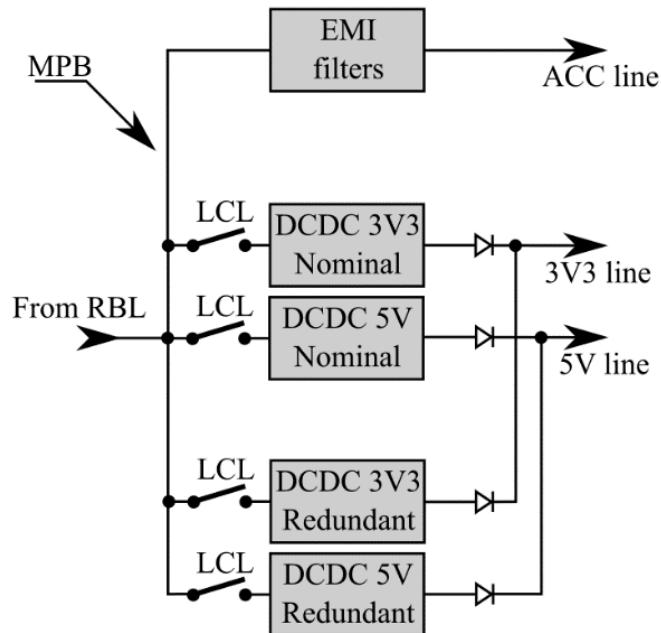


Figure 3-35. DCDC 5V and 3V3 topology

The converters will be protected by LCL switches. In the nominal mode the nominal converters are switched on, but the redundant converters are switched off. The LCLs are autonomous and they have an additional logic which is semi-independent of the main controllers. If the autonomous logic detects

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

any failure, then the logic switches off the nominal converter and the logic switches on the redundant converter. The 3V3 line and the 5V line are independent and they have independent protections.

The nominal converter is switched on (and the nominal converter is switched off), when:

- A voltage at the output of the nominal converter is lower than or higher than defined threshold value – an autonomous response,
- The main controller detects any failure and the controller sends commands to the logic - an autonomous response or a driven response,
- The GS team sends a command to the satellite, which triggers the logic – a driven response.

The procedures are not applicable for latch-up event. To protect from latch-up event, the LCLs shall contain auto-repeat circuits with period time around a few hundred milliseconds. If the main controller of the EPS detects too many auto-repeat periods in a short time, the main controller sends a command to the logic.

A nominal converter and a redundant converter are connected together through ideal diodes. The 3V3 line and the 5V line are decoupled by high-reliability capacitors. The capacitors are connected in mixed connections: series and parallel circuits. The method is used for the ACC line. It increases the reliability of the lines.

The MPB should be separated from the ACC line by an EMI filter. The EMI filter is responsible for both noise suppression and stability assurance of all DCDC converters. Output and input impedance of the EMI filter should be matched during the design process.

3.13 GROUNDING SCHEME

To prevent stray currents which are flown through a mechanical structure, the grounding scheme should be specified. The single point grounding scheme was selected. To align electric potentials (between the mechanical structure and a subsystem) during an assembling process, all subsystems will be connected to mounting holes through $1\text{k}\Omega$ resistors. Equivalent resistance of a path between a GND of each subsystem and mounting holes, should be equal to 1k . Only the PE net of the EPS will be connected to the mechanical structure through a single wire with a 0Ω path.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

4 PRELIMINARY RADIATION ANALYSIS

Detailed radiation analysis will be performed during phase C. This is only preliminary radiation analysis performed for an SSO orbit (LEO). Parameters of the analysis are show below:

- Circular 700km orbit, inclination 98°, SSO,
- The mission time: around 3 months,
- Equivalent of radiation shielding: 1mm of Al as a sphere.

4.1 GENERAL BACKGROUND

During the design process of the mission an influence of space environment on the spacecraft shall be analyzed. The main phenomenon which has influence on the electronics of spacecraft is ionizing radiation effect. There are three kinds of ionizing radiation sources:

- Cosmic rays – high energy radiation from outside of the Solar System,
- Solar wind – stream of plasma released from the upper atmosphere of the Sun,
- Trapped and charged particles – high energy protons and electrons trapped in the Van Allen belts.

4.2 RADIATION EFFECTS ON ELECTRONICS

There are two main kinds of radiation effects on electronics:

- Total Ionization Dose (TID) effects – some parameters of electronic components are degraded during a long time. The units which are used to measure the TID are Rad or Gray. The TID level should be determined for most components within the EPS.
- Single Event Effects (SEE) – a high ionization radiation dose deposited in a short time. Some parameters of components are degraded in a one moment but some components can be destroyed. Linear Energy Transfer Threshold (LET_{th}) level determines the immunity of the component on the SEE.

4.3 SOUTH ATLANTIC ANOMALY

The radiation effect higher than usual is present within the SAA anomaly (South Atlantic Anomaly). For example the Hubble Space Telescope is switched off within the SAA anomaly. To prevent from damage of SEE effects, most subsystems of PW-Sat2 should be switched off within the SAA anomaly.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

For trapped proton and electron populations simulations the AP-8 and AE-8 models were used. The models were developed by NASA.

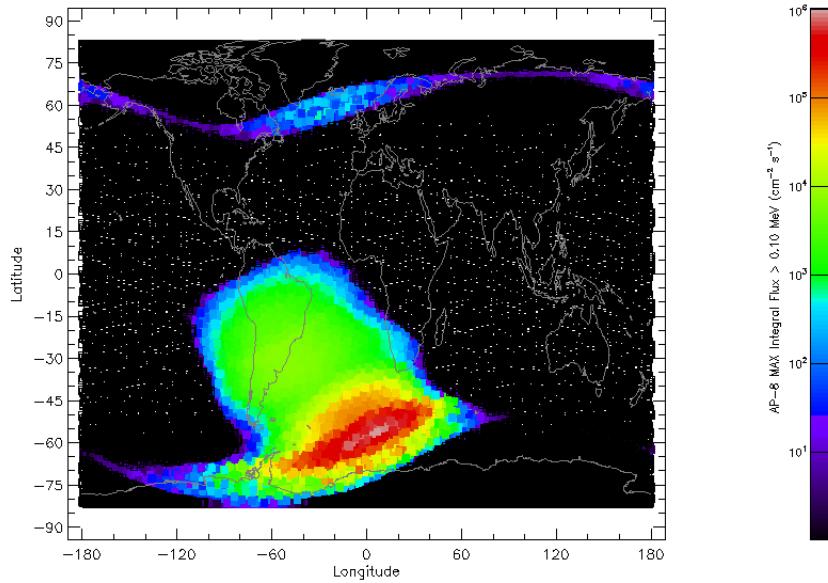


Figure 4-1. Trapped protons flux above 1MeV on 700km SSO orbit – SPENVIS software from ESA

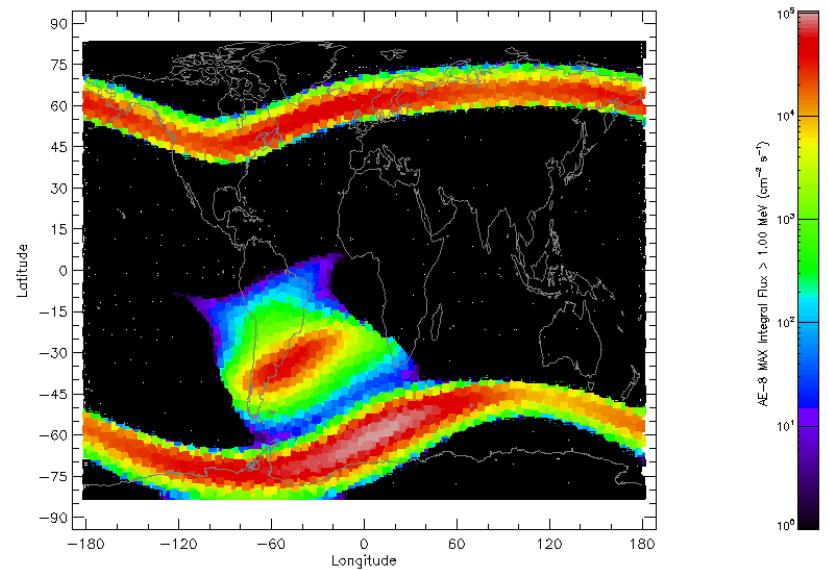


Figure 4-2. Trapped electrons flux above 1MeV on 700km SSO orbit – SPENVIS software from ESA

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

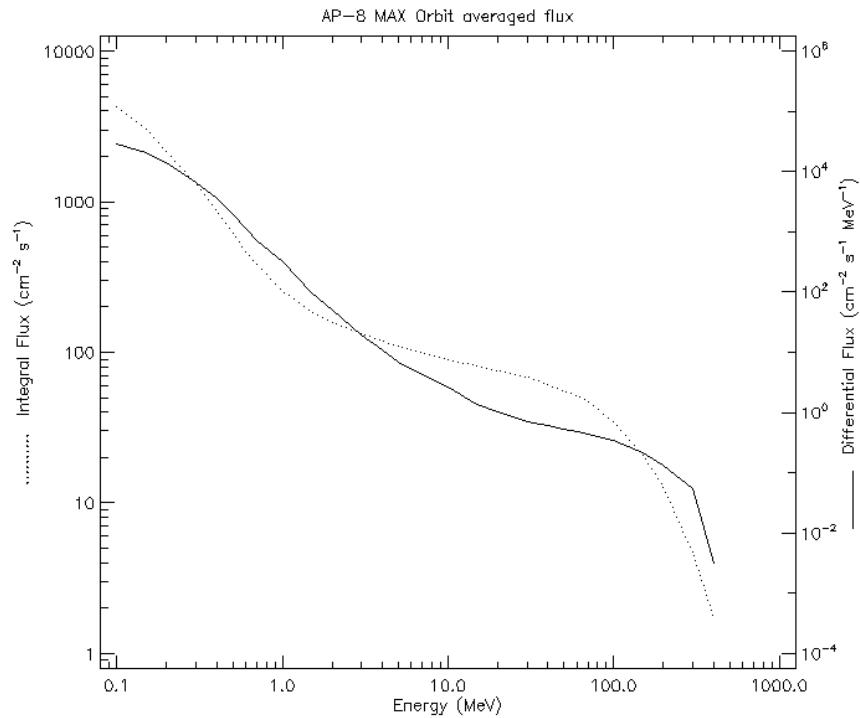


Figure 4-3. Averaged spectra of trapped protons on 700km SSO orbit – SPENVIS software from ESA

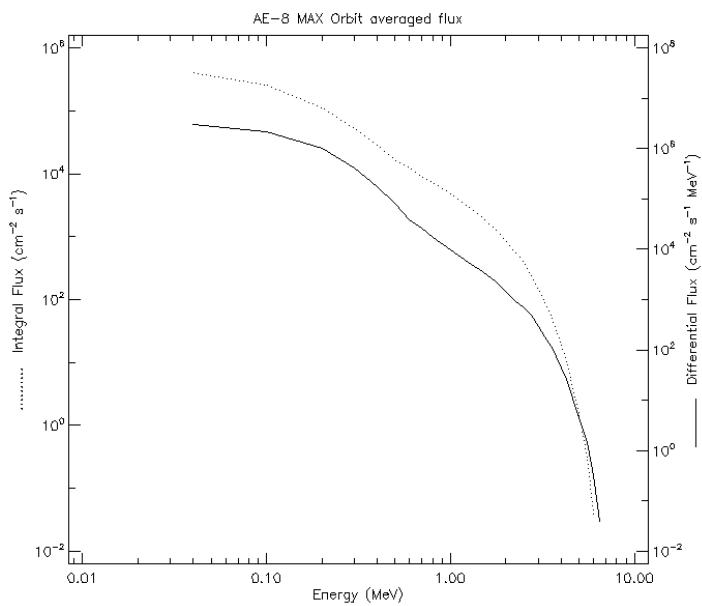


Figure 4-4. Averaged spectra of trapped electrons on 700km SSO orbit – SPENVIS software from ESA

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

4.4 ABSORBED TID LEVEL CALCULATION

Analysis of ionizing radiation dose as a function of shielding thickness was performed by the SPENVIS software from ESA. Results of the analysis are shown below:

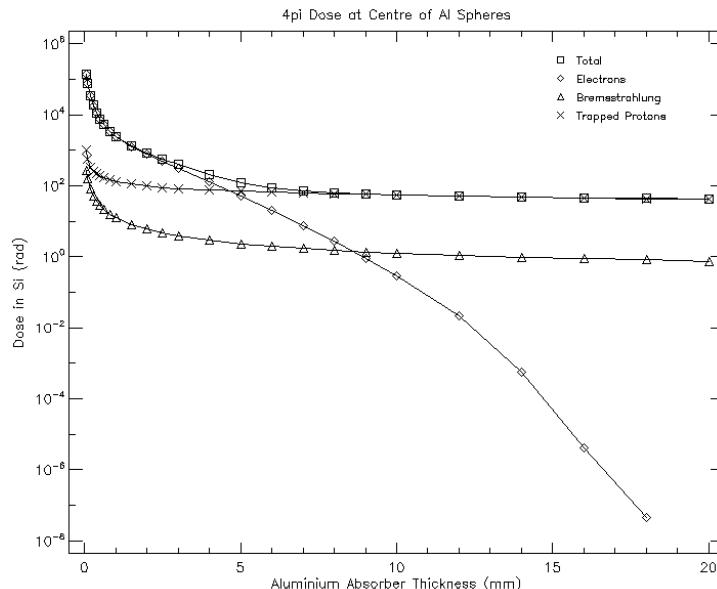


Figure 4-5. Radiation dose as a function of shielding thickness for the PW-Sat2 mission

Predicted total TID level for the mission (target material: Si; thickness of shielding: 1mm; shield configuration: Centre of Al sphere) is around 2.5kRad. Components with the TID level above 5kRad should be used. Most industrial components can withstand the TID level. Consequently, an additional radiation shielding is not necessary for the mission.

4.5 METHODS OF PROTECTION FROM RADIATION EFFECTS

To protect from TID effects, the TID tested components should be used (if possible). Many TID tests were performed by members of IEEE organization, NASA, ESA, TRAD, JAXA, etc. We will refer to the tests.

To protect from SEE effects we will use:

- LCL protections for all active components (microcontrollers, power components),
- To decrease SEE probability, components with high LET level should be used,
- ECC of RAM, Flash (if possible), FRAM,

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

- Segmentation of all memories and cyclic testing,
- Redundancy of critical data within Flash/FRAM memories,
- Switch off most components within the SAA anomaly.

	PW-Sat2	Preliminary Design Review			
	2015-05-23	Electrical Power System			
	Phase B				

5 COMPONENTS SELECTION

All components shall be selected with great care and great caution. The space environment is very demanding for the components. First, some parameters of the components shall be derated in conformance with [4] standard. Second, a radiation immunity of the components should be analyzed. Third, a reliability of the components shall be analyzed.

We decided that most components within the EPS should be radiation tested and all components shall to have a known reliability level.

5.1 LOW POWER AND THIN FILM SMD RESISTORS

Resistors with 0402, 0603, 0805 and 1206 form factors with known the failure-rate level are necessary. Resistors CRCW series from Vishay company were selected.

Data for WCA/PSA analysis (and more):

TECHNICAL SPECIFICATIONS									
PARAMETER	UNIT	D10/ CRCW0402	D11/ CRCW0603	D12/ CRCW0805	D25/ CRCW1206	CRCW1210	CRCW1218	CRCW2010	CRCW2512
Rated dissipation P_{70} ⁽¹⁾	W	0.063	0.1	0.125	0.25	0.5	1.0	0.75	1.0
Limiting element voltage U_{max} AC/DC	V	50	75	150	200	200	200	400	500
Insulation voltage U_{ins} (1 min)	V	> 75	> 100	> 200	> 300	> 300	> 300	> 300	> 300
Insulation resistance	Ω	$> 10^9$							
Category temperature range	$^{\circ}\text{C}$	- 55 to + 155							
Failure rate	h^{-1}	$< 0.1 \times 10^{-9}$							
Weight	mg	0.65	2	5.5	10	16	29.5	25.5	40.5

Table 5-1. CRCW series resistors from Vishay company

Stability $\frac{\Delta R}{R}$ is equal to 1% for 1000h at 70°C.

Selected tolerance: at least 1%.

Selected temperature coefficient: at least $\pm 100\text{ppm/K}$.

Qualification: AEC-Q200 - Automotive Electronics Council-Q200, Stress Test Qualification for Passive Components.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Procurement of the resistors: Farnell/Digikey. The resistors will be used both for EM (engineering model) and FM (flight model).

PART NUMBER AND PRODUCT DESCRIPTION											
Part Number: CRCW0603562RFKEC											
C	R	C	W	0	6	0	3	5	6	2	R
MODEL	VALUE	TOLERANCE	TCR	PACKAGING	SPECIAL						
CRCW0402 CRCW0603 CRCW0805 CRCW1206 CRCW1210 CRCW1218 CRCW2010 CRCW2512	R = Decimal K = Thousand M = Million 0000 = Jumper	F = ± 1.0 % J = ± 5.0 % Z = Jumper	K = ± 100 ppm/K N = ± 200 ppm/K 0 = Jumper	EA, EB, EC, ED, EE, EF, EG, EH, EI, EL, EK	Up to 2 digits						
Product Description: D11/CRCW0603 100 562R 1% ET6 e3											
D11/CRCW0603	100	562R	1%	ET6	e3						
MODEL	TCR	RESISTANCE VALUE	TOLERANCE	PACKAGING	LEAD (Pb)-FREE						
D10/CRCW0402 D11/CRCW0603 D12/CRCW0805 D25/CRCW1206 CRCW1210 CRCW1218 CRCW2010 CRCW2512	± 200 ppm/K ± 100 ppm/K	10R = 10 Ω 562R = 562 Ω 10K = 10 kΩ 1M0 = 1 MΩ 0R0 = Jumper	± 5 % ± 1 %	ET1, ET2, ET3, ET4, ET5, ET6, ET7, ET8, ET9, EF4, E02, E67, E82	e3 = Pure tin termination finish						

Table 5-2. CRCW resistors from Vishay - part numbers

5.2 SMD CERAMIC CAPACITORS

Capacitors with 0402, 0603, 0805 and 1206 form factors with known failure-rate level are needed. COTS capacitors from KEMET company were selected..

C	1210	T	104	K	5	R	A	C	TU
Ceramic	Case Size (L' x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance	Voltage	Dielectric	Failure Rate/Design	Termination Finish ¹	Packaging/Grade (C-Spec) ²
0402	T = COTS	2 significant digits + number of zeros	J = ±5% K = ±10% M = ±20%	9 = 6.3 V 8 = 10 V 4 = 16 V 3 = 25 V 5 = 50 V 1 = 100 V 2 = 200 V A = 250 V	R = X7R	A = Testing per MIL-PRF-55681 PDA 8% B= Testing per MIL-PRF-55681 PDA 8%, DPA per EIA-469 C = Testing per MIL-PRF-55681 PDA 8%, DPA per EIA-469, Humidity per MIL-STD-202, Method 103, Condition A	C = 100% Matte Sn L = SnPb (5% minimum)	Blank = Bulk TU = 7" Reel Unmarked TM = 7" Reel Marked	
0603									
0805									
1206									
1210									
1812									
2220									

Table 5-3. KEMET COTS ceramic capacitors - ordering information

Procurement of the capacitors: Digikey. The capacitors will be used only for FM model. For EM model we will use replacements of the capacitors.

5.3 SOLID TANTALUM SMD CAPACITORS

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Solid tantalum Hi-Rel COTS capacitors from Vishay company were selected.

ORDERING INFORMATION									
T83	D	107	K	010	E	A	A	S	
TYPE	CASE CODE	CAPACITANCE	CAPACITANCE TOLERANCE	DC VOLTAGE RATING AT +85 °C	TERMINATION AND PACKAGING	RELIABILITY LEVEL	SURGE CURRENT	ESR	
See Ratings and Case Codes table.	This is expressed in picofarads. The first two digits are the significant figures. The third is the number of zeros to follow.	K = ± 10 % M = ± 20 % J = ± 5 % (special order)	This is expressed in volts. To complete the three-digit block, zeros precede the voltage rating. A decimal point is indicated by an "R" (6R3 = 6.3 V).	See table Termination and Packaging Codes	A = 1.0 % B = 0.1 % C = 0.01 % S = hi-rel standard Z = non-ER	A = 10 cycles at +25 °C B = 10 cycles at -55 °C / +85 °C C = 10 cycles at -55 °C / +85 °C (before Weibull grading) Z = none S = 3 cycles at +25 °C	S = std L = low		

Table 5-4. Solid tantalum COTS capacitors from Vishay – ordering information

Selected reliability level: at least 0.1%.

Procurement of the capacitors: Digikey. The capacitors will be used only for FM model. For EM model we will use replacements of the capacitors.

5.4 IDEAL DIODE CONTROLLER

The ideal diode controllers are used for:

- Power harvesting from solar panels,
- Power summing to the MPB,
- Current paths separation for charging and discharging controllers for the battery pack,
- Power summing for redundant converters for 5V and 3V3 lines.

5.4.1 REQUIREMENTS FOR IDEAL DIODE CONTROLLER

Requirements for the ideal diode controller:

- The controller controls an external P-MOSFET – no charge pumps,
- Voltage range: at least from 3V,
- Manual control input,
- Small package,
- Radiation tests or space heritage.

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

5.4.2 IDEAL DIODE CONTROLLER SELECTION

For example, originally the LTC4412 was selected as the ideal diode controller for the ESTCube-1 satellite (power harvesting for solar panels [18]). Finally the LTC4352 controller was selected for the ESTCube-1 satellite [15].

Due to integrated charge pump within LTC4352, we rejected the controller. LTC4412 ideal diode controller from Linear Technology was selected for the PW-Sat2 satellite.

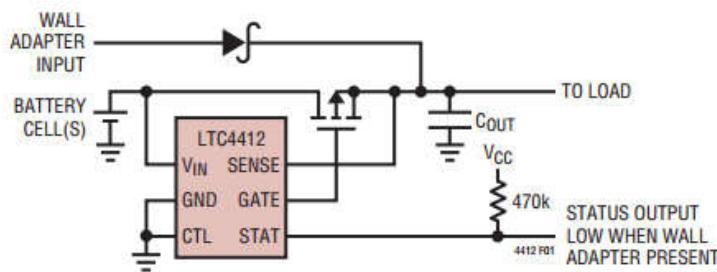


Figure 5-1. LTC4412 from Linear Technology - typical application

The ideal diode controller is available in a military plastic version: LTC4412MPxx. The military plastic version has a wider temperature range: -55°C to 150°C.

Procurement of the military version of the LTC4412 for the FM model: Digikey.

The ideal diode controller shall be protected from a destructive latch-up.

5.4.3 MOSFET FOR IDEAL DIODE CONTROLLER

The LTC4412 ideal diode controller requires an external P-MOSFET.

Requirements for the P-MOSFET:

- Small package, for example SO-8,
- V_{DS} at least 25V,
- V_{th} lower than 1.5V,
- Continuous drain current: at least 5A,
- $R_{DS(ON)}$ lower than $40m\Omega$ - it was calculated according to the ideal diode datasheet,
- Radiation tests – TID.

IRF7416 from International Rectifier was selected. The MOSFET is packed in the SO-8 package.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-10	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-7.1	
I_{DM}	Pulsed Drain Current ①	-45	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	370	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Table 5-5. Parameters of the IRF7416 from datasheet – International Rectifier company

Drain-to-source breakdown voltage $V_{DS} = -30\text{V}$ and minimum gate threshold voltage $V_{GS(\text{th})} = -1.0\text{V}$. $R_{DS(\text{ON})}$ is between to $20\text{m}\Omega$ and $35\text{m}\Omega$.

Radiation test results are shown below (source [19]):

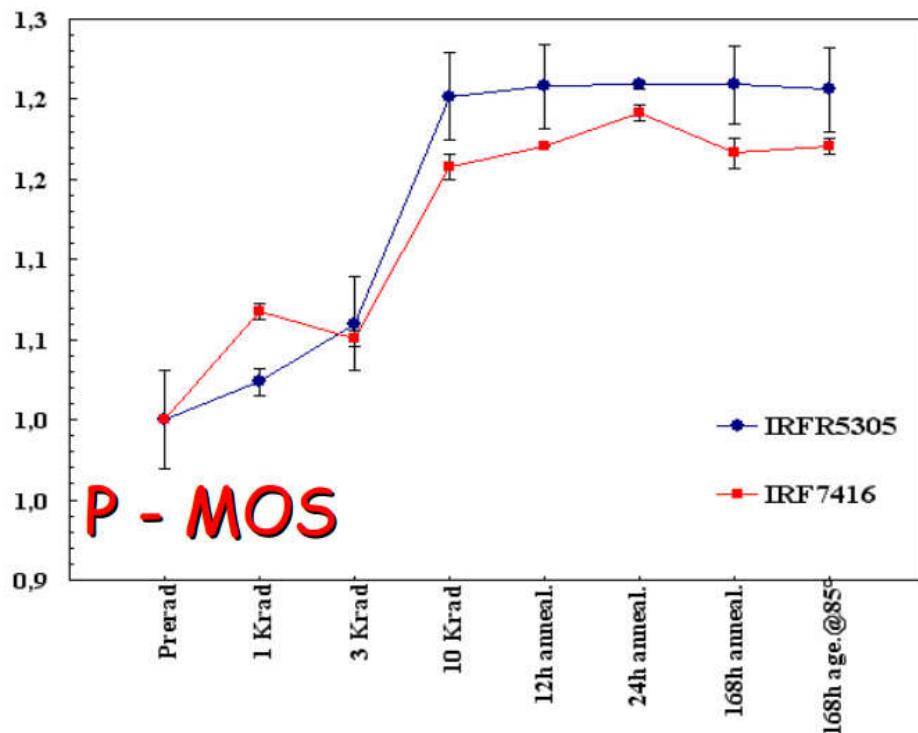


Figure 5-2. V_{th} relative variation of the IRF7416 – source [19]

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

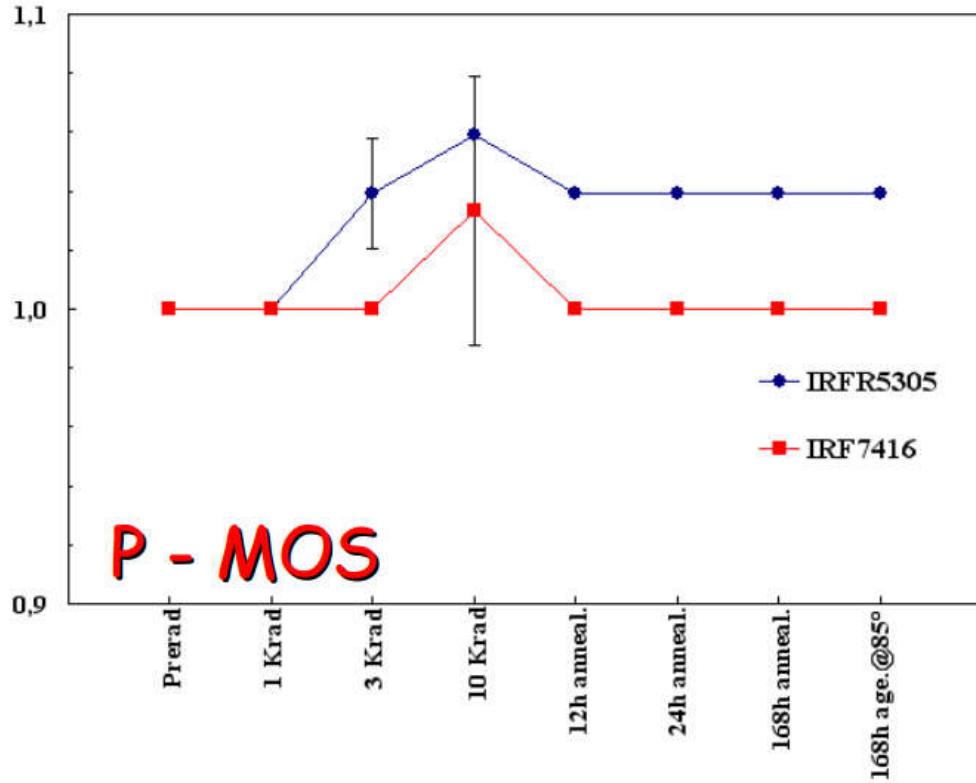


Figure 5-3. R_{DS(ON)} relative variation of the IRF7416 – source [19]

Generally the $R_{DS(ON)}$ is very stable within 10% and the V_{th} voltage is stable within 20%, when the TID value is equal to 10kRad.

5.5 BOOST CONVERTER

A boost converter is placed between solar panels at X sides (two-cells panels) and the MPB bus. It will be driven by an MPPT controller. Requirements for the boost converter are shown below:

Parameter	Values
Operating input voltage range	Min. from 3V to 8V (derated in conformance with [4])
Output voltage range	Min. from 6.5V to 15V (derated in conformance with [4])
Switching frequency	Min. 500kHz
Integrated power switch	Min. 0.6A (derated in conformance with [4])
Under voltage protection	To protect from transient states at low voltages

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Soft-start	To decrease inrush currents
Temperature range	Min. industrial temperature range: -40°C to 85°C
Small package	Max. SO package
Over current protection	It is not necessary
Over temperature protection	To protect from overheat

Table 5-6. Requirements for boost converter

The LT3580MPMS8E from Linear Technology was selected. The converter uses constant-frequency, current mode control scheme and it is offered in MP (military plastic) grade, where the MP-grade operates with a junction temperature range of -55°C to 125°C. The converter can be used as a COTS component for harsh military applications [20].

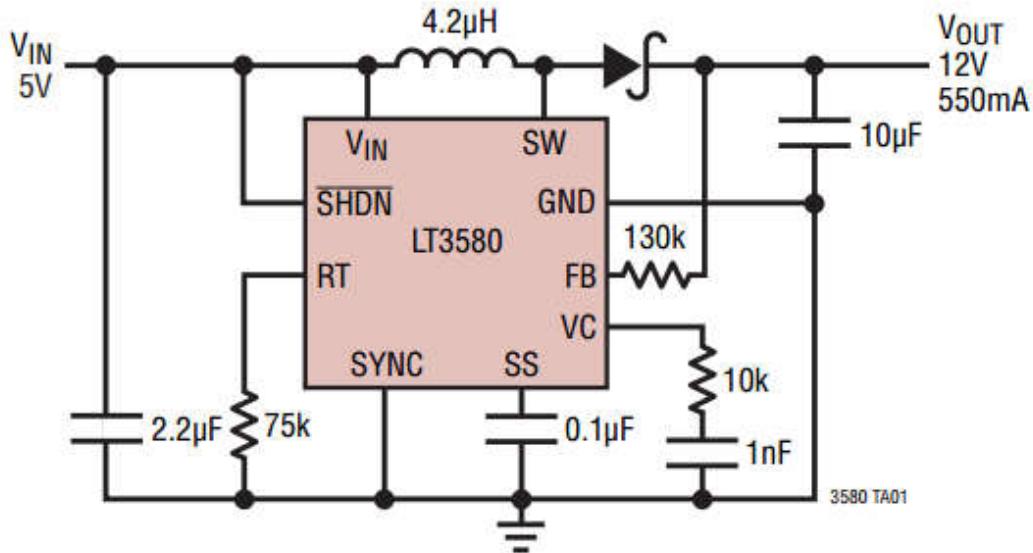


Figure 5-4. LT3580 converter from Linear Technology - typical application

The converter will be controlled by an external DAC converter. It was checked by simulations and we know that it is possible.

The TSSOP package was selected. The package has a thermal pad which is placed on the bottom side of the package. It will be soldered to the PCB and it increases the thermal contact to the PCB.

Procurement of the military plastic version of the LT3580 for the FM model: Digikey.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.6 BUCK-BOOST CONVERTERS

Buck-boost converters will be placed between solar panels, which are mounted on solar wings, and the MPB bus. The converters will be controlled by separate MPPT controllers. Requirements for the converters are shown below:

Parameter	Values
Operating input voltage range	Min. from 6V to 18V (derated in conformance with [4])
Output voltage range	Min. from 6.5V to 15V (derated in conformance with [4])
Switching frequency	Min. 500kHz
Integrated power switch	Min. 1.2A at step-down operations (derated in conformance with [4]). The current at step-up operations can be smaller, but a built-in over current protection is necessary
Under voltage protection	To protect from transient states at low voltages
Soft-start	To decrease inrush currents
Temperature range	Min. industrial temperature range: -40°C to 85°C
Small package	Max. SO package
Over current protection	Needed
Over temperature protection	To protect from overheating

Table 5-7. Requirements for buck-boost converters

The LTC3115MPFE from Linear Technology was selected. This is a monolithic synchronous buck-boost converter which is offered in MP (military plastic) grade. The converter can be used as a COTS component for harsh military applications [20].

The converter will be controlled by an external DAC converter. It was checked by simulations and we know that it is possible.

The TSSOP package was selected. The package has a thermal pad which is placed on the bottom side of the package. It will be soldered to the PCB and it increases a thermal contact to the PCB.

	PW-Sat2 2015-05-23 Phase B	Preliminary Design Review Electrical Power System	
---	----------------------------------	--	---

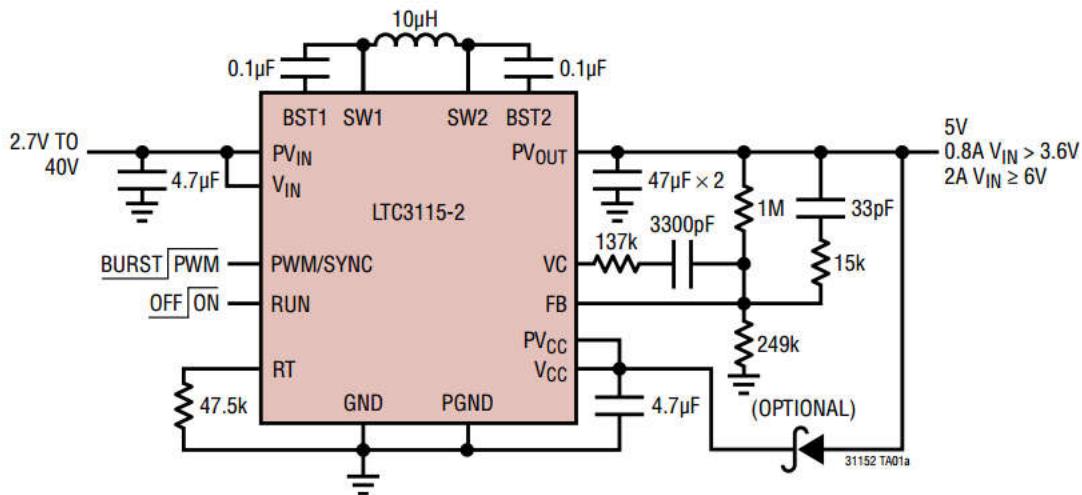


Figure 5-5. LTC3115 converter from Linear Technology - typical application

Procurement of the military plastic version of the LTC3115 for the FM model: Digikey.

5.7 DCDC CONVERTERS FOR 3V3 AND 5V LINES

The converters convert the power from the MPB bus to the distribution module. Next, the power is distributed to subsystems. Requirements for the converters are shown below:

Parameter	Values
Operating input voltage range	Min. from 6V to 15V (derated in conformance with [4])
Output voltage range	3.3V and 5V with some margins
Switching frequency	Min. 500kHz
Integrated power switch	Min. 1.5A for 5V line (derated in conformance with [4])
	Min 0.5A for 3.3 line (derated in conformance with [4])
Under voltage protection	To protect from transient states at low voltages
Soft-start	To decrease inrush currents
Temperature range	Min. industrial temperature range: -40°C to 85°C
Small package	Max. SO package
Over current protection	Needed

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Over temperature protection	To protect from overheating
-----------------------------	-----------------------------

Table 5-8. Requirements for DCDC converters for 3V3 and 5V lines

Both for 3V3 and 5V lines the TPS5430DDA converter from Texas Instruments was selected. The converter is a PWM converter that integrates a N-channel MOSFET (unfortunately it has a built-in charge pump but it has performed radiation tests by IEEE members). Additionally the converter is described as an Enhanced Product in the Defense Guide from Texas Instruments corporation [21].

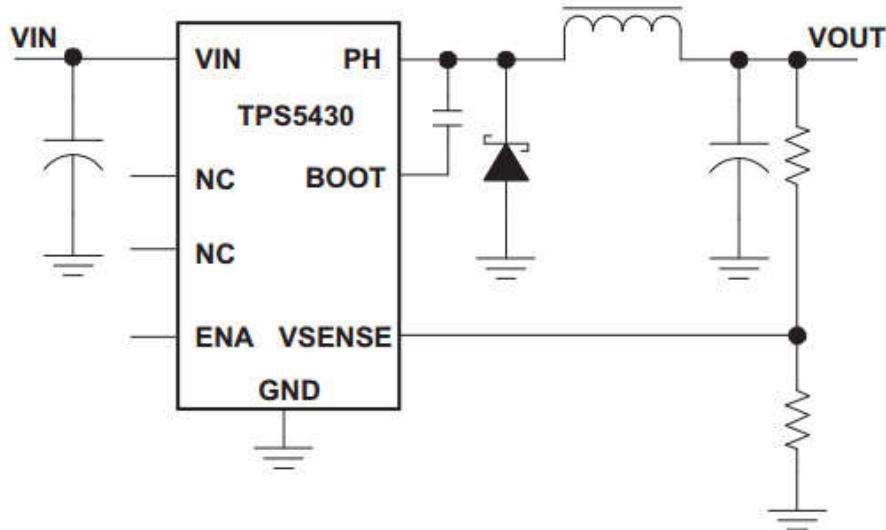


Figure 5-6. TPS5430 from Texas Instruments - simplified schematic

Radiation analysis were performed for the TPS5420 converter by IEEE members. The component is similar to the TPS5430 converter (the TPS5430 has a thermal pad placed on the bottom side of the package – it increases a thermal contact to the PCB). Radiation analysis of the TPS5420 is shown below (source [22]):

Manufacturer	LDC	Technology/ Device Function	Facility/Date/PI	Summary of Results	App. Spec. Test (Y/N)	Dose rate (rads(Si)/s)	Deg. Level (krads (Si))
Texas Instruments	7AKDKE5	BiCMOS/ Voltage Regulator	08MAR:DC	$15 < V_{ENABLE} < 20$ krads(Si). Parts failed to turn on after 20 krads(Si).	Y	9	15-20

Figure 5-7. Radiation analysis for the TPS5420 – source [22]

Summarizing,, the selected converter can withstand a TID level which is lower than 15kRad (when the dose rate is equal to 9Rad/s).

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

5.8 LCL FOR ACC AND 5V LINES

The LCL switches will be responsible for switching on the load to the MPB bus and the load to the 5V bus. Requirements for the LCL:

- Threshold current of the protection shall be regulated from 0.5A to 2A,
- Operating voltage: 3V to 12V,
- Under voltage protection,
- Protection from hard-short-circuit,
- Temperature range: at least industrial range from -40°C to 85°C,
- Possibility to switch on or switch off a load (EN input).

The FPF270xMX from Fairchild Semiconductor was selected. This is a current-limiting load switch that provide protection to systems and loads from excess current conditions. Current limit is adjustable by an external resistor from 0.4A to 2A. Switches with auto-restart time are available too.

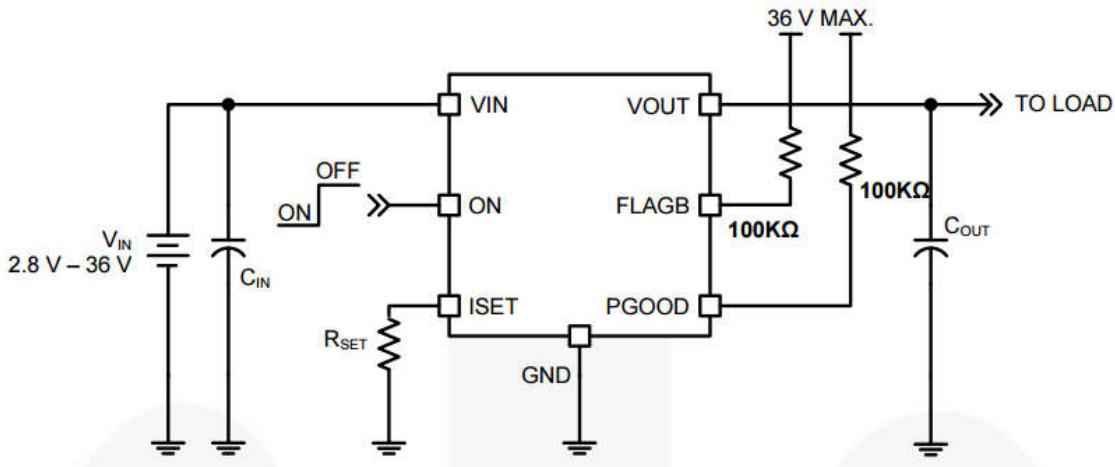


Figure 5-8. FPF270xMX from Fairchild Semiconductor – typical application

Radiation tests of the FPF2700 were performed by a IEEE members (source [23]) . The tests were performed at the University of Massachusetts Lowell Radiation Laboratory using a high-dose rate Cobalt-60 gamma source. Results of the tests are shown below:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

DUT	Dose	I_{trip} (A)	R_{ON} (mΩ)	V_{OFF} (mV)	I_Q (μA)
#1	0 krad	0.447	162	2.1	92
#1	8 krad	0.442	90	0.8	89
#2	0 krad	0.509	156	1.6	92
#2	24 krad	0.505	77.2	1.5	105

Figure 5-9. Radiation analysis of the FPF2700 – IEEE [23]

The tests were performed for the MicroMASS mission (Micro-sized Microwave Atmospheric Satellite – 3U cubesat satellite). The FPF2700 successfully passed the radiation tests for the mission. Of course, the IC is a good option for the PW-Sat2 satellite.

The SO-8 package was selected.

Procurement of the FPF270x: Farnell/Digikey/Mouser.

5.9 LCL FOR 3V3 AND 5V LINES – LOW CURRENT APPLICATIONS

The LCL switches will be responsible for switching on the load to the 3V3 and 5V lines at low currents. The FPF2700 can switch on the load from 0.4A. Requirements for the low-current LCL:

- Threshold current of the protection shall be regulated from 0.1A to 0.5A,
- Operating voltage: 3.3V range and 5V range,
- Under voltage protection,
- Protection from hard-short-circuit,
- Small package: SO, TSSOP, SOT-23 or smaller,
- Temperature range: at least industrial range from -40°C to 85°C,
- Possibility to switch on or switch off a load (EN input).

The TPS2551 switch was selected for our satellite. It has a heritage from the ESTCube-1 satellite mission [15].

The TPS2551 switch has a small package which is easy-to-use as current protection for microcontrollers, DACs, etc.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

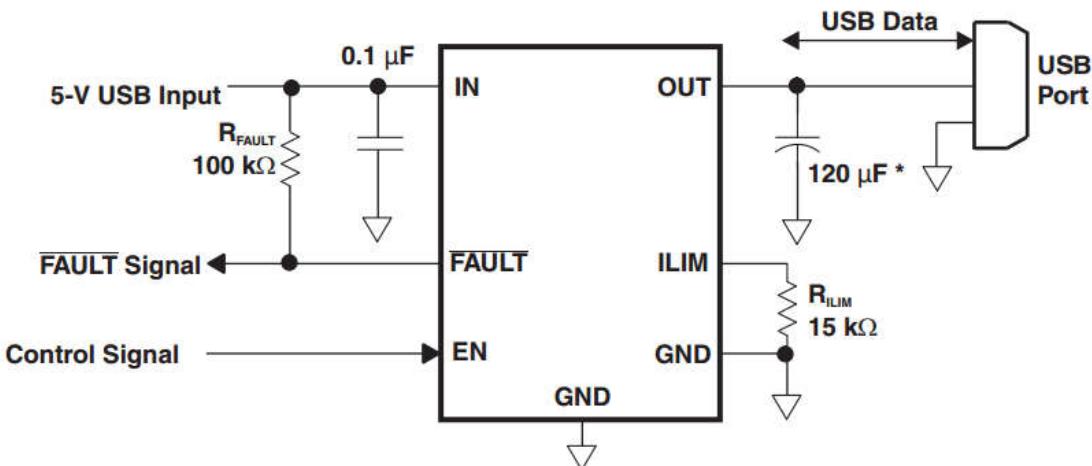


Figure 5-10. TPS2551 from Texas Instruments - typical application

Procurement of the TPS2551 switch: Farnell/Digikey/Mouser.

5.10 HIGH-SIDE CURRENT-SENSE AMPLIFIER

High-side current-sense amplifiers will be used for:

- Current measurement at inputs of MPPT converters,
- Currents measurement which are supplied to subsystem.

Requirements for the current-sense amplifiers:

Parameter	Values
Operating input voltage range	Min. from 2.8V to 15V
Supply method	External supply or from a measured bus
Type of output	Voltage output or current output
Measurement method	High-side on shunt-resistor
Small package	Max. SO package
Temperature range	At least industrial range from -40°C to 85°C
Gain of shunt's voltage	50V/V

Table 5-9. Requirements for high-side current-sense amplifiers

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

The MAX4372F from Maxim was selected. It is a high-side current-sense amplifier in a tiny, space-saving SOT23-5-pin package. It operates from 2.7V to 28V supply and consumes around 30uA.

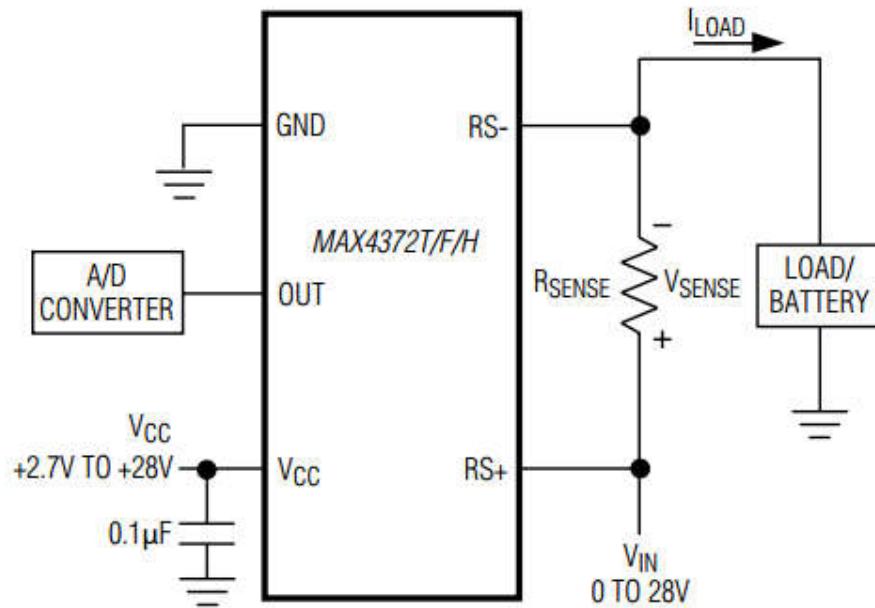


Figure 5-11. MAX4372 from Maxim - typical application

Radiation tests of the MAX4372 was performed by IEEE members [24]. During the tests no destructive events were observed:

Part Number	Manufacturer	Device Function	Test Facility	Results
MAX4372	Maxim	Current Sense Amplifier	LBL-HI	SETs observed > 9.74 MeV-cm ² /mg. . No destructive events observed > LET=58.78 Mev-cm ² /mg

Figure 5-12. Summary of radiation tests of MAX4372 – source [24]

The MAX4372 successfully pass TID level test equal to 30kRad – source [25]. The tests were performed to identified good candidates for use in the CMS end cap environment during HL-LHC operation.

Procurement of the MAX4372F amplifier: Farnell/Digikey/Mouser.

5.11 SMALL LDO REGULATOR

LDO regulators will be used:

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

- To supply microcontrollers within the EPS
- To supply other digital electronics within the EPS

Requirements for the LDO regulators:

Parameter	Values
Operating input voltage range	Min. from 2V to 15V
Output voltage	Fixed 3.3V or Adj
Output current	Min. 50mA
Small package	Max. SO package
Temperature range	At least industrial range from -40°C to 85°C
Protections	Over-current and over-temperature are necessary

Table 5-10. Requirements for LDO regulator

The LT1761MPS5-3.3 from Linear Technology was selected. The LDO regulator is capable of operating over an input voltage from 1.8V to 20V, and can supply 100mA of output current with a dropout voltage of 300mV. Military plastic (MP) grade was selected [20] with SOT23-5 package.

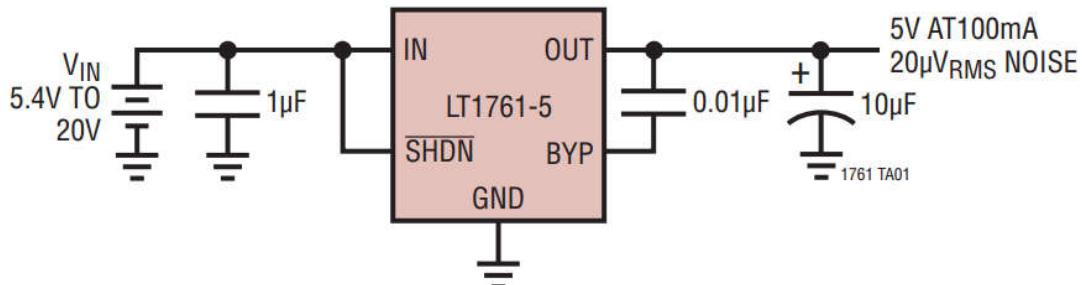


Figure 5-13. LT1761 from Linear Technology - typical application

To protect from a high-current latch-up path within the LT1761, an additional input resistor should be added (placed between a supply source and an input capacitor). A calculated short-circuit current should be higher than current limit threshold of the LT1761, but the current shall not be too high.

Procurement of the LT1761MPS5-3.3: Digikey.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.12 RESET SUPERVISORS

To protect digital electronics from transient states, additional reset supervisors shall be used. The supervisor is connected at the RESET line of digital electronics. Requirements for the reset supervisors:

Parameter	Values
Operating input voltage range	3.3V standard
Output type	<i>RESET</i> – open drain/collector
Small package	SOT-23
Temperature range	At least industrial range from -40°C to 85°C
Additional function	Manual reset

Table 5-11. Requirements for reset supervisors

The TPS3836L33 from Texas instruments was selected. It provides circuit initialization and timing supervision, primarily for digital electronics. During power on transient states can occur. The device prevents from this. The device was selected from Defense Guide From Texas Instruments [21].

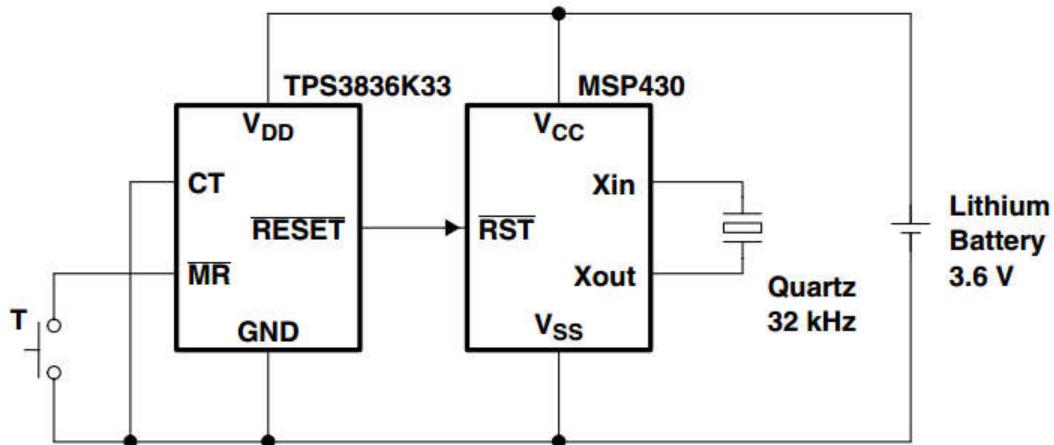


Figure 5-14. TPS3836 from Texas Instruments - typical application

Procurement of the TPS3836L33: Digikey/Farnell/Mouser.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.13 RESET SUPERVISORS WITH WATCHDOG

To protect digital electronics from transient states and infinity loops, additional reset supervisors with watchdog shall be used. Requirements for the reset supervisors with watchdog:

Parameter	Values
Operating input voltage range	3.3V standard
Output type	$\overline{\text{RESET}}$ – open drain/collector
Small package	SOT-23
Temperature range	At least industrial range from -40°C to 85°C
Additional function	Manual reset, watchdog

Table 5-12. Requirements for reset supervisors with watchdog

The TPS3813K33 from Texas Instruments was selected. It contains a reset supervisor and window-watchdog with programmable delay and window ratio. The device was selected from Defense Guide From Texas Instruments [21].

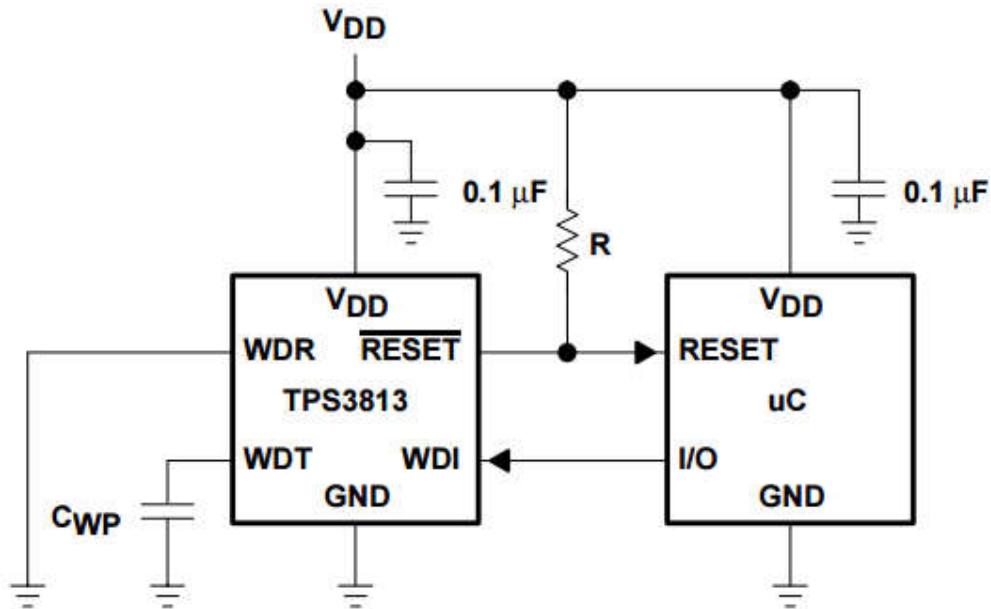


Table 5-13. TPS3813 from Texas Instruments - typical application

Procurement of the TPS3813K33: Digikey/Farnell/Mouser.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.14 SMALL POWER SCHOTTKY RECTIFIER DIODE

Small power Schottky rectifier diodes will be used:

- Within the MPPT boost converter,
- To supplying MPPT converters during the pre-flight testing,
- To decrease power losses on internal P-MOSFET diodes controlled by ideal diode controllers,
- Within the buck converters for 3V3 and 5V lines.

Requirements for power Schottky rectifiers:

Parameter	Values
Operating voltage	Min. 30V
Forward current	Min. 2A
Additional requirements	Suitable for DC/DC converters with switching frequency around 500kHz
Small package	For example SMB or SMC package
Operating temperature range	At least industrial range from -40°C to 85°C

Table 5-14. Requirements for Schottky rectifier diodes

The STPS340 from STMicroelectronics was selected. Diodes of the family are available in the European Preferred Parts List developed by ESA members [26].

Symbol	Parameter			Value	Unit
V_{RRM}	Repetitive peak reverse voltage			40	V
$I_{F(RMS)}$	Forward rms current			6	A
$I_{F(AV)}$	Average forward current	SMB	$T_L = 95 \text{ }^\circ\text{C} \delta = 0.5$	3	A
		SMC	$T_L = 105 \text{ }^\circ\text{C} \delta = 0.5$	3	A
I_{FSM}	Surge non repetitive forward current		$t_p = 10 \text{ ms sinusoidal}$	75	A
P_{ARM}	Repetitive peak avalanche power		$t_p = 1 \mu\text{s} \quad T_j = 25 \text{ }^\circ\text{C}$	1300	W
T_{stg}	Storage temperature range			-65 to +150	$^\circ\text{C}$
T_j	Operating junction temperature ⁽¹⁾ range			-40 to +150	$^\circ\text{C}$

Table 5-15. STPS340 from STMicroelectronics - absolute ratings

Both SMB and SMC packages will be used, depending from circuit.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.15 GENERAL PURPOSE ADC CONVERTER

External ADC converters will be used for:

- Voltages and current (as voltage at an output of the current sense amplifier) measurement within the distribution module,
- Voltages and current (as voltage at an output of the current sense amplifier) measurement at MPPT converters.

Requirements for the ADC converters:

Parameter	Values	
Operating voltage	3.3V range	
Digital interface	SPI based interface	
Resolution	12-bit	
Sample rate	>100sps	
ADC architecture	Not critically	
No. of analog inputs	For MPPT converters	4ch single ended
	For the distribution module	8ch single ended
Small package	Max. SO package	
Operating temperature range	At least industrial range from -40°C to 85°C	

Table 5-16. Requirements for external ADC converters

For MPPT converters the ADC124S021 from Texas Instruments was selected. For the distribution module the ADC128S022 from Texas Instruments was selected. These are low-power, CMOS ADCs converters specified for conversion throughput rates from 50ksps to 200ksps. The converters are based on a successive-approximation register (SAR) architecture with an internal track-and-hold circuits. The ADC124Sxxx is a four channel 12-bit ADC and the ADC128Sxxx is a eight channel 12-bit ADC. The converters operates with independent analog and digital voltage for 3.3V and 5V ranges. Digital supply shall be lower than analog supply. Analog supply is used as a reference voltage.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

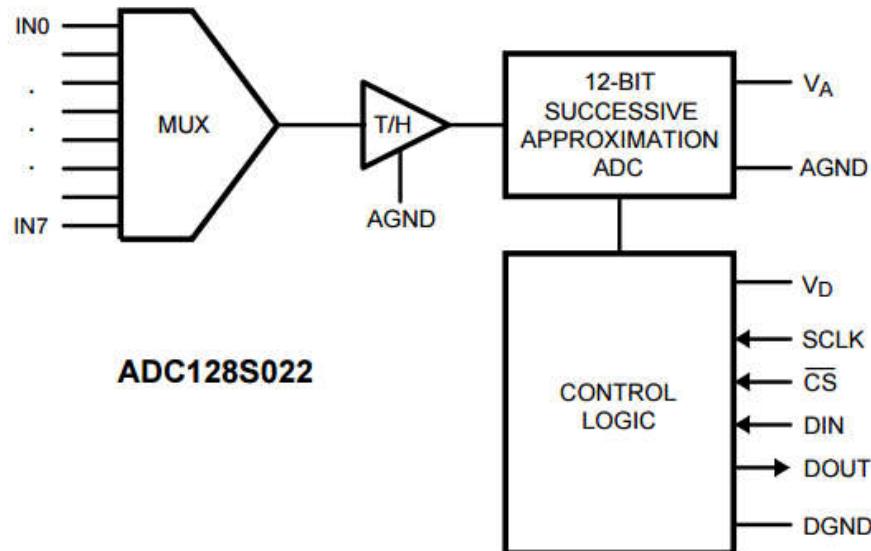


Figure 5-15. ADC128S022 from Texas Instruments - block diagram

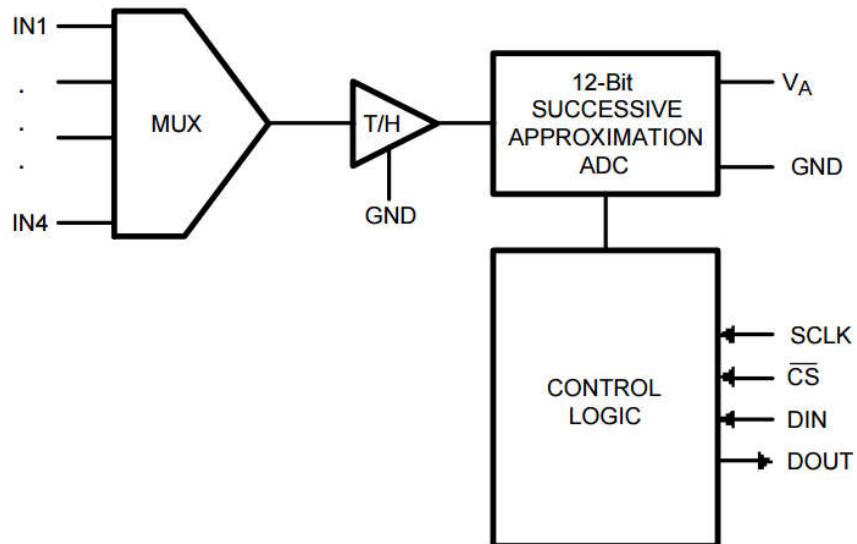


Figure 5-16. ADC124S021 from Texas Instruments - block diagram

The ADC128S022 (see [27]) is functionally and electrically similar to the QML version (see [28] and [29]) of the converter. The QML version is a space qualified component with determined TID and SEL levels. The QML version is specified to 100kRad in conformance with MIL-STD-883G standard. Probably the QML ICs have the same die like industrial version, but with different packages (FlatPack for QML version, TSSOP for industrial version).

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

To prevent damages of ADCs, some rules shall be respected:

- LCL for the ADC shall be added,
- Power shall be applied in the correct sequence,
- Digital and analogue supplies shall be separated.

We have some experience with ADC128Sxxx converters. We know that the additional digital buffer to a CLK line should be added (the converters are very fragile on slow and noisy edges).

Procurement of the ADC128S022 and the ADC124S021: Digikey/Farnell.

5.16 DAC CONVERTER FOR MPPT

DAC converter will be used to drive an MPPT converter. Requirements for the DAC converter:

Parameter	Values
Operating voltage	3.3V range
Digital interface	SPI based interface
Resolution	12-bit
Min. clock rate	100kHz
Output type	Rail-to-rail
No. of analog outputs	1
Small package	SOT23, TSOT23, etc.
Operating temperature range	At least industrial range from -40°C to 85°C

Table 5-17. Requirements for DAC converters

The DAC121S101 from Texas Instruments was selected. QML version [28] of the DAC is similarly to the DAC121S101. The QML version is specified to TID equal to 100kRad. Probably the QML ICs have the same die like industrial version, but with different packages.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

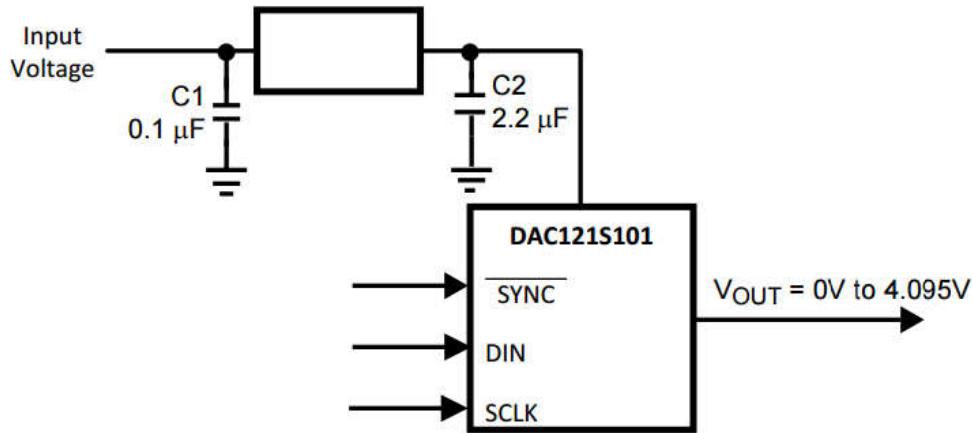


Figure 5-17. DAC121S101 from Texas Instruments - typical application

Procurement of the DAC121S101 and the DAC121S101: Digikey/Farnell.

5.17 MICROCONTROLLER SELECTION

In EPS microcontroller(s) will be responsible for MPPT (to control boost and buck-boost converters) and doing measurements of current/voltages in each channel – basic telemetry.

5.17.1 REQUIREMENTS

Requirements:

- due to it is low usage (basic calculations does not take much processor time) it should allow for under-clocking for lower power consumption,
- low starting voltage (preferably 1.8V),
- I²C (slave) interface for communicating with OBC,
- radiation-tests and examples in space,
- extended temperature range,
- low complexity – also connected with transistor technological process,
- well-known architecture and known bugs/problems,
- flash memory about 16kB,
- JTAG interface for debugging and programming,
- Bootloader and ISP programming for on-board reprogram

It was chosen to use ATMega family from Atmel corporation.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.17.2 PART SELECTION

5.17.2.1 ATMega parts codes

An example:

ATMEGA164PV-10AQR

Table 5-18. An example of ATMega part code

- 164 – part number

Before hyphen:

- P – pico-power - some improvements to core and ability to put controller in deeper sleep mode,
- V – lower starting voltage (1.8V), lower clock (10 MHz maximum),
- A – new production line (possibility of smaller transistor process due to reduction of power consumption).

After hyphen:

- "10" - maximum clock frequency (in MHz),
- A/M/P - package (A - TQFP; M - MLF; P - PDIP),
- Q/U - temperature range (Q - up to 105 degrees Celsius, U - normal),
- R - tape & reel.

5.17.2.2 Preferred part code:

- V – low starting voltage,
- P – pico-power model,
- 10MHz clock,
- A package (TQFP model),
- Q temperature range (extended).

5.17.2.3 Couple microcontrollers to review

Couple microcontrollers to review were selected and they are shown below:

5.17.2.3.1 ATMEGA164P-B15AZ – automotive series

Automotive series of ATMega164 microcontroller.

Inconsistency with operating voltage – on Atmel website 1.8V, in datasheet 2.7V.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Pros	Cons
Extended (-40 to 125 degrees) temperature range	Operation voltage from 2.7V

Table 5-19. ATMEGA164P-B15AZ – automotive series

5.17.2.3.2 ATMega16(L)

Oldest microcontroller from Atmel with 16kB of flash memory.

Pros	Cons
probably low technological process in old production line	Starting voltage from 2.7V
old core with some registers with strange access (ex. URSEL bit in UCSRC register)	

Table 5-20. ATMega16 review

5.17.2.3.3 ATMega164

Pros	Cons
Starting voltage from 1.8V	
New core with better access	
2x SPI, 2xI2C interfaces	

Table 5-21. ATMega164 review

5.17.2.3.4 ATMega168

Pros	Cons
Starting voltage from 1.8V	No JTAG interface
New core with better access to registers	
2x SPI, 2xI2C interfaces	

Table 5-22. ATMega168 review

5.17.2.4 Selected part

For flight model ATMEGA164PV-10AQ was selected.

It is available from Digikey distributor.

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

For engineering model ATMEGA164PV-10AU was selected. The only difference is the temperature range. This part is wider available.

5.17.3 RADIATION EFFECT ANALYSIS IN ATMEGA

Analysis is based on radiation tests made by CERN (ATMega128) [30] and IEEE (ATMega128) [31]. Both processors are similar to chosen one, but with larger flash memory. Technological process should be similar.

CERN has made numerous tests it's ELMB (Embedded Local Monitor Board) – also for older version with ATMega103 (actually obsolete). Technological processes are noted as follows: 103L – 500nm; 128 – 350nm. Despite that, it was shown that newer processors behave better and are more immune to radiation effects.

It is considered that chosen microprocessor has technological process of 350nm also.

5.17.3.1 Total Ionising Dose (TID)

IEEE made TID tests with dose rate up to 17.1 rad/s – ATMega1280 was fully operational up to 18.3kRad. There was no significant current changes. “The initial failure was detected in the ADC test at 27.3kRad (Si) followed by complete loss of functionality at 28.3kRad (Si).”

Test conducted by CERN shown similar results – after radiation to 18 - 25krad devices were fully operational (3 months after radiation, it was not able to test them earlier – but [31] shown that there were not recovery with time). Only encountered problem was reFlashing device – “About 100 of 30000 flash memory addresses failed to program correctly.”.

5.17.3.2 Single event effects (SEE)

5.17.3.2.1 Latch-ups

Due to possible latch-ups the microcontroller will be protected with a current-limiter and reset device. Some events are recovered automatically some require reset of processor and other are recovered after power cycling.

5.17.3.2.2 Flash memory

SEU in flash memory will lead to bit change – and corruption of program data.

Tests in [30] have not detected errors with flash memory – with proton fluency of $1.3 \cdot 10^{12} \text{ protons/cm}^2$ there were no flash memory errors.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Due to possibility of reprogramming device in-flight and to provide ability to restore original software (in case error is detected in memory) there will be a bootloader. More detailed information is in corresponding section.

5.17.3.3 EEPROM memory

Similar to flash, there was no detected errors in EEPROM memory. Despite that, it was chosen to use external FRAM memory due to its immunity for TID.

5.17.3.4 SRAM memory

SEE in SRAM memory was tested in [30].

Most SEE in this IC are bit changes in SRAM memory. This can lead to problems with numerical calculus and even bad controlling MPPT. There will be both hard- and software protection for these kind of effects.

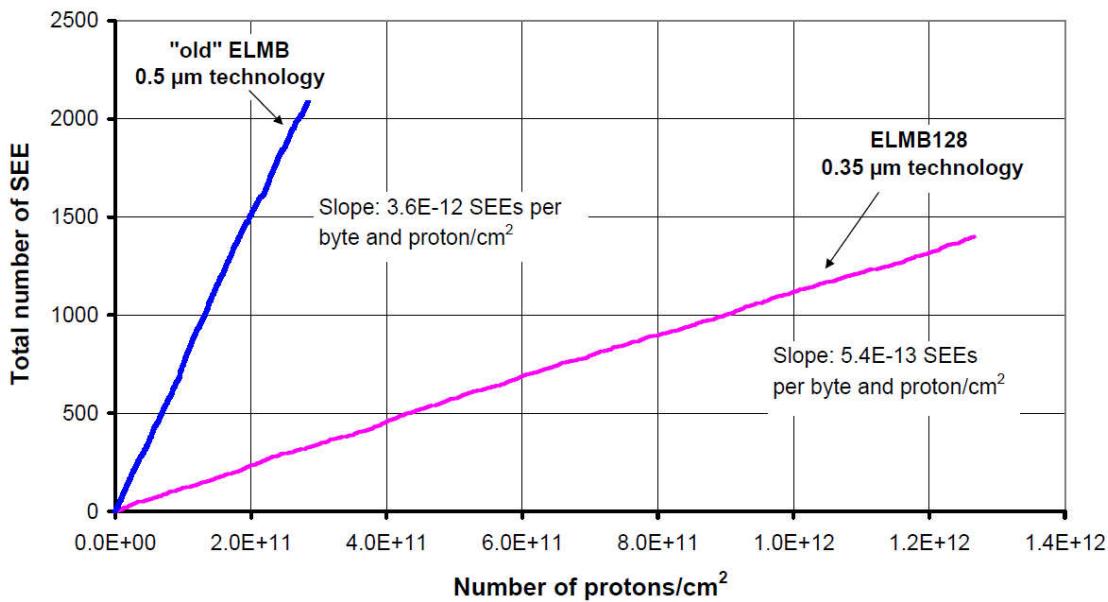


Figure 5-18. SEE in 2048 bytes of SRAM – source [30]

There is a very big difference within technology change – newer processors produce less errors than older ones.

5.17.3.5 Other memories

Registers and other memories (ADC, CAN configuration, etc.) has shown little amount of errors – which can lead to changing configuration of given peripheral.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

5.17.4 ATMega SELECTION CONCLUSION

Numerous ATMega microcontrollers tests were held. CERN researches shown ATMega128 immunity is sufficient for PW-Sat2. Our selected processor is very similar (but it has less flash memory size – so the SEE in flash is reduced).

TID tests shown that ATMega is immune to expected radiation dose.

Considering SEE ATMega main problem can be bit squatting in SRAM memory – but it can be protected from it via multiple calculations, redundancy etc.

5.17.5 PROGRAMMING ATMEGA MICROCONTROLLER

5.17.5.1 Bootloader

For changing flash memory content (firmware) when in orbit it was proposed to use bootloader connected to FRAM memory.

Firmware from ground, passing to EPS microcontrollers (via I²C satellite bus) will be stored in FRAM memory – and after reset microcontroller will re-program itself. Holding data in FRAM memory will provide redundancy to flash memory – when the error is detected in firmware (via ex. CRC) microcontroller will automatically upload firmware from FRAM memory.

5.17.5.2 In-System Programming interface

Due to possibility of error in bootloader section of flash memory it should be possible to program the bootloader from other source. One of possibilities is use of ATMega ISP protocol. It is simple SPI protocol which can be used to upload new firmware to Flash/EEPROM memories inside microcontroller. Possible solution is to connect two EPS microcontrollers via SPI bus. Problem encountered – they have to have RESET connected to each other – when one fails, it can hold second one in RESET state.

5.17.5.3 JTAG protocol

On ground, when developing software for EPS the JTAG programmer/debugger will be used. It can be used for step execution, variables watches, breakpoints etc. In flight model, firmware upload method used will be bootloader. It is not considered as option for in-flight firmware upload due to its complex protocol, number of I/O needed and no further advantages.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

6 FINAL BLOCK DIAGRAM OF THE SYSTEM

The final block diagram of the system is composed of two parts:

- Power part – power harvesting from solar panels, energy storage, EMI filters, 5V and 3V3 DCDC converters, main controllers,
- Distribution part – EMI filters, distribution switches.

The block diagrams are appended in the Appendix A.

6.1 POWER SUMMING CH0, CH1, CH2

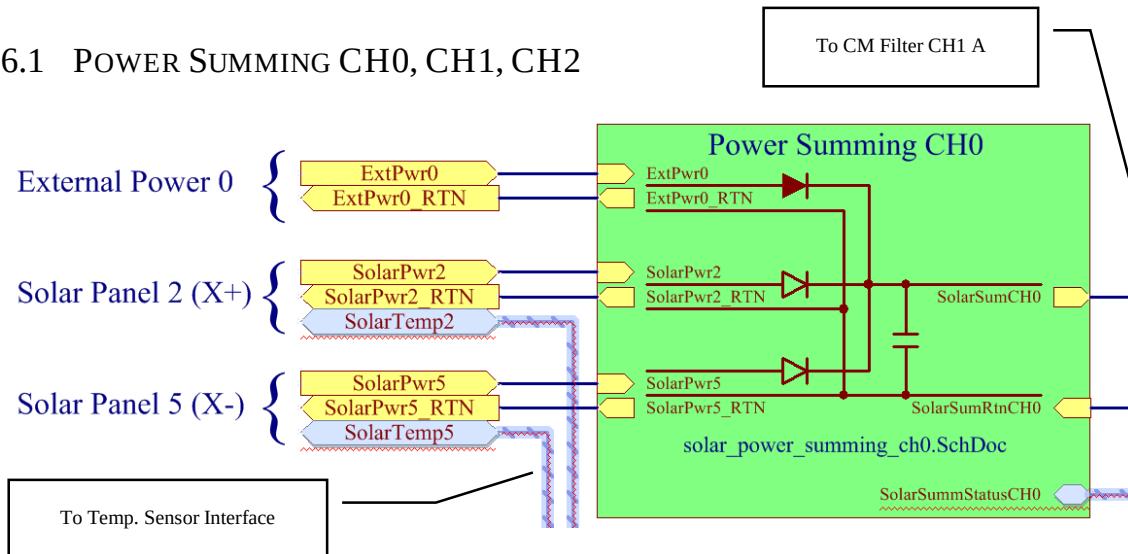


Figure 6-1. Block diagram - Power Summing CH0

Power summing modules are responsible to harvest the power from solar panels. The power summing modules are based on ideal diode controllers LTC4412, P-MOSFETs IRF7416 and Schottky diodes STPS340. External power for pre-launch testing is provided by the Shottky diode. To decrease power losses, when the ideal diode is broken, Schottky diode is connected in parallel circuit at the P-MOSFET.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

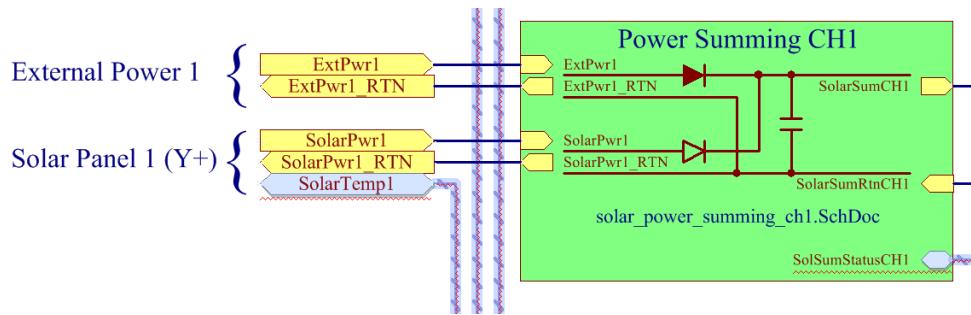


Figure 6-2. Block diagram - Power Summing CH1

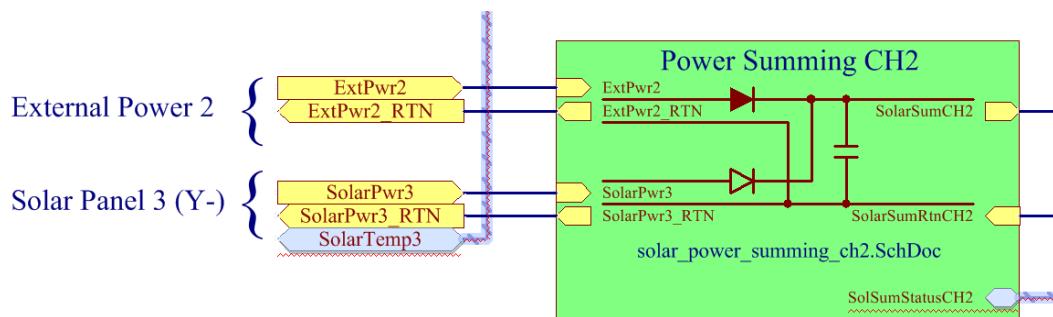


Figure 6-3. Block diagram - Power Summing CH2

To measure temperature at solar panels we will use PT1000 sensors. An interface which is responsible to measure the temperature is shown below:

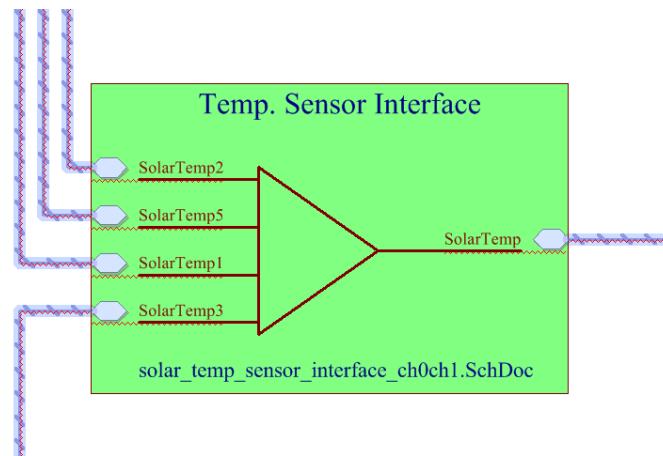


Figure 6-4. Block diagram - Temp. Sensor Interface

Detailed description of the Temp. Sensor Interface is placed in the SunS' (PW-Sat2 Sun Sensor) documentation. There is used a similar solution.

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

6.2 CM FILTERS

To suppress common-mode noise from MPPT converters we will use additional common-mode filters.

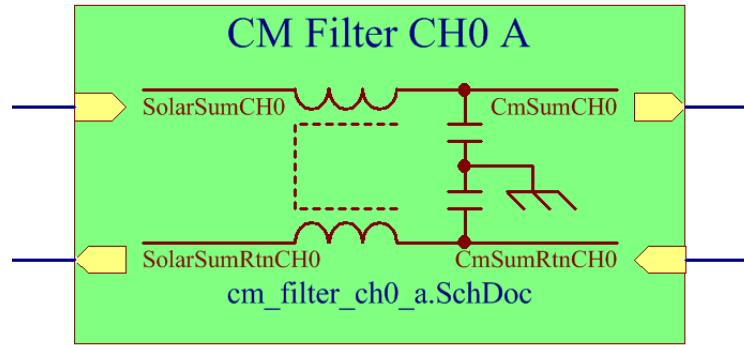


Figure 6-5. Block diagram - CM Filter CH0 A

Similar filters are used at input and output of the MPPT converters.

6.3 MEASUREMENTS CH0

To measure input power at an MPPT converter, we shall measure voltage and current at input of the converter. It will be based on the MAX4372 (to measure current) and on a voltage divider (to measure voltage). The voltage signals will be converted to a digital signal within a ADC converter.

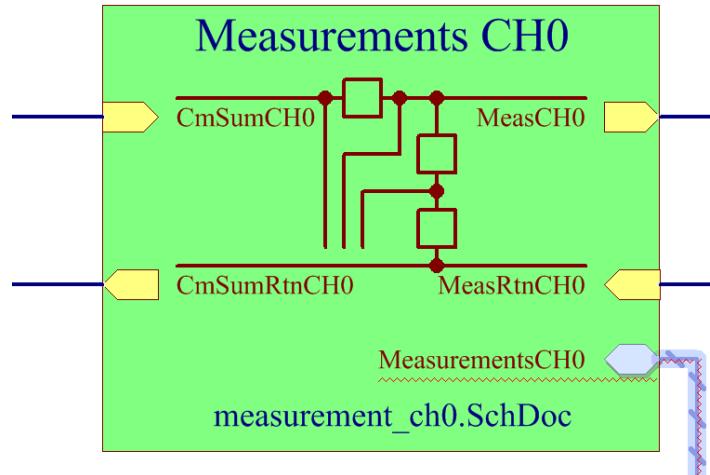


Figure 6-6. Block diagram - Measurements CH0

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

6.4 MPPT BOOST CONVERTER

The MPPT boost converter at CH0 will be controlled by a microcontroller which is placed in CH1 (because there are three MPPT channels but only 2 microcontrollers). The microcontroller from CH1 controls both the MPPT CH0 and the MPPT CH1.

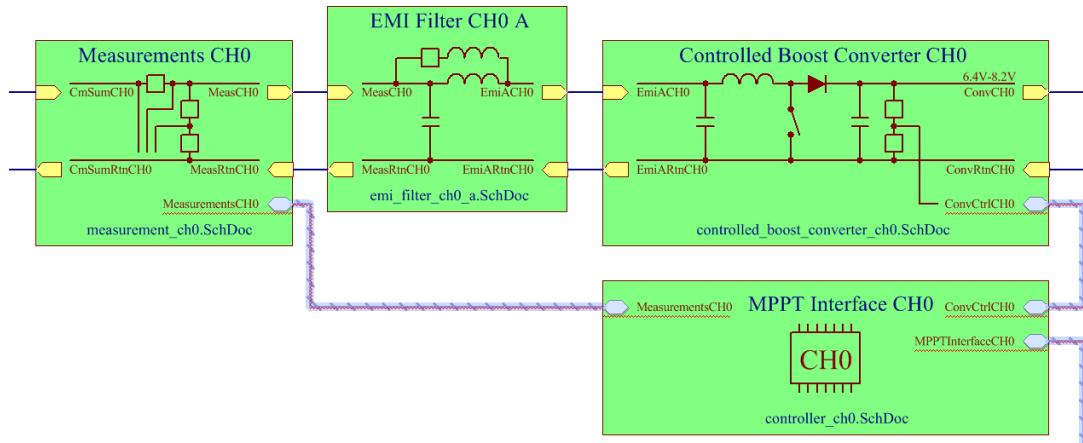


Figure 6-7. Block diagram - MPPT boost converter

EMI filters at input and output of the boost converter will be placed. ICs which are used within the Controlled Boost Converter CH0 and the MPPT Interface CH0 are placed below:

IC	Comment
T3580MPMS8E + STPS340	Boost converter
DAC121S101	To control the boost converter
ADC124S021	To measure voltages
TPS2551DBVT	Latch-up protection

Table 6-1. Block diagram – MPPT CH0 boost converter - ICs

6.5 MPPT BUCK-BOOST CONVERTERS

The MPPT buck-boost converters will be responsible to convert the harvested power from 4-cell solar panels. The 4-cell solar panels are placed on deployable solar wings. The buck-boost converters will be used by MPPT CH1 and MPPT CH2.

ICs which are used within the Controlled Buck-Boost Converter CH2 and the MPPT Interface CH2 are placed below:

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

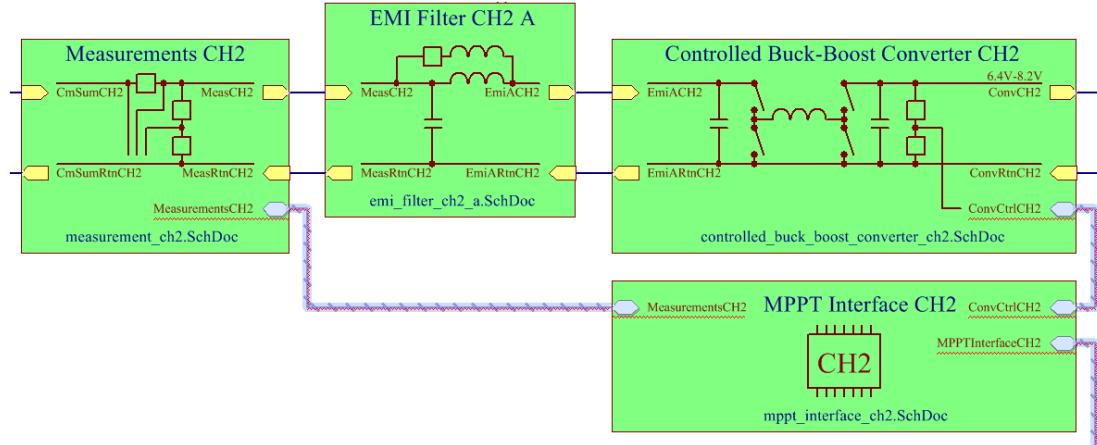


Figure 6-8. Block diagram - MPPT CH2

IC	Comment
LTC3115	Buck-Boost converter
DAC121S101	To control the boost converter
ADC124S021	To measure voltages
TPS2551DBVT	Latch-up protection

Table 6-2. Block diagram – MPPT CH2 boost converter - ICs

6.6 CONTROLLERS

To control the MPPT converters, the distribution module and other functions of EPS, ATMega microcontrollers will be used.

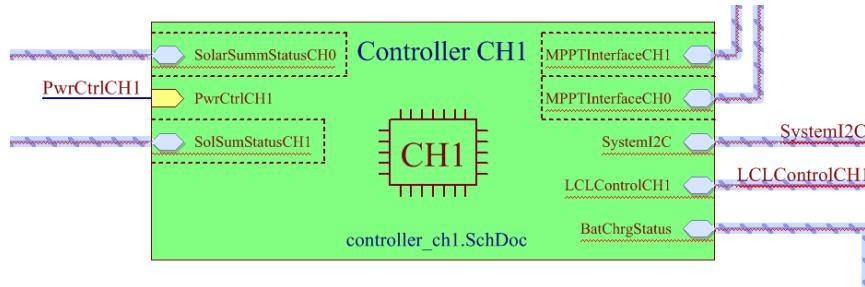


Figure 6-9. Block diagram - Controller CH1

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

Some digital interfaces will be isolated by galvanic isolation (dotted line around the Sheet Entry).

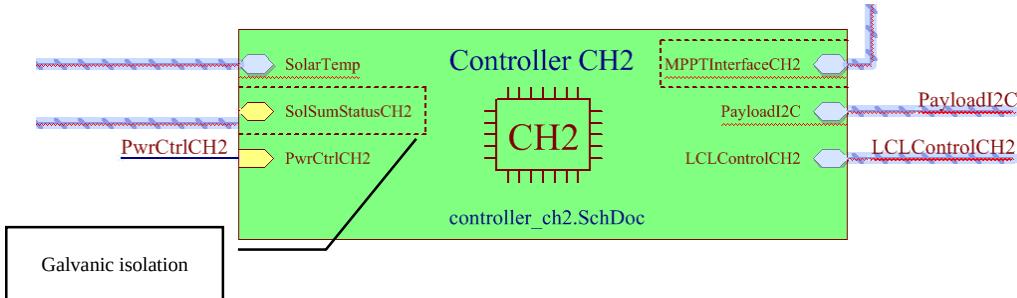


Figure 6-10. Block diagram - Controller CH2

6.7 THE MPB BUS

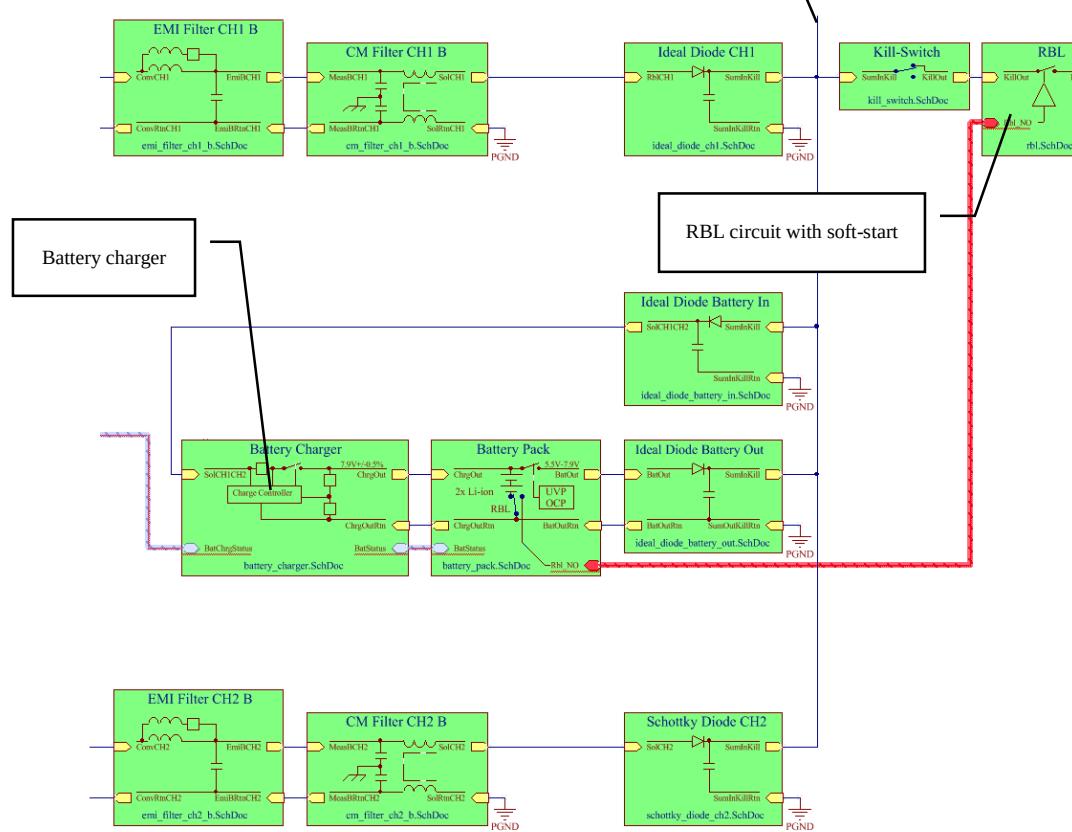


Figure 6-11. Block diagram - the MPB bus

	PW-Sat2	Preliminary Design Review	
2015-05-23			
Phase B		Electrical Power System	

6.8 THE DISTRIBUTION MODULE

The distribution module contains:

- LCL switches – FPF270x or TPS2551 switches will be used, depending on a supply voltage and a supply current of a subsystem. Both the Controller CH1 and the Controller CH2 will be controlled simultaneously all LCL switches – full redundancy.
- Current and voltage measurements based on MAX4372, voltage dividers and ADC128S022 – SPI communication with controllers of the EPS,
- EMI filters, which are responsible for a noise separation between subsystems.

The distribution module will be placed on a daughter board which is stacked on the top side of the main EPS board.

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

7 DEVELOPMENT SCHEDULE

Development schedule of the EPS is shown below:

Model	Comment	Date
EM	PCB manufacturing, EM parts ordering	05.2015 - 06.2015
EM	Assembling	06.2015
EM	First functional tests	06.2015
EM	Software developing and testing	06.2015 – 09.2015
EM	First functional tests with OBC from Createch Instruments S.A.	09.2015
EM -> PFM	First revision of the PCB	08.2015
PFM	PCB manufacturing, FM parts ordering	09.2015
PFM	Assembling	09.2015 – 10.2015
PFM	First functional tests	10.2015
PFM	Software developing and testing	11.2015
FM	Spacecraft long-term tests and software developing	12.2015 – 05.2016

Table 7-1. Development schedule

	PW-Sat2	Preliminary Design Review	
	2015-05-23		
	Phase B	Electrical Power System	

8 APPENDIX A

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

Bibliography

- [1] ECSS, „Space engineering; Technical requirements specification; ECSS-E-ST-10-06C,” 2009.
- [2] NASA, "Redundancy Switching Analysis; PD-AP-1315," 1995.
- [3] L. Simon, H. Amy, T. Armen, L. Wenschel and M. Riki, "Cubesat Design Specification Rev. 12," California Polytechnic State University, California, 2009.
- [4] ECSS, „Space product assurance; Derating - EEE components; ECSS-Q-ST-30-11C Rev 1,” 2011.
- [5] ECSS, „Space engineering; Spacecraft charging; ECSS-E-ST-20-06C,” 2008.
- [6] AWR, „CubeSat Kit PCB Specification, Rev. A5,” PUMPKIN, San Francisco, 2007.
- [7] ECSS, „Space product assurance; Design rules for printed circuit boards; ECSS-Q-ST-70-12C,” 2014.
- [8] ECSS, „Space product assurance; High-reliability soldering for surface-mount and mixed technology; ECSS-Q-ST-70-38C,” 2008.
- [9] ECSS, „Space product assurance; Manual soldering of high-reliability electrical connections; ECSS-Q-ST-70-08C,” 2009.
- [10] ECSS, „Space engineering; Electromagnetic compatibility; ECSS-E-ST-20-07C Rev. 1,” 2012.
- [11] D. o. Defense, „Interfece Standard; Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment; MIL-STD-461F,” 2007.
- [12] M. R. Patel, Spacecraft Power Systems, CRC Press, 2005, p. 691.
- [13] M. Rosu-Hamzescu and S. Oprea, "AN1521 - Practical Guide to Implementing Solar Panel MPPT Algorithms," Microchip Technology Inc., 2013.
- [14] N. Steiner, „Phase C; EPS subsystem: Electrical qualification tests,” SwissCube, 2007.
- [15] M. Pajusalu, E. Ilbis, T. Ilves, M. Veske, J. Kalde, H. Lillmaa, R. Rantsus, M. Pelakauskas, A. Leitu, K. Voormansik, V. Allik, S. Lätt, J. Envall i M. Noorma, „Design and pre-flight testing of the electrical power system for the ESTCube-1 nanosatellite,” Estonian Academy of Sciences, 2014.
- [16] I. Buchmann, Batteries in a Portable World, Cadex Electronics Inc., 2011.
- [17] M. Sclocchi, „Input Filter Design for Switching Power Supplies,” National Semiconductor, 2010.
- [18] R. Rantsus, „Designing, Implementing and Testing the Solar Power Harvesting System for ESTCube-1,” University of Tartu, Faculty of Science and Technology Institute of Physics, Tartu, 2011.
- [19] E. Fiori, B. Alpat, R. Battiston, M. Bizzarri, S. Blasko, M. T. Brunetti, D. Caraffini, L. Di Masso, L. Farnesini, M. Menichelli, A. Papi, M. Petasecca, V. Postolache, G. Scolieri i A. Secchi, „Total Dose Test

	PW-Sat2	Preliminary Design Review	
	2015-05-23	Electrical Power System	
	Phase B		

for AMS Power Supply Components," University of Perugia.

- [20] L. T. Corporation, „Products for Harsh Environments; High Reliability Analog ICs,” 2012.
- [21] T. Instruments, „Defense Guide; Rev. A,” www.ti.com/defense, 2012.
- [22] D. J. Cochran, S. P. Buchner, D. Chen, H. S. Kim, K. A. LaBel, T. R. Oldham, M. J. Campola, M. V. O’Bryan, R. L. Ladbury, C. Marshall, A. B. Sanders i M. A. Xapsos, „Total Ionizing Dose and Displacement Damage Compendium of Candidate Spacecraft Electronics for NASA,” IEEE, 2009.
- [23] R. Kingsbury, F. Schmidt, K. Cahoy i D. Sklair, „TID Tolerance of Popular CubeSat Components,” IEEE, Cambridge, 2013.
- [24] T. Fairbanks, H. Quinn, J. Tripp, J. Michel, A. Warniment i N. Dallmann, „Compendium of TID, Neutron, Proton and Heavy Ion Testing of Satellite Electronics for Los Alamos National Laboratory,” IEEE, 2013.
- [25] J. Gilmore, J. Haley, V. Khotilovich, J. K. Roe, A. Safonov, I. Suarez i S. Yeager, „Very forward muon trigger and data acquisition electronics for CMS: design and radiation testing,” IOP Publishing for Sissa Medialab, 2013.
- [26] ESCC, „European Preferred Parts List; Issue 28,” ESA, 2015.
- [27] T. Instruments, „ADC128S102 8-Channel, 500-ksps to 1-Msp, 12-Bit A/D Converter,” 2015.
- [28] N. Semiconductor, „Space Solutions; Selection Guide; Vol. 1,” 2010.
- [29] T. Instruments, „ADC128S102QML 8-Channel, 50 kSPS to 1 MSPS, 12-Bit A/D Converter,” 2011.
- [30] H. Boterenbrood i B. Hallgren, „SEE and TID Tests of the Embedded Local Monitor Board with the ATMEGA128 processor,” CERN ATLAS Internal Working Note DCS- IWN20, 2003.
- [31] K. Avery, J. Finchel, J. Mee, W. Kemp, R. Netzer, D. Elkins, B. Zufelt i D. Alexander, „Total Dose Test Results for CubeSat Electronics,” IEEE, 2011.
- [32] R. W. Erickson, Fundamentals of Power Electronics, 1997.
- [33] A. K. Hyder, R. L. Wiley, G. Halpert, D. J. Flood and S. Sabripour, Spacecraft Power Technologies, London: Imperial College Press, 2003.
- [34] M. Steller, „Solar Orbiter; RPW DPU Hardware; DPU Preliminary Design Report,” IWF Space Research Institute, 2014.