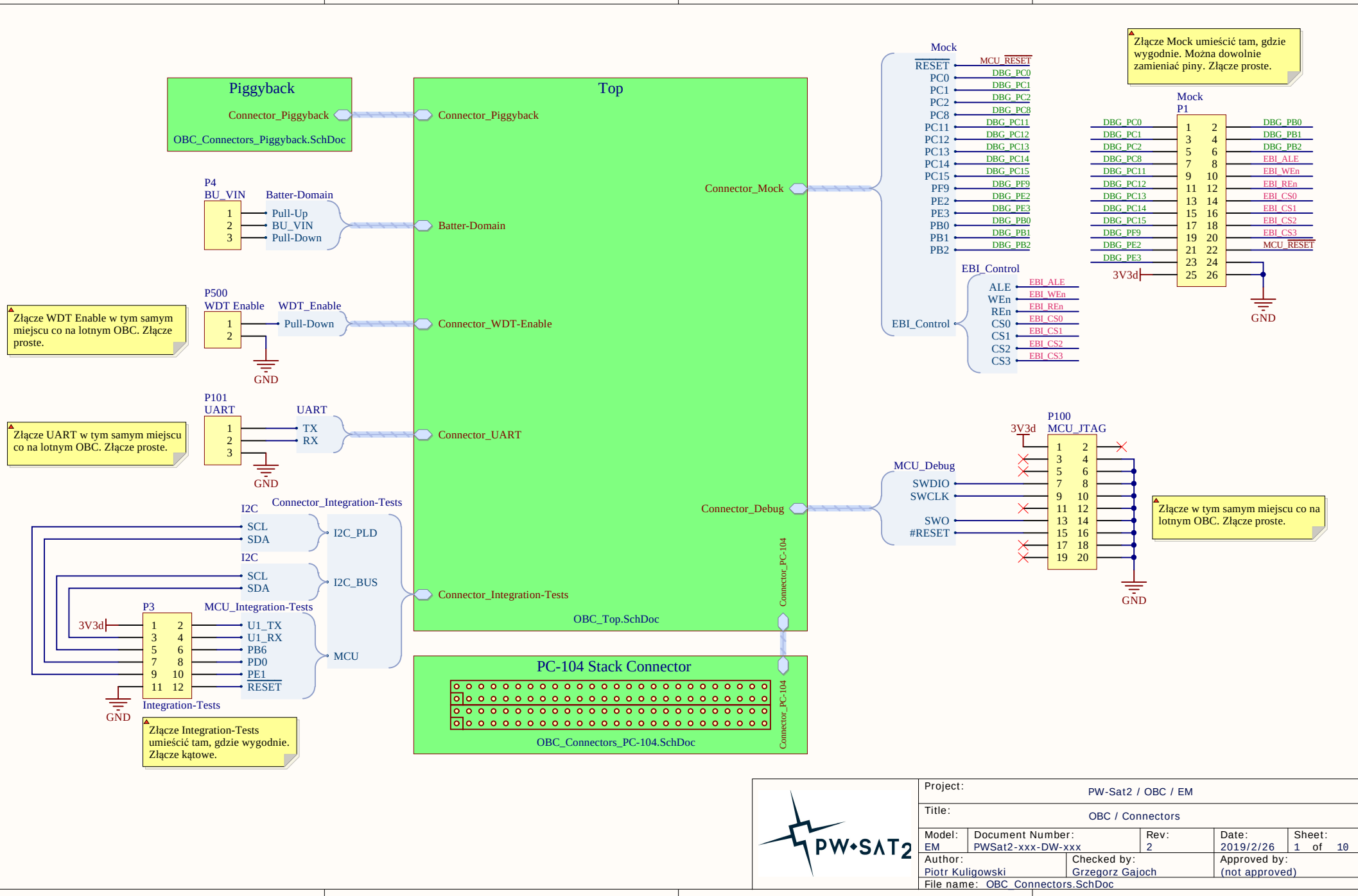
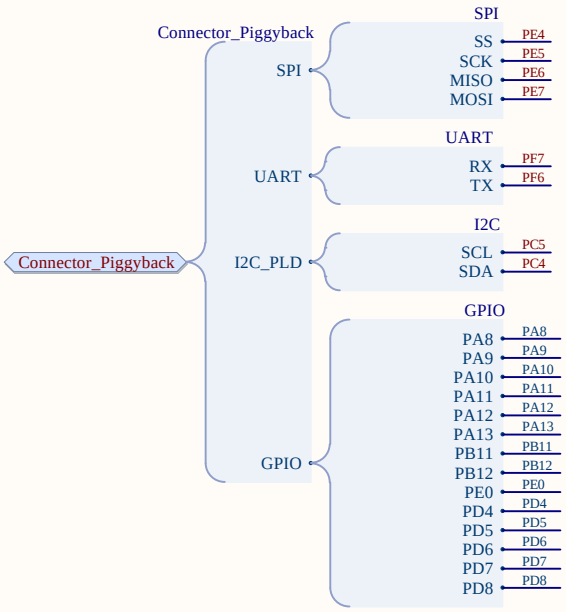
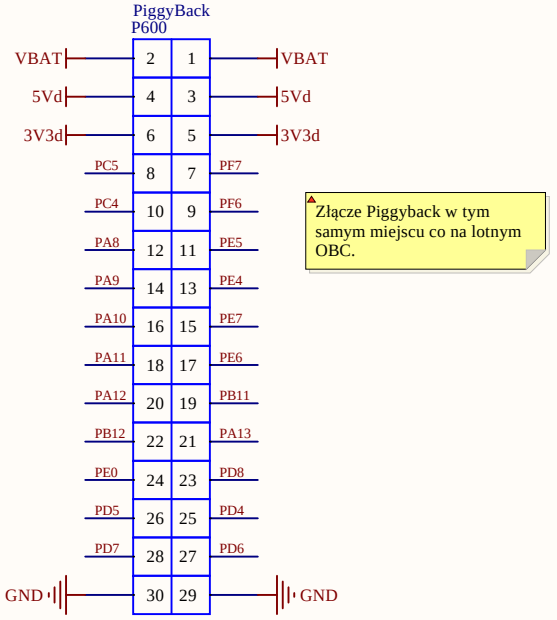
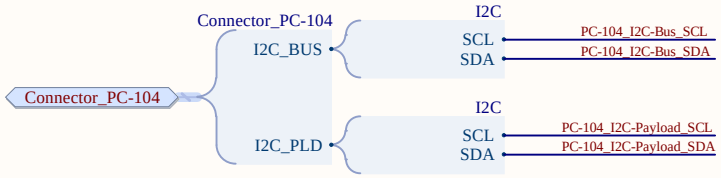


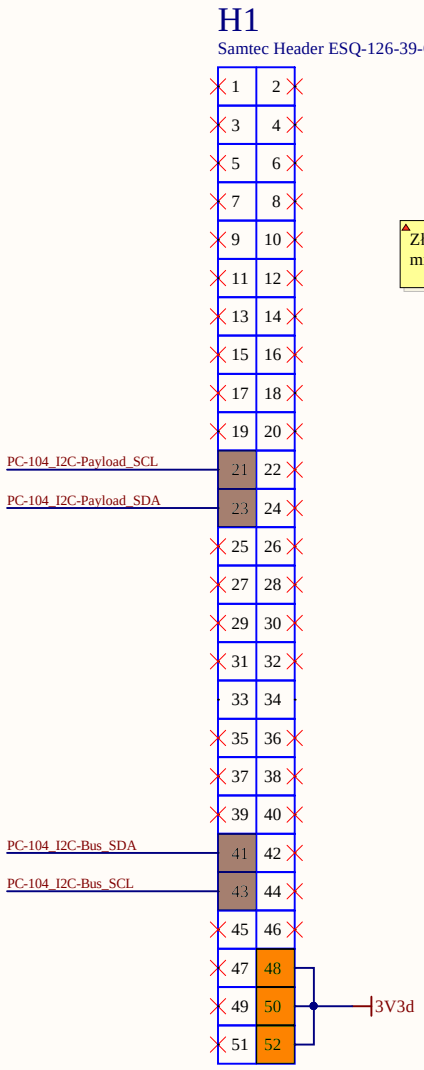
Project: PW-Sat2 / OBC / EM				
Title: OBC / Connectors				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 1 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_Connectors.SchDoc				



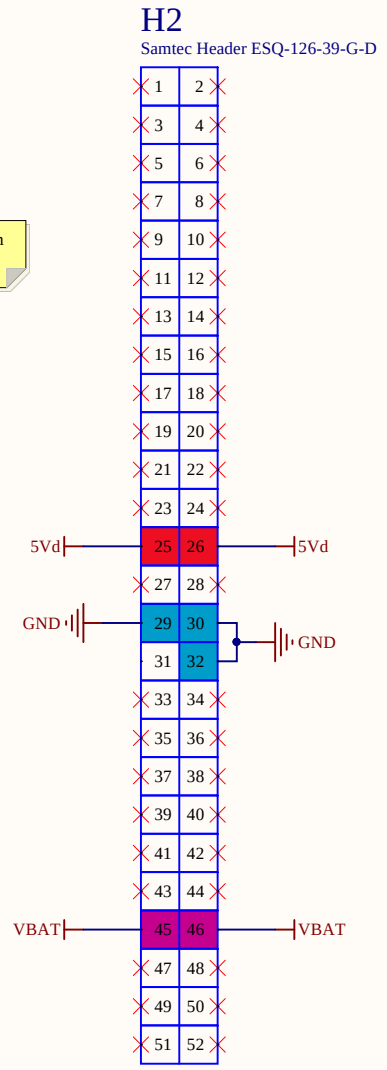


PW-SAT2	Project: PW-Sat2 / OBC / EM			
	Title: OBC / Connectors / Piggyback			
	Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 2 of 10
	Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)	
	File name: OBC_Connectors_Piggyback.SchDoc			

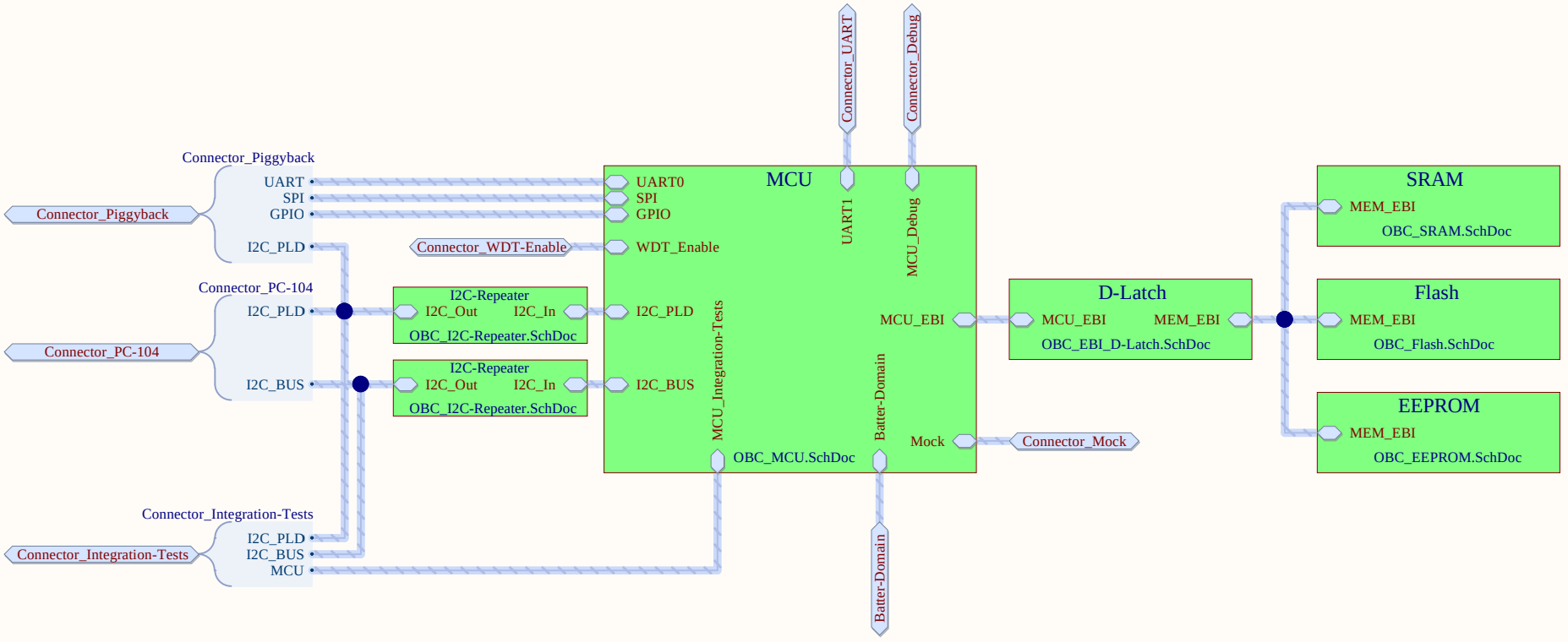




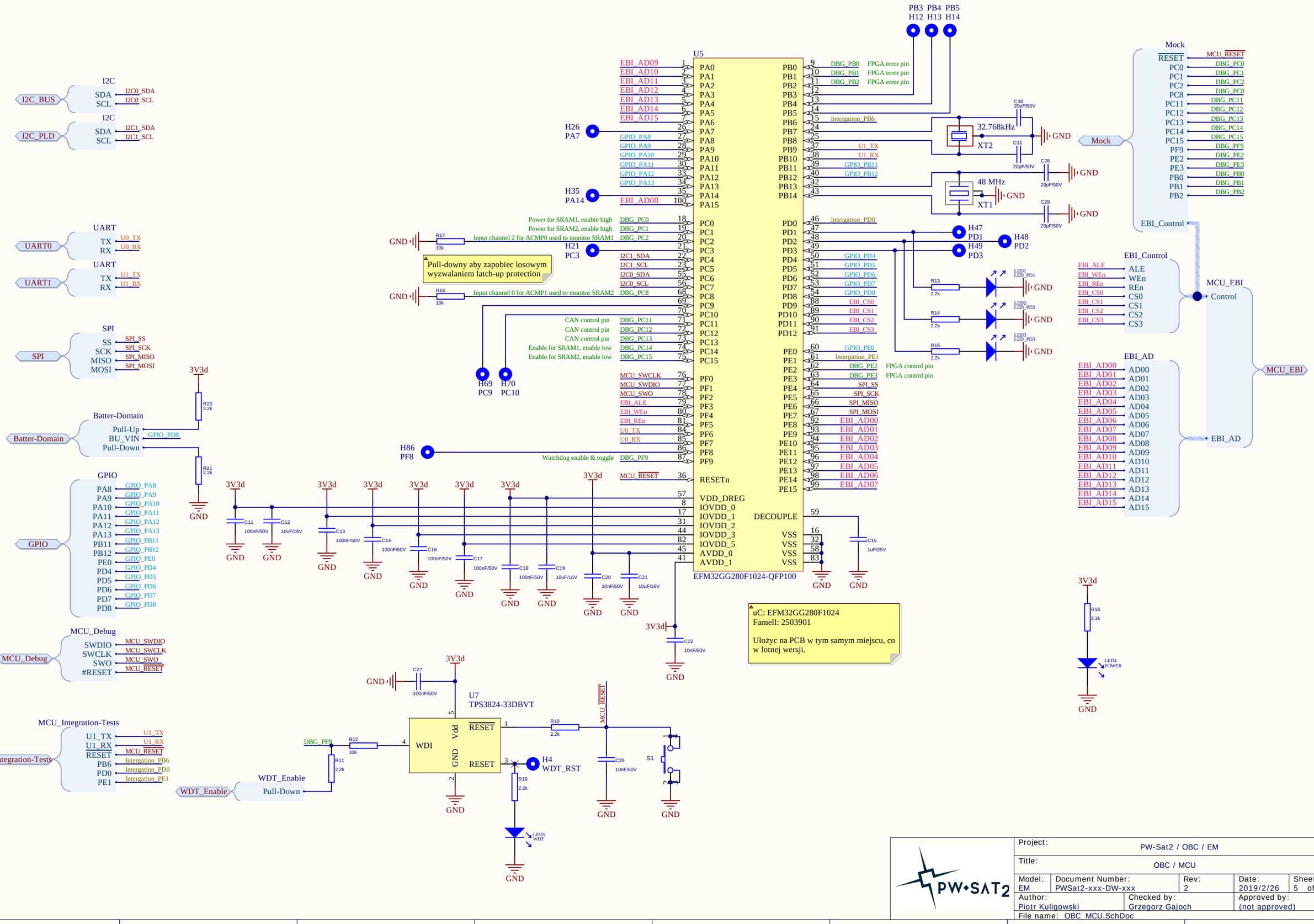
Złącza PC-104 w tym samym miejscu co na lotnym OBC.



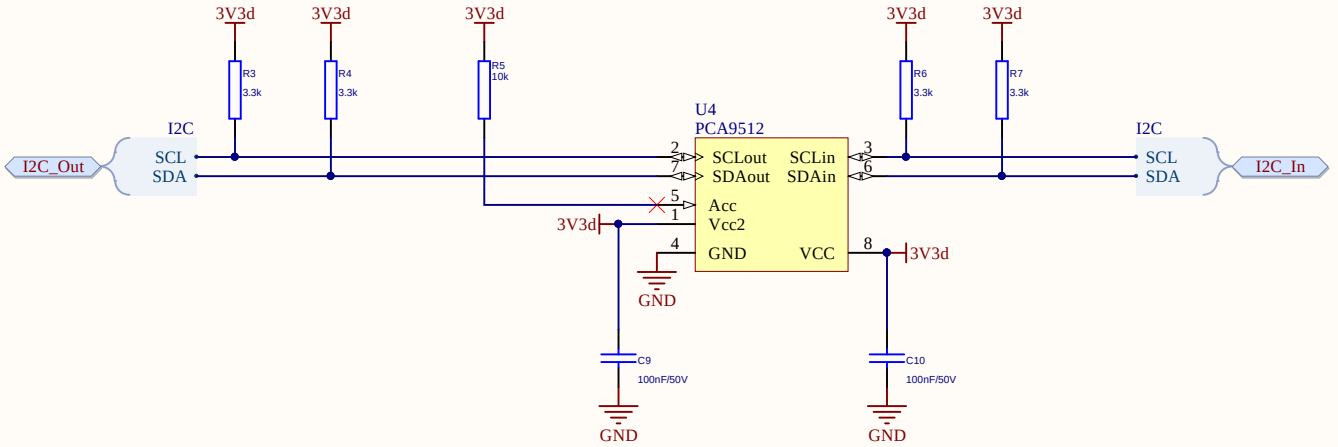
Project: PW-Sat2 / OBC / EM				
Title: OBC / Connectors / PC-104				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 3 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch		Approved by: (not approved)	
File name: OBC_Connectors_PC-104.SchDoc				



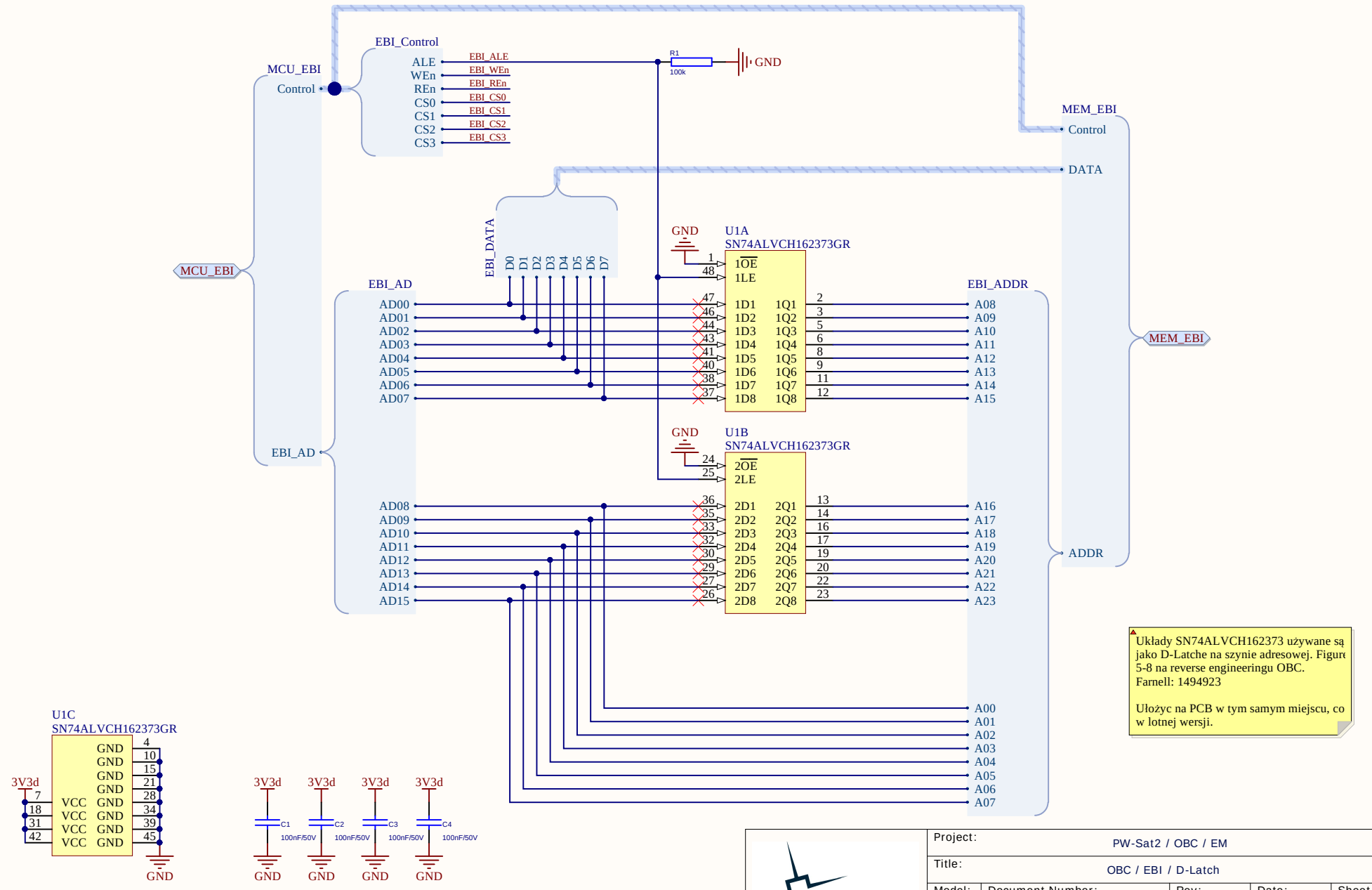
Project: PW-Sat2 / OBC / EM				
Title: OBC / Top				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 4 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_Top.SchDoc				



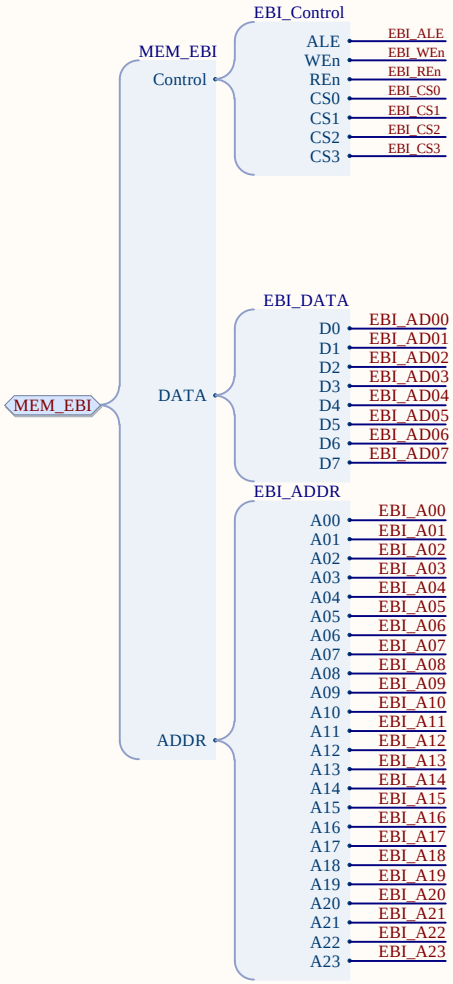
Project: PW-Sat2 / OBC / EM				
Title: OBC / MCU				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 5 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_MCU.SchDoc				

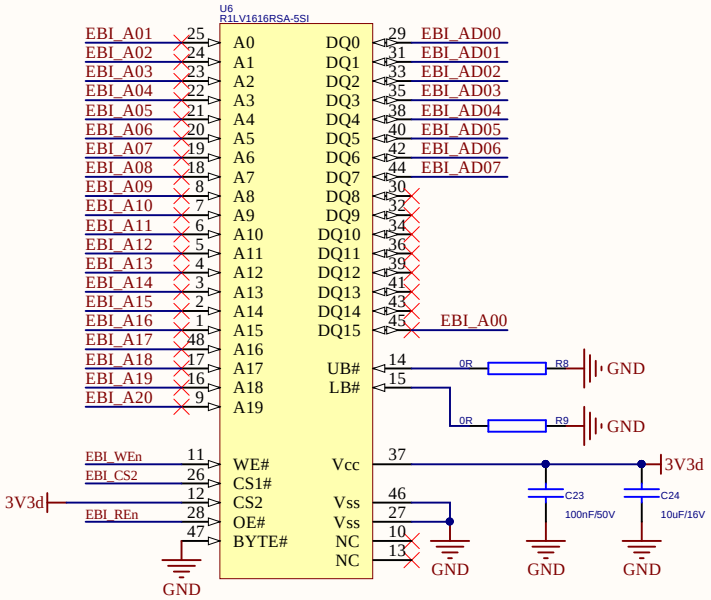


Project: PW-Sat2 / OBC / EM				
Title: OBC / I2C Repeater				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 6 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch		Approved by: (not approved)	
File name: OBC_I2C-Repeater.SchDoc				



Project: PW-Sat2 / OBC / EM				
Title: OBC / EBI / D-Latch				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 7 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_EBI_D-Latch.SchDoc				

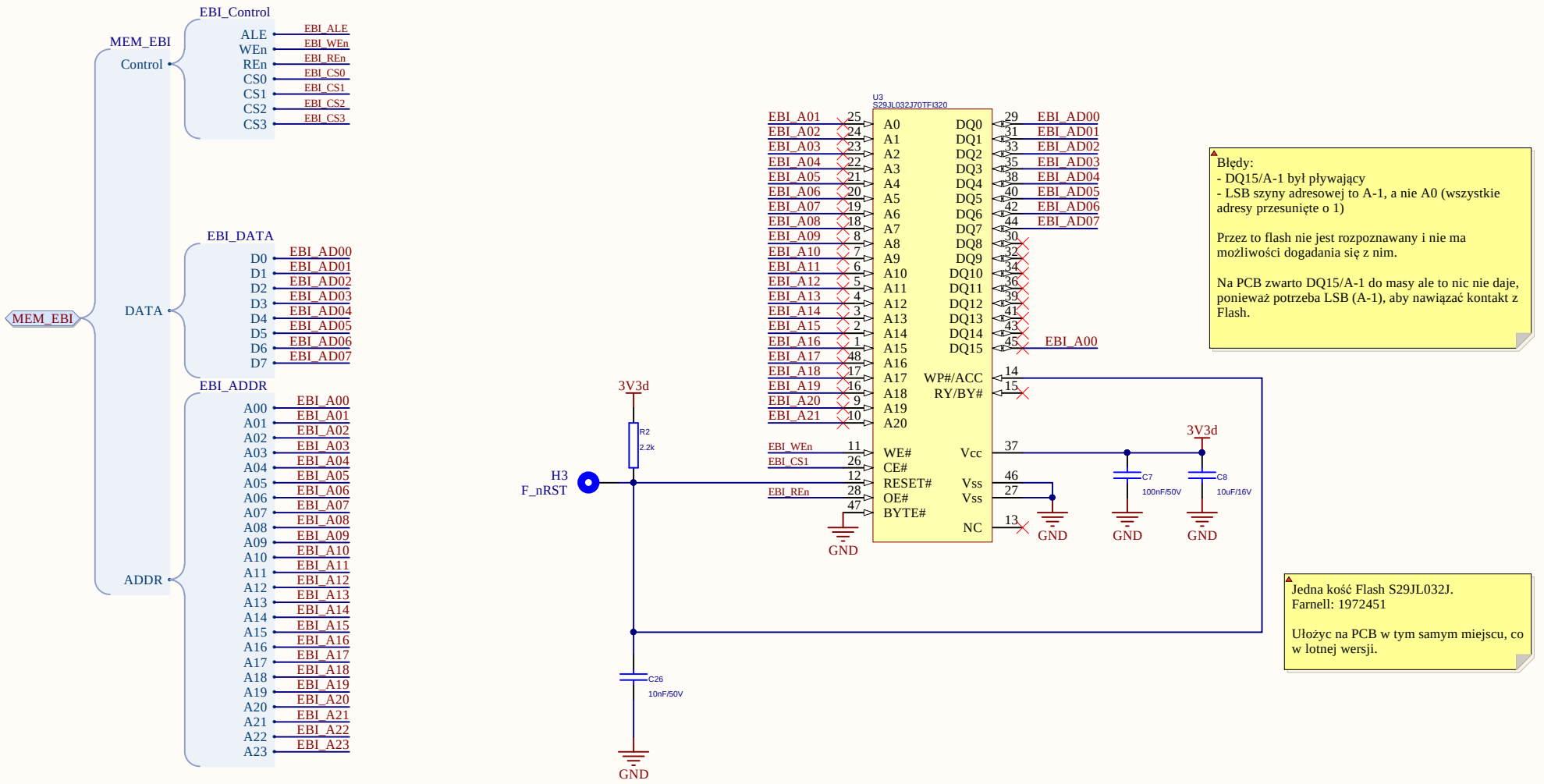




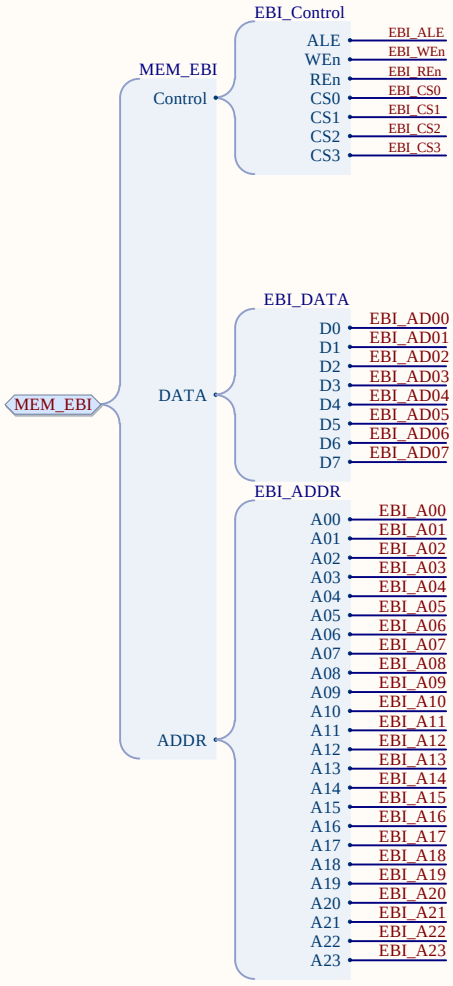
Jeden SRAM R1LV1616RSA-5SI
Digikey: R1LV1616RSA-5SI#B0-ND

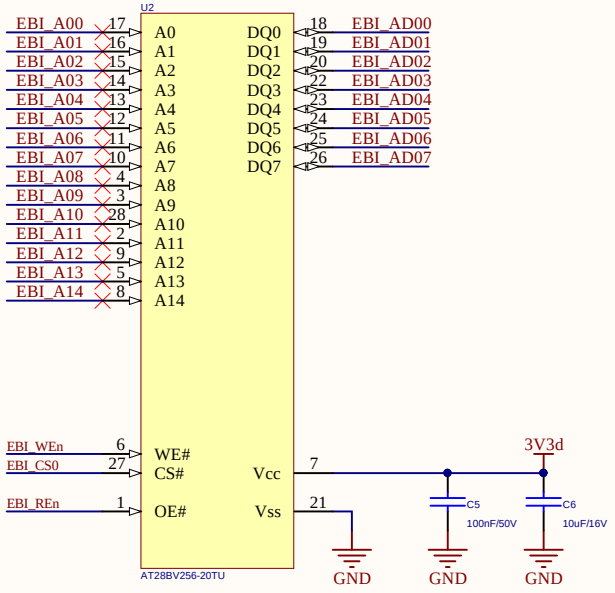
Ułożyc na PCB w tym samym miejscu, co w lotnej wersji. W lotnej wersji są dwie pamięci, tutaj będzie jedna.

PW-SAT2	Project: PW-Sat2 / OBC / EM			
	Title: OBC / SRAM			
	Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 8 of 10
	Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)	
	File name: OBC_SRAM.SchDoc			



PW-SAT2	Project: PW-Sat2 / OBC / EM			
	Title: OBC / Flash			
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 9 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_Flash.SchDoc				





Jedna kość EEPROM AT28BV256.
Farnell: 2345612

Ułożyc na PCB w tym samym miejscu, co w lotnej wersji.

Project: PW-Sat2 / OBC / EM				
Title: OBC / EEPROM				
Model: EM	Document Number: PWSat2-xxx-DW-xxx	Rev: 2	Date: 2019/2/26	Sheet: 10 of 10
Author: Piotr Kuligowski	Checked by: Grzegorz Gajoch	Approved by: (not approved)		
File name: OBC_EEPROM.SchDoc				

OBC EM.2.02

S1
MCU RESET

P1 (MOCK)

GND		3.3V
GND		PE3
nRST		PE2
EBI_nCS3		PF9
EBI_nCS2		PC15
EBI_nCS1		PC14
EBI_nCS0		PC3
EBI_REN		PC12
EBI_WEN		PC11
EBI_ALE		PC8
PB2		PC2
PB1		PC1
PB0		PC0

P4
Pull-up
BU_VIN (PD8)
Pull-down

P500 (WDT Enable)
WDT

GND
RX
TX
P101

P100 (SWD)

P3 (Integration)

nRST		GND
PE1		PC5
PD0		PC4 (BUS)
PB6		SCL
(U1)		SDA
RX		
TX		3.3V

C1 C15 C19 C18 C25 R10 C28 C29 C20 C16 C17 C22 C14 C13 C11 C12 C24 C23 C8 C7 C26 R2 R16 POWER

H70 H69 H4 H86 H26 H35 H21 H12 H14 H3 H13 H47 H48 H49

R1 R9 R8 R13 R14 R15 LED_PD1 LED_PD2 LED_PD3

U1 U5 U6 U3 XT1

R6_1 R3_1 C9_1 C10_1 U4_1 R5_1 R7_1 R4_1
R6_2 R3_2 C9_2 C10_2 U4_2 R5_2 R7_2 R4_2

PC8 -> ACMP1
PC2 -> ACMP0
PC1 -> Power SRAM2
PC0 -> Power SRAM1
PC14->Enable SRAM1
PC15->Enable SRAM2
PE2->FPGA ctrl. pin
PE3->FPGA ctrl. pin
PB0->FPGA err. pin
PB1->FPGA err. pin
PB2->FPGA err. pin
PF9->WDT enable/toggle

Active high
Active low

H1
H2

TOP

P600
(Piggyback)

GND PD7 PD5 PE0 PB12 PA12 PA11 PA10 PA9 PA8 PC4 PC5 3.3V 5V VBAT

GND PD6 PD4 PD8 PA13 PB11 PE6 PE7 PE4 PE5 PF6 PF7 3.3V 5V VBAT

R12 R11 C27 U7 R19 C21 C2 C3 C4 R21 R20 C30 C31 XT2

NC
NC
nRST
SWO
NC
SWCLK
SWDIO
NC
NC — GND
NC — NC
3.3V

U2 R18 C6 C5 R17

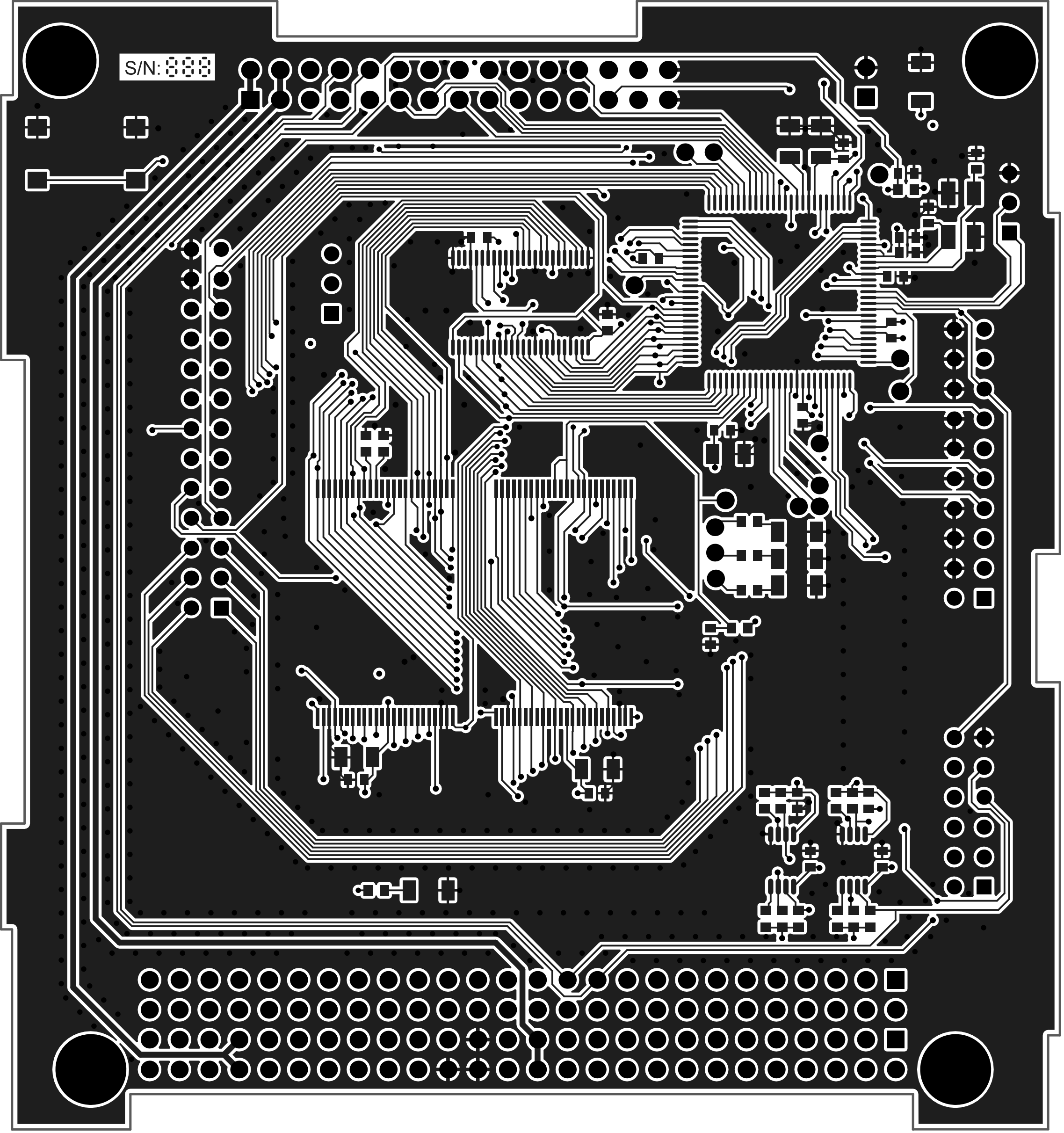
GND GND

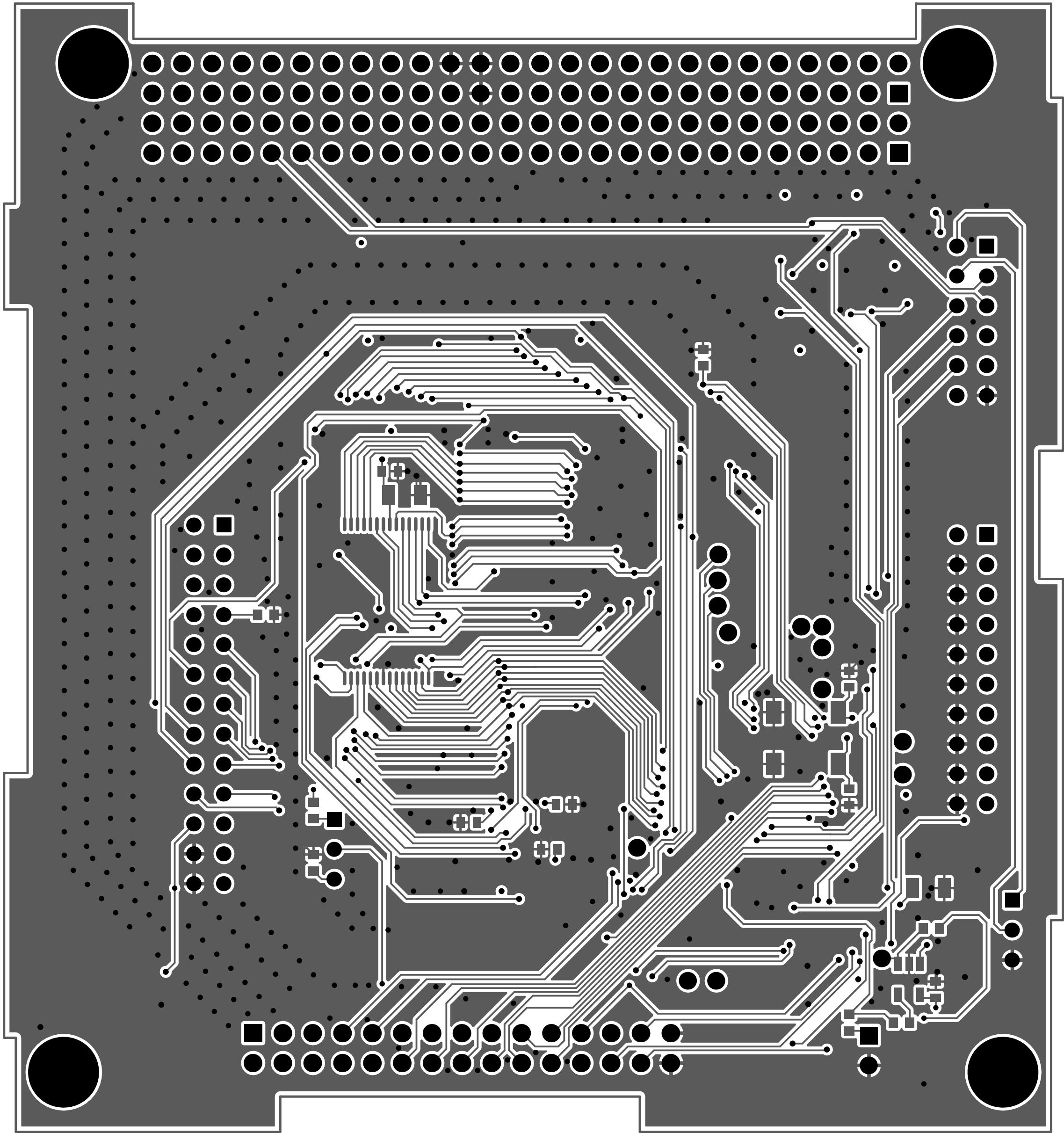
GND GND

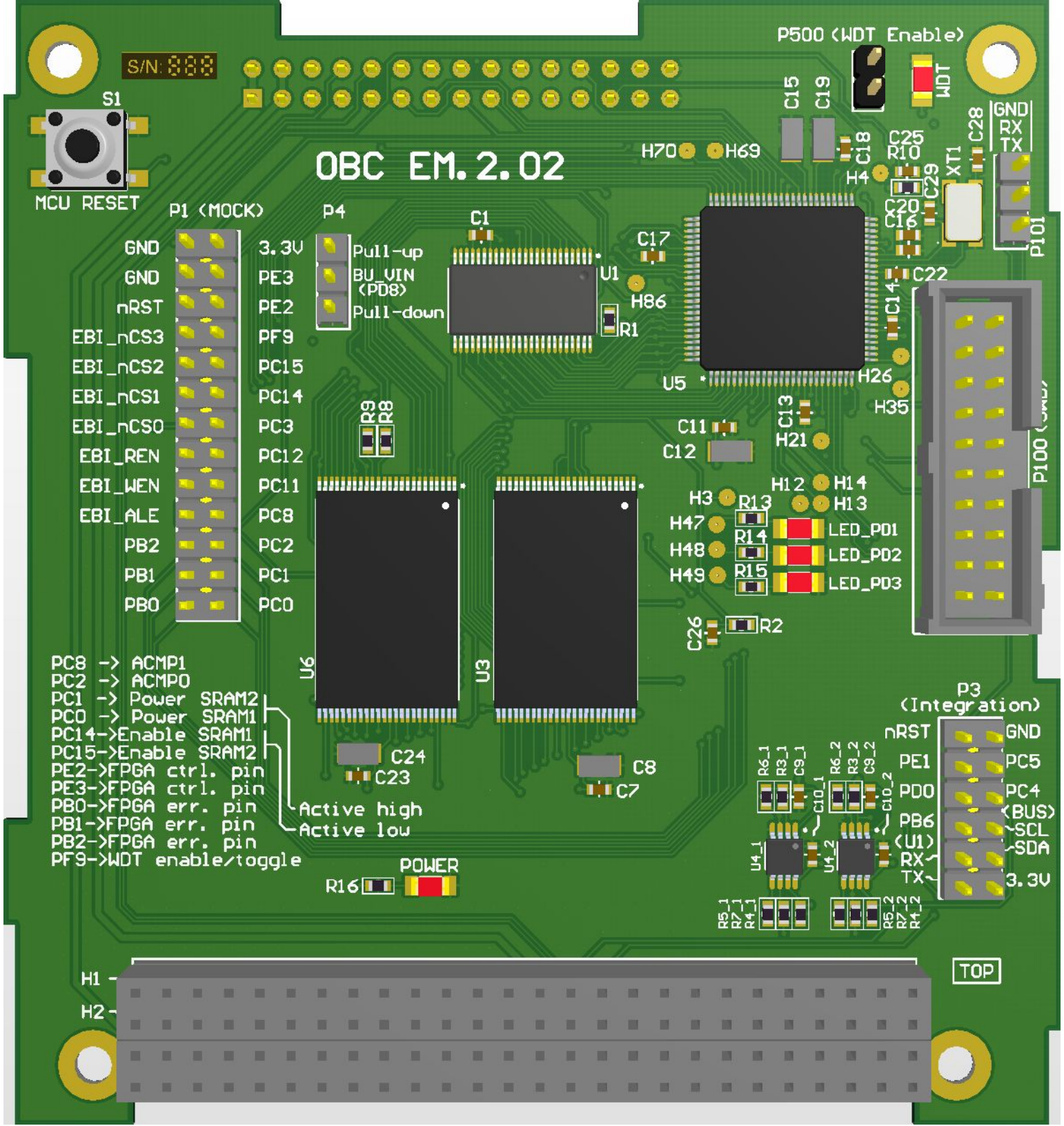
Supply

3V3 3V3 3V3

BOTTOM


S/N:




OBC EM.2.02
S/N:888
S1
MCU RESET
P1 (MOCK)
GND
GND
nRST
EBI_nCS3
EBI_nCS2
EBI_nCS1
EBI_nCS0
EBI_REN
EBI_WEN
EBI_ALE
PB2
PB1
PB0
3.3V
PE3
PE2
PF9
PC15
PC14
PC3
PC12
PC11
PC8
PC2
PC1
PC0
P4
Pull-up
BU_VIN (PD8)
Pull-down
U1
U5
U6
U3
P500 (WDT Enable)
WDT
P101
P100
P3 (Integration)
nRST
PE1
PD0
PB6 (U1) RX
TX
GND
PC5
PC4 (BUS) SCL
SDA
3.3V
LED_PD1
LED_PD2
LED_PD3
POWER
PC8 -> ACMP1
PC2 -> ACMP0
PC1 -> Power SRAM2
PC0 -> Power SRAM1
PC14->Enable SRAM1
PC15->Enable SRAM2
PE2->FPGA ctrl. pin
PE3->FPGA ctrl. pin
PB0->FPGA err. pin
PB1->FPGA err. pin
PB2->FPGA err. pin
PF9->WDT enable/toggle
Active high
Active low
H1
H2
TOP

P600
(Piggyback)
GND PD7 PD5 PE0 PB12 PA12 PA11 PA10 PA9 PA8 PC4 PC5 3.3V 5V VBAT
GND PD6 PD4 PD8 PA13 PB11 PE6 PE7 PE4 PE5 PF6 PF7 3.3V 5V VBAT
R12
R11
C27
U7
R19
C21
C30
X12
C31
C2
C3
C4
R21
R20
NC
NC
nRST
SWO
NC
SWCLK
SWDIO
NC
NC
GND
NC
3.3V
U2
R18
C6
C5
R17
GND
GND
GND
Supply
3V3
3V3
3V3
BOTTOM