Low Power Digital Beamforming with Approximate Compute for Mobile Ultrasound Systems

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Abstract—**As the size of 2D transducer arrays for ultrasound systems increase, the hardware complexity, die area, and power of digital beamforming circuits increases by the number of elements squared; moreover, as ultrasonic imaging systems trend toward mobile applications, modern beamforming techniques do not address the growing power and area restrictions demanded by these applications. Approximate computing (AC) introduces a technique to reduce power and area in integrated digital circuits. By implementing a delay and sum (DAS) beamformer with approximate compute arithmetic blocks, lower power and area will be achieved while mitigating image resolution loss compared to conventional ultrasound imaging. A delay and sum beamformer implemented with approximate compute provides adequate image resolution while minimizing power and area to be beneficial toward mobile ultrasound applications.**

Index Terms—**Beamforming, Transducer, Approximate Computing, Delay-and-Sum.**

I. Introduction

HIGH frequency ultrasound imaging is an effective tool for medical diagnosis due to its non-invasive, real time body imaging capability. Evolution of ultrasonic imaging technology from single element transducers to 2D transducer arrays improved focusing techniques for both the transmitting and receiving operations of the ultrasonic imaging device [1]. Receive focusing is known as beamforming and may be implemented with a series of delays and adders. However, the growing number of elements in 2D ultrasonic imaging devices have greatly increased the rate at which data needs to be transmitted from the system front-end and processed by the beamformer. Additionally, the increase in transmission and processing rates have greatly increased circuit area and power consumption in traditional digital beamformers [2]. These shortcomings become increasingly more prevalent as ultrasonic imaging devices transition to mobile platforms [3].

Approximate computing (AC) has recently emerged as a promising technique for reducing power and area in digital integrated circuits. The principle behind AC is using deterministic hardware that will produce low order errors but can be built with much fewer resources. For example, adder cells can be designed with only 10 transistors by utilizing XOR/XNOR gates and pass transistor style muxes [4]. The use of pass transistors in these adders reduces the noise margin and can therefore produce less accurate results compared to a conventional CMOS adder which uses 28 transistors. Han et. al implemented an inverse discrete cosine transform algorithm with approximate adders and simulated a 38% energy savings compared to an exact computation [5].

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Beamforming implemented with approximate compute offers an attractive solution for mobile ultrasound systems that require low power, small area and only moderate accuracy. This project explores the use of approximate compute techniques for beamforming implementations in mobile ultrasound applications.

II. Problem Description

A. Area and Power Limitations in Beamforming

Advances in ultrasonic imaging system technology have enabled larger transducer arrays, resulting in greater control of delay and weighting of each array element for receive beamforming. Beamforming enables dynamic scan depth focusing as opposed to fixed focal lengths of single element transducer systems [6]. However, more elements in transducer arrays inherently produce beamforming architectures that suffer from increased area and power dissipation. This increase in power and area is compounded by the desire for higher resolution images that demand higher transmission and image processing rates. A push toward mobile applications has put increasing pressure on ultrasonic imaging systems to be low power while occupying smaller area. Therefore, emerging beamforming techniques must maintain high quality imaging while minimizing power dissipation and area.

Modern beamforming techniques attempt to remedy the tradeoffs between power and resolution and between area and resolution through various techniques. Wagner reduced power dissipation by reducing processing rates in a technique describe as compressed beamforming. In compressed beamforming, low power is achieved by beamforming the sub-Nyquist samples obtained from multiple transducer elements; however, increased beamformer complexity translated to greater area when implemented on chip [7]. Feldkamper proposed a low power iterative algorithm for calculating delay information for each channel in a beamforming configuration. The design consisted of only 8 adders and 8 registers per channel but limits the image resolution [8]. In [9], an analog dynamic delay-and-sum beamformer was proposed for high frequency ultrasonic imagers. The method used a current-mode first-order all-pass filter topology with an enhancement technique on the current mirrors to increase the bandwidth. Although this method dissipated relatively low power for higher frequency

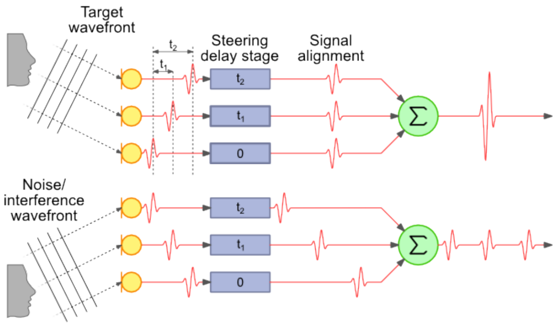


Fig. 1: Diagram of Typical DAS Digital Beamformer

systems, the analog beamformer required considerably more area.

The increased complexity of ultrasonic systems coupled with a growing trend in mobile ultrasonic applications creates a need for low power, small area beamforming with adequate accuracy. Although prior works demonstrate beamforming techniques that manipulate these tradeoffs, an optimal beamforming solution for mobile ultrasound applications has not been explored.

B. Approximate Compute Tradeoffs

When designing with approximate computing techniques the main trade off is between accuracy and power. A designer must consider how much accuracy can be compromised before the result of the computation is unusable. Another metric that is not often considered is the NRE cost due to the lack of tool support for designing inexact circuits. Adders and multipliers provided in most PDKs must be replaced with hand tuned approximate configurations. Despite these challenges, many groups have successfully implemented numerous algorithms with low precision hardware. For instance, one group was able to implement a 560 nW heartbeat detection and classification circuit by using variable precision approximate compute adders [10].

When applied to beamforming in mobile ultrasonic applications, the inaccuracies introduced by AC must not mitigate the resolution improvements due to beamforming. In other words, AC beamforming integration must provided enough resolution improvement to justify the increased power and area caused by the added beamformer hardware.

III. Solution

In this project, a method for beamforming is proposed using approximate compute arithmetic blocks. Implementing beamforming with AC inherently reduces power and area at the expense of accuracy; however, the reduced resolution of a beamforming solution with AC may be suitable for mobile applications. Therefore, the goal of this work is to identify if AC beamforming integration presents an acceptable solution for ultrasonic mobile applications.

Delay-and-sum (DAS) beamforming is a conventional technique in medical ultrasound imaging. Depicted in figure 1, this technique delays a received signal by array elements appropriate to the distances from the main target of the imaging and then sums the delayed signals to construct the echo signal originating from the main target. By summing the received signals with the appropriate delays, the signal is amplified by the number of receivers and the signal to noise ratio of the ultrasound imager is improved. Delay and sum beamforming provides a simple yet effective solution to improving signal resolution while providing a framework to explore low power beamforming techniques with approximate computing [11].

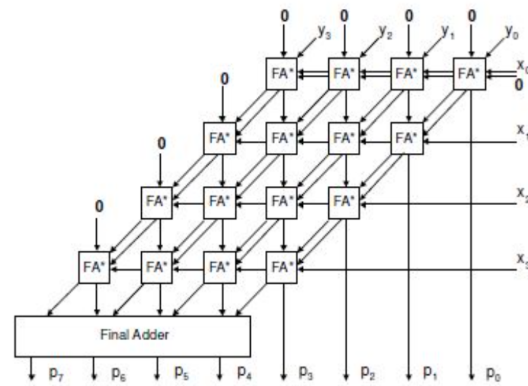


Fig. 2: Carry Save Multiplier

A set of full adder cells that employ approximate computing techniques will be designed. These include but are not limited to a 6 transistor XOR adder that is accurate for 4 of 8 inputs, and an 8 transistor XOR based adder that is accurate for 6 out of 8 inputs. These full adder cells will be used in ripple-carry adders, carry-lookahead adders, and multipliers.

We hope that the use of approximate computing will result in the power savings necessary for modern digital beamforming. For low precision applications with a low energy budget, the authors expect that approximate computing is a viable option.

IV. Experiment

The purpose of this project was to determine if delay and sum beamforming implemented with approximate compute is a viable option for mobile ultrasound applications. To determine this, multiple DAS beamformers were designed in the 28/32nm technology utilizing varying degrees of approximation. The following approximate compute arithmetic blocks were implemented: the 8T XOR adder, the 6T XNOR adder, and the 8T XNOR adder. The DAS beamformer was designed in a modular fashion such that arithmetic blocks were interchanged for easy comparison of accuracy versus the number of bits of approximation for each adder cell. All multiplications were computed with a 24 bit carry save multiplier with a ripple carry output stage for a mantissa operation in a floating point unit. A 4 bit carry save multiplier is shown in figure 2.

Multiple simulations were executed replacing n full adder cells with approximate adders in each operand circuit. The power, area, and image resolution of each implementation was analyzed.

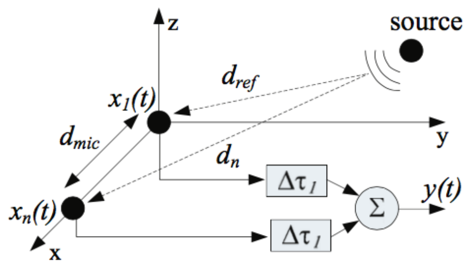


Fig. 3: Delay and sum beamforming with two elements

A. Delay and Sum Beamforming

The method for delay and sum beamforming is described in [12]. Delay and sum beamforming is achieved by compensating signal delay to each transducer appropriately before summing the signals to achieve improved SNR. For simplicity, the signal source is assumed to be sufficiently far from the transducer array such that the wavefront is effectively flat. Additionally, the attenuation of the signals as it travels from the source to the transducers are not taken into consideration. Figure 3 depicts the situation in which a desired signal is received by 2 transducers at time t. In a transducer array, each element will interpret a delayed version of the original signal $s(t-\tau_n)$ and noise v_n as described in equation 1.

$$x_n(t) = s(t-\tau_n) + v_n(t) \tag{1}$$

In the frequency domain, the signal is represented by equation 2

$$\mathbf{X}(\omega) = S(\omega)\mathbf{d} + \mathbf{V}(\omega) \tag{2}$$

where $\mathbf{X} = [X_1(\omega), X_1(\omega), ..., X_N(\omega)]$ and $\mathbf{V} = [V_1(\omega), V_1(\omega), ..., V_N(\omega)]$. The vector $\mathbf{d}$ represents the array steering vector. This steering vector depends on the transducer array and signal source locations. The steering vector is described by:

$$\mathbf{d} = [e^{-j\,\omega\tau_1}, e^{-j\,\omega\tau_2}, ..., e^{-j\,\omega\tau_N}] \tag{3}$$

$$\tau_N = \frac{d_n - d_{ref}}{c} \tag{4}$$

where d_n and d_{ref} represent the Euclidean distance between the source and transducer n, and c is the speed of sound in the transmitting medium. To recover the desired signal, each transducer received response is weighted by a frequency domain coefficient $\omega_n(\omega)$ for the steering angle ($\mathbf{w}^H\mathbf{d} = 1$). Thus, the beamformed output signal is described by the sum of each weighted transducer response:

$$Y(\omega) = \sum_{n=1}^{N} \omega_n^*(\omega)\, X_n(\omega) \tag{5}$$

B. 8T Approximate XOR Adder

The 8 transistor approximate XOR based adder is shown in figure 4a. The outputs that the circuit generates are shown in the equations below:

$$Sum = C_{in}$$
$$C_{out} = \overline{(A \oplus B)C_{in} + \bar{A}\bar{B}}$$

The carry output is regenerative while the Sum output will adopt the noise of the input C_{in}. The truth table for this adder cell is shown in table I where the incorrect outputs are highlighted in red. The adder cell will be designed by sizing gates for minimum average delay across all possible inputs.

C. 6T Approximate XNOR Adder

The 6 transistor Approximate XNOR Adder is implemented with an XNOR gate to generate an approximate sum and a pass transistor style circuit to generate the carry. The circuit diagram for the 6T approximate XNOR adder is shown in figure 4b.

D. 8T Approximate XNOR Adder

The 8 transistor Accurate XNOR Adder (AXA3) is shown in figure 4c. The circuit consists of a 4 transistor XNOR gate fed into two pass transistors to generate the sum and carry signals.

The truth table for this adder is shown in table I. This adder cell has the least number of errors across all possible inputs.

V. Results

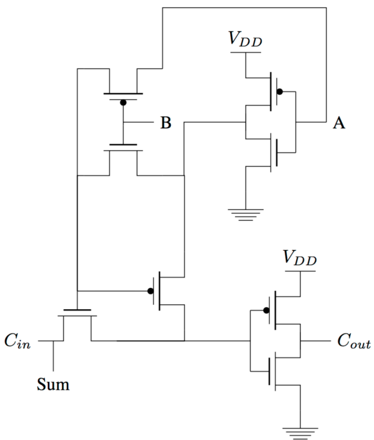
A. Steered Response Accuracy

The delay and sum beamformer was used to generate the steered response for the target signal with varying amounts of approximation. The steered response of the DAS beamformer describes the the power of the beamformer output in the frequency domain as a function of the steering vector. Figure 5a, 5b, and 5c shows the steered responses of the delay and sum beamformer as the number of bits using AXA1, AXA2, and AXA3 cells in the carry save multiplier varies.

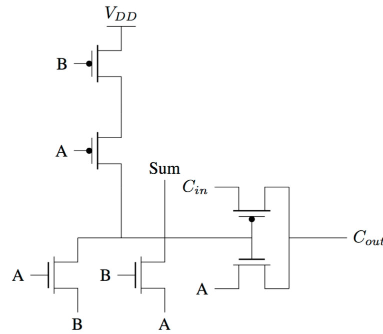
For all approximate adders, tolerable error is observed with up to 77.3% of the full adders in the carry save multipliers replaced with approximate adders. Intolerable distortion is observed when 89.6% of the full adders in the carry save multipliers are replaced. Out of the three approximate adders analyzed, AXA1 showed the most distortion while AXA3 showed the least distortion. These results agree with the error rate described by each approximate adder's truth table.

B. Delay and Sum Beamformer with Optimal Approximate Compute for Mobile Application

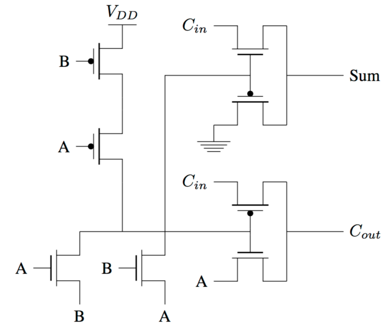
The delay and sum beamformer with various amounts of approximation for each approximate adder unit was applied to experimental ultrasound data with simulated noise and delays. RF data was collected from the ultrasonic fingerprint sensor at UC Berkeley. The sensor consists of a transducer array of 56 x 110 rectangular piezoelectric micromachined



(a) 8T AXA1



(b) 6T AXA2



(c) 8T AXA3

Fig. 4: Approximate Full Adder Cells

AXA1					AXA2					AXA3				
A	B	C_{in}	C_{out}	Sum	A	B	C_{in}	C_{out}	Sum	A	B	C_{in}	C_{out}	Sum
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	1	0	1	0	0	1	0	1
0	1	0	1	0	0	1	0	0	0	0	1	0	0	0
0	1	1	0	1	0	1	1	1	0	0	1	1	1	0
1	0	0	1	0	1	0	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	1	1	0	1	0	1	1	0
1	1	0	1	0	1	1	0	1	1	1	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TABLE I: Truth Tables for Approximate Full Adder Cells

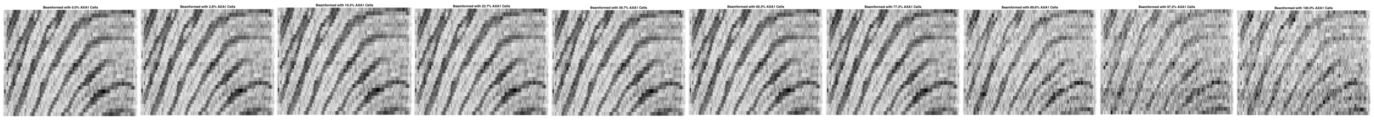
ultrasonic transducers (PMUT) with 14MHz resonance, Q 4, 51.7% fill-factor and 43 and 58m pitch [13]. The ultrasonic fingerprint sensor is a good candidate for approximate (DAS) beamforming because the sensor was designed for mobile applications such as a smartphone. Additionally, the ultrasonic fingerprint sensor has a relatively large sensor array, making area and power a concern. The ultrasound signal was recorded for each transducer in all 110 columns and 28 rows without beamforming. Delays were added to each signal for a signal source placed at the center of the array at a depth of 250 μm. Additionally, Gaussian noise was added to each signal before beamforming.

The delay and sum beamformers were applied to the ultrasound signal data for each approximate adder for various amounts of approximation. The resulting images are displayed in table III, IV, V for AXA1, AXA2, and AXA3, respectively. As demonstrated by the steered responses for each approximate adder, the tolerable amount of approximation occurs when 77.3% of full adders are replaced with approximate adders.

Simulations of each approximate adder cell were performed in Cadence's HPSICE in Synopsys' 28/32 nm process, for which 1.05V is used as the standard supply. Since dynamic power is significantly larger than static power, the dynamic power of AXA1, AXA2, AXA3, and a standard full adder cell were found by integrating the product of the current from a voltage source and the supply voltage during the transition interval at the beamformer's frequency of operation (100 MHz). To accomplish this, all 64 transitions for different input combinations were considered. The number of full adders used in a single delay calculation unit was reported by Synopys' Design Compiler (DC) to be 1211 full adder units. Based on the number of full adders in single element delay calculation, the total power saved for each approximate adder with highest acceptable approximation was found for a single delay unit and the the example ultrasonic fingerprint sensor. Table II summarizes the power comparison of each adder cell and describes the power saving for a single element and the example ultrasonic fingerprint sensor.

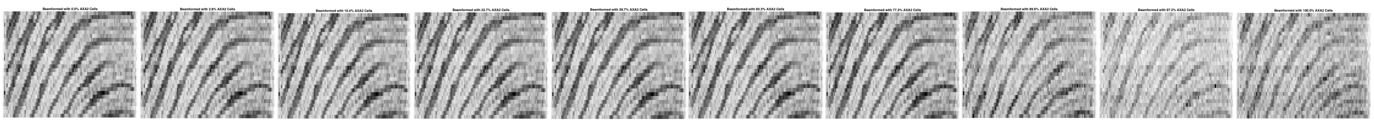
Adder	FA	AXA1	AXA2	AXA3
Dynamic Power per adder [nW]	173	24.2883	14.2386	10.2828
Power savings with 77.3 % approx adders per array element [μW]	N/A	139.201	148.617	152.320
Total Power savings for fingerprint sensor [mW]	N/A	15.3130	16.3479	16.7552

TABLE II: Power summary for approximate delay-and-sum beamforming



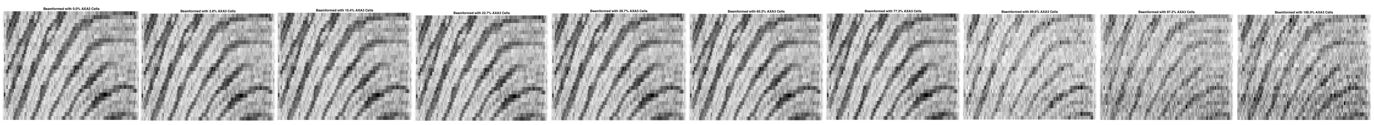
0% 2.8% 10.4% 22.7% 39.7% 60.3% 77.3% 89.3% 97.2% 100%

TABLE III: Beamformed Ultrasound Fingerprint Images using AXA1 with Decreasing Accuracy. Percent of approximate adders shown below.



0% 2.8% 10.4% 22.7% 39.7% 60.3% 77.3% 89.3% 97.2% 100%

TABLE IV: Beamformed Ultrasound Fingerprint Images using AXA2 with Decreasing Accuracy. Percent of approximate adders shown below.



0% 2.8% 10.4% 22.7% 39.7% 60.3% 77.3% 89.3% 97.2% 100%

TABLE V: Beamformed Ultrasound Fingerprint Images using AXA3 with Decreasing Accuracy. Percent of approximate adders shown below.

C. Area Savings

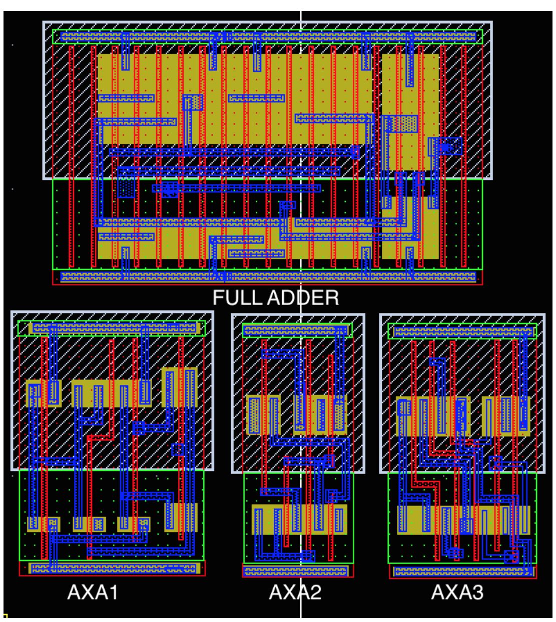


Fig. 7: Layout comparison of full adder and approximate adders

Each approximate adder designed in Cadence Layout using the 28/32nm process. The comparison of the layouts and area for each approximate adder and full adder cell are shown in figure 7 and summarized in table VI.

The authors estimate that the area savings for a full beamforming system are around 6-8% of the total die area.

Adder	FA	AXA1	AXA2	AXA3
Cell Area [μm^2]	5.712	2.568	1.687	2.63
Area Savings with 77.3 % approx adders per array element [μm^2]	N/A	2,943.1	3,767.8	2,885.1
Total Area savings for fingerprint sensor [mm^2]	N/A	0.3237	0.41428	0.31735

TABLE VI: Area Summary for Approximate Adder Cells

VI. Conclusion

Delay and sum implemented with approximate computing adders offers a potentially viable beamforming technique for mobile beamforming applications. Up to 77.3 % of approximate adders are tolerable for all three approximate adders analyzed. Although power and area savings are not very significant for one element (up to 152.320μW and 3,767.8μm^2), the savings from approximate delay and sum beamforming becomes more relevant as the size of the sensor array increases. The power saving of the ultrasonic fingerprint sensor with 77.3 % of approximation was found to be up to up to 16.7552mW and 0.41428mm^2. Therefore, delay and sum beamforming with approximate computing should be considered as a viable beamforming solution for large array beamformers in mobile applications.

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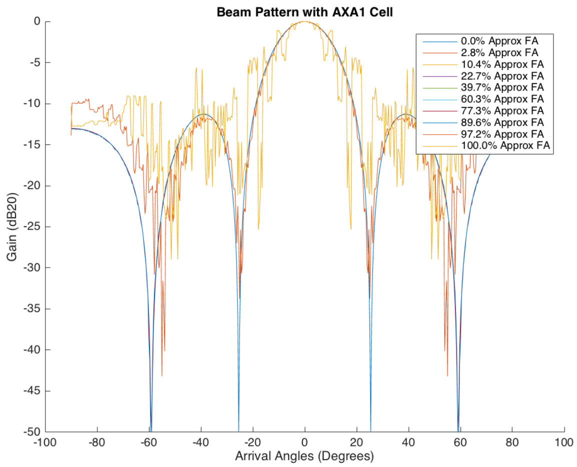
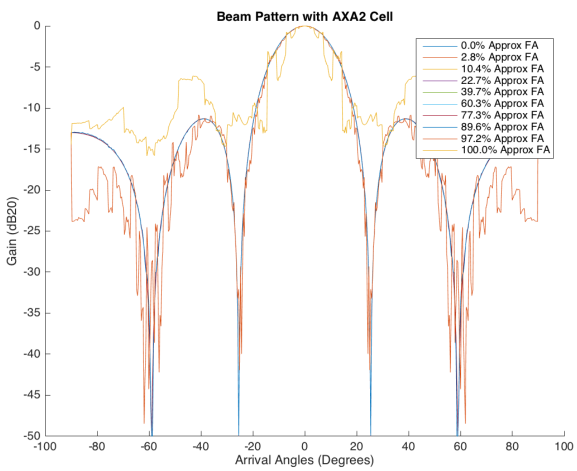
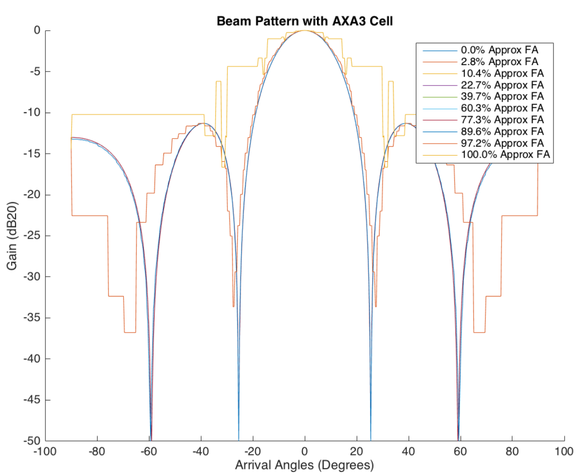


(a)



(b)



(c)

Fig. 5: Steered Response with Varying Levels of Approximation

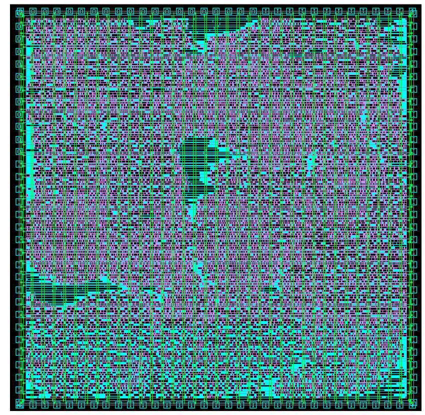


Fig. 6: Layout of Single Delay Calculation Unit

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