Low Power Digital Beamforming with Approximate Compute for Mobile Ultrasound Systems

Josh Kay, Karthik Gopalan

***Abstract*—As the size of 2D transducer arrays for ultrasound systems increase, the hardware complexity, die area, and power of digital beamforming circuits increases by the number of elements squared; moreover, as ultrasonic imaging systems trend toward mobile applications, modern beamforming techniques do not address the growing power and area restrictions demanded by these applications. Approximate computing (AC) introduces a technique to reduce power and area in integrated digital circuits. By implementing an adaptive minimum variance (MV) beamformer with approximate compute arithmetic blocks, lower power and area will be achieved while mitigating image resolution loss compared to conventional delay-and-sum beamformers. An adaptive minimum variance beamformer implemented with approximate compute provides adequate image resolution while minimizing power and area to be beneficial toward mobile ultrasound applications.**

***Index Terms*—Beamforming, Transducer, Approximate Computing, Minimum Variance, Delay-and-Sum.**

I. Introduction

HIGH frequency ultrasound imaging is an effective tool for medical diagnosis due to its non-invasive, real time body imaging capability. Evolution of ultrasonic imaging technology from single element transducers to 2D transducer arrays improved focusing techniques for both the transmitting and receiving operations of the ultrasonic imaging device [1]. Receive focusing is known as beamforming and may be implemented with a series of delays and adders. However, the growing number of elements in 2D ultrasonic imaging devices have greatly increased the rate at which data needs to be transmitted from the system front-end and processed by the beamformer. Additionally, the increase in transmission and processing rates have greatly increased circuit area and power consumption in traditional digital beamformers [2]. These shortcomings become increasingly more prevalent as ultrasonic imaging devices transition to mobile platforms [3].

Approximate computing (AC) has recently emerged as a promising technique for reducing power and area in digital integrated circuits. The principle behind AC is using deterministic hardware that will produce low order errors but can be built with much fewer resources. For example, adder cells can be designed with only 10 transistors by utilizing XOR/XNOR gates and pass transistor style muxes [4]. The use of pass transistors in these adders reduces the noise margin and can therefore produce less accurate results compared to a conventional CMOS adder which uses 28 transistors. Han et. al implemented an inverse discrete cosine transform algorithm with approximate adders and simulated a 38% energy savings compared to an exact computation [5].

Beamforming implemented with approximate compute offers an attractive solution for mobile ultrasound systems that require low power, small area and only moderate accuracy. This project explores the use of approximate compute techniques for beamforming implementations in mobile ultrasound applications.

Karthik Gopalan and Josh Kay are graduate student researchers at the University of California, Berkeley.

II. Problem Description

A. Area and Power Limitations in Beamforming

Advances in ultrasonic imaging system technology have enabled larger transducer arrays, resulting in greater control of delay and weighting of each array element for receive beamforming. Beamforming enables dynamic scan depth focusing as opposed to fixed focal lengths of single element transducer systems [6]. However, more elements in transducer arrays inherently produce beamforming architectures that suffer from increased area and power dissipation. This increase in power and area is compounded by the desire for higher resolution images that demand higher transmission and image processing rates. A push toward mobile applications has put increasing pressure on ultrasonic imaging systems to be low power while occupying smaller area. Therefore, emerging beamforming techniques must maintain high quality imaging while minimizing power dissipation and area.

Modern beamforming techniques attempt to remedy the tradeoffs between power and resolution and between area and resolution through various techniques. Wagner reduced power dissipation by reducing processing rates in a technique describe as compressed beamforming. In compressed beamforming, low power is achieved by beamforming the sub-Nyquist samples obtained from multiple transducer elements; however, increased beamformer complexity translated to greater area when implemented on chip [7]. Feldkamper proposed a low power iterative algorithm for calculating delay information for each channel in a beamforming configuration. The design consisted of only 8 adders and 8 registers per channel but limits the image resolution [8]. In [9], an analog dynamic delay-and-sum beamformer was proposed for high frequency ultrasonic imagers. The method used a current-mode first-order all-pass filter topology with an enhancement technique on the current mirrors to increase the bandwidth. Although this

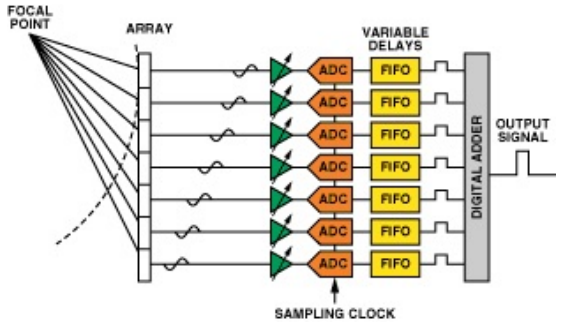

Fig. 1. Block Diagram of typical DAS Digital Beamformer

method dissipated relatively low power for higher frequency systems, the analog beamformer required considerably more area.

The increased complexity of ultrasonic systems coupled with a growing trend in mobile ultrasonic applications creates a need for low power, small area beamforming with adequate accuracy. Although prior works demonstrate beamforming techniques that manipulate these tradeoffs, an optimal beamforming solution for mobile ultrasound applications has not been explored.

B. Approximate Compute Tradeoffs

When designing with approximate computing techniques the main trade off is between accuracy and power. A designer must consider how much accuracy can be compromised before the result of the computation is unusable. Another metric that is not often considered is the NRE cost due to the lack of tool support for designing inexact circuits. Adders and multipliers provided in most PDKs must be replaced with hand tuned approximate configurations. Despite these challenges, many groups have successfully implemented numerous algorithms with low precision hardware. For instance, one group was able to implement a 560 nW heartbeat detection and classification circuit by using variable precision approximate compute adders [10].

When applied to beamforming in mobile ultrasonic applications, the inaccuracies introduced by AC must not mitigate the resolution improvements due to beamforming. In other words, AC beamforming integration must provided enough resolution improvement to justify the increased power and area caused by the added beamformer hardware.

III. Solution

In this project, a method for beamforming is proposed using approximate compute arithmetic blocks. Implementing beamforming with AC inherently reduces power and area at the expense of accuracy; however, the reduced resolution of a beamforming solution with AC may be suitable for mobile applications. Therefore, the goal of this work is to identify if AC beamforming integration presents an acceptable solution for ultrasonic mobile applications.

Delay-and-sum (DAS) beamforming is a conventional technique in medical ultrasound imaging. Depicted in figure 1, this technique delays a received signal by array elements appropriate to the distances from the main target of the imaging and then sums the delayed signals to construct the echo signal originating from the main target. Although this technique for beamforming is common in medical ultrasound systems due to its simplicity, DAS is a non-adaptive beamforming. Consequently, DAS beamformed signals have large side lobes, resulting in low resolution and weak suppression of interfering signals. Therefore, traditional DAS beamformers will not be suitable for an AC beamformer implementation due to the expected degradation in resolution from AC inaccuracies. To combat the expected errors from the approximate compute arithmetic blocks, an adaptive minimum variance (MV) beamforming technique will be implemented. The improved resolution from MV beamforming will forgive some of the inaccuracies due to AC [11].

A set of full adder cells that employ approximate computing techniques will be designed. These include but are not limited to an accurate XNOR based adder with pass transistors, a 6 transistor XOR adder that is accurate for 4 of 8 inputs, and an 8 transistor XOR based adder that is accurate for 6 out of 8 inputs. These full adder cells will be used in ripple-carry adders, carry-lookahead adders, and multipliers.

We hope that the use of approximate computing will result in the power savings necessary for modern digital beamforming. For low precision applications with a low energy budget, the authors expect that approximate computing is a viable option.

IV. Experiment

The purpose of this project is to determine if adaptive minimum variance beamforming implemented with approximate compute is a viable option for mobile ultrasound applications. To determine this, two MV beamformer will be designed in the 28/32nm technology: one design implemented with AC arithmetic blocks and one design implemented with exact arithmetic blocks. The following approximate compute arithmetic blocks will be implemented: the 8T XOR adder, the 6T XNOR adder, and the 8T XNOR adder. The MV beamformer will be designed in a modular fashion such that arithmetic blocks can be interchanged for easy comparison. The power, area, and image resolution of each implementation will be anaylzed.

A. Adaptive Minimum Variance Beamforming

The method for adpative MV beamforming is described in [11]. A transducer is assumed to contain an array of M, where each element records a signal $x_m(t)$. $P+1$ scatterers will be considered with each scatterer with a reflected signal $s_p(t)$. $s_0(t)$ describes the signal that originated from the focal point of the receiver. Under these assumptions, equation 1 describes the mth time-delayed channel.

$$x_m(t) = \frac{1}{r_{m,0}}\, s_0(t) + \sum_{p=1}^{P} \frac{1}{r_{m,p}}\, s_p(t) * \delta(t - \tau_{m,p}) + n_m(t) \quad (1)$$

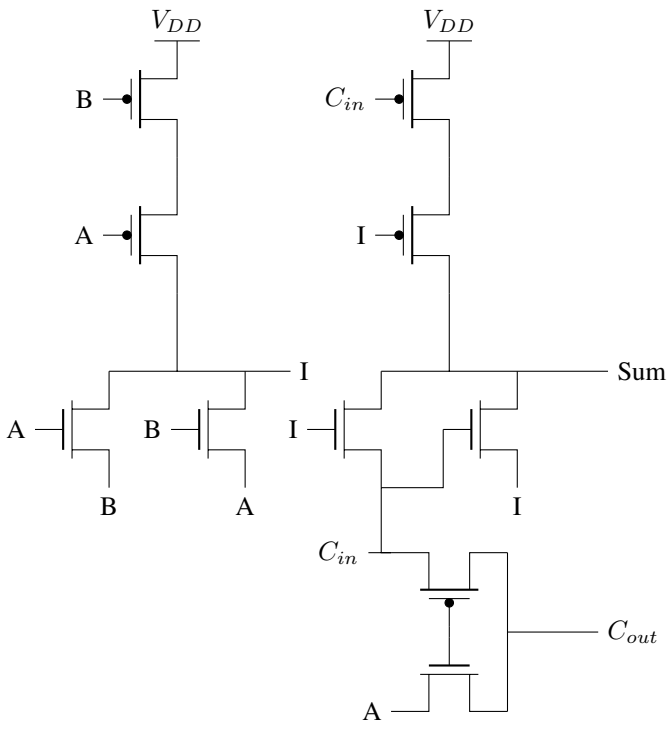

Fig. 2. 10T Accurate XNOR Adder

In equation 1, $r_{m,p}$ is the distance from the reflected object p to the receiver sensor m, $\delta(t)$ is the Dirac delta-function, $\tau_{m,p}$ is the delay from the reflected object p to the receiver sensor m, $n_m(t)$ is the noise on channel m, and $(*)$ is the convolution operator. The M observed time-delays are then ordered in a vector, $\mathbf{X}(t)$. With each channel delayed to focus at a point in the image, the adaptive beamformer computes the the optimal aperature shading before combining the channels. The weighted sum output of the spatial measurements is described by:

$$z(t) = \sum_{m=0}^{M-1} w_m(t) x_m(t) = \mathbf{w}(t)^H \mathbf{X}(t) \tag{2}$$

where $w_m(t)$ is the aperature weight for the sensor m and $\mathbf{w}(t) = [w_0(t) w_1(t) .. w_{M-1}(t)]^H$. The MV achieves minimum variance (power) of $z(t)$ while maintaining unit gain in the focal point. This is achieved by applying the following weights to equation 2:

$$\mathbf{w}(t) = \frac{\mathbf{R}(t)^{-1}\,\mathbf{a}}{\mathbf{a}^H\,\mathbf{R}(t)^{-1}\,\mathbf{a}} \tag{3}$$

where $\mathbf{R}(t)$ is the spatial covariance matrix and $\mathbf{a}$ is a vector of ones.

B. 10T Accurate XNOR Adder

We will design the accurate XNOR based adder shown in figure 2. The gates will be sized in order to minimize average delay across all inputs. The circuit uses two XNOR gates and a set of pass transistors. The node I is internal to the circuit and labelled for clarity. The reader should note that no transistor is tied to the lower supply, therefore the lower noise margins are expected to be worse than the upper noise margins. Verification of the functionality of the circuit is left as an exercise to the reader.

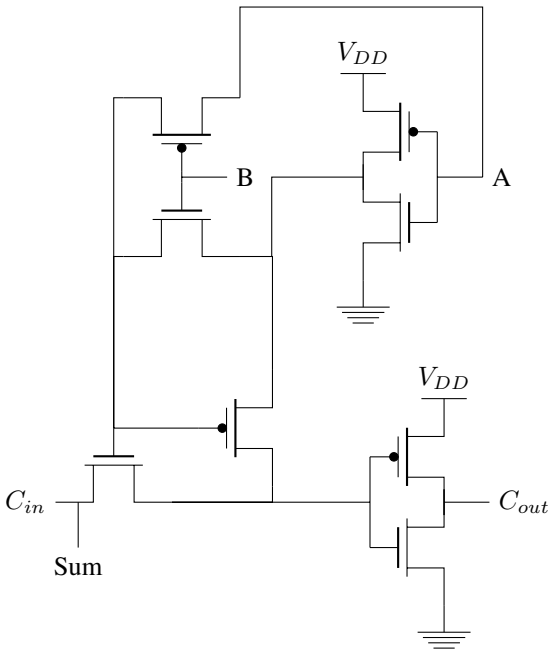

Fig. 3. 8T Approximate XOR Adder (AXA1)

A	B	C_{in}	C_{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

TABLE I
TRUTH TABLE FOR AXA1

C. 8T Approximate XOR Adder

The 8 transistor approximate XOR based adder is shown in figure 3. The outputs that the circuit generates are shown in the equations below:

$$Sum = C_{in}$$
$$C_{out} = \overline{(A \oplus B) C_{in} + \bar{A}\bar{B}}$$

The carry output is regenerative while the Sum output will adopt the noise of the input C_{in}. The truth table for this adder cell is shown in table I where the incorrect outputs are highlighted in red. The adder cell will be designed by sizing gates for minimum average delay across all possible inputs.

D. 6T Approximate XNOR Adder

The 6 transistor Approximate XNOR Adder is implemented with an XNOR gate to generate an approximate sum and a pass transistor style circuit to generate the carry. The circuit diagram for the 6T approximate XNOR adder is shown in figure 4.

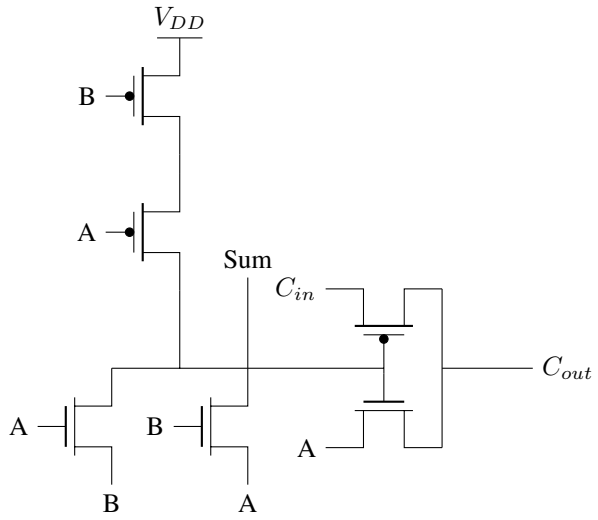

Fig. 4. 6T Approximate XNOR Adder (AXA2) with Pass Transistor Logic

A	B	C_{in}	C_{out}	Sum
0	0	0	0	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

TABLE II
TRUTH TABLE FOR AXA2

E. 8T Approximate XNOR Adder

We will design and layout the 8 transistor Accurate XNOR Adder (AXA3) shown in figure 5. The circuit consists of a 4 transistor XNOR gate fed into two pass transistors to generate the sum and carry signals. The circuit will be designed using the same methods discussed earlier.

The truth table for this adder is shown in table III. This adder cell has the least number of errors across all possible inputs.

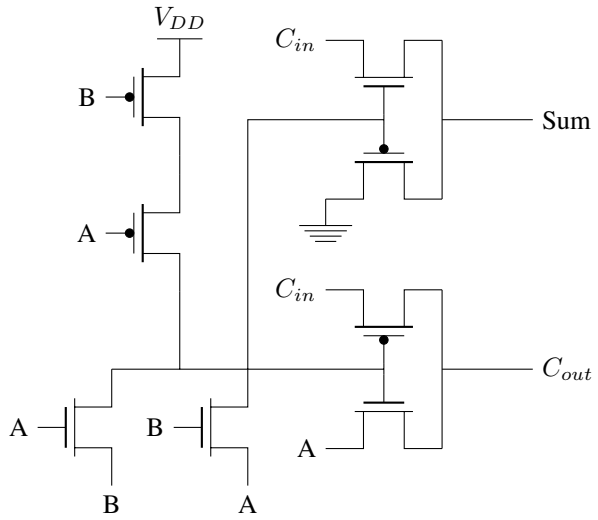

Fig. 5. 8T Approximate XNOR Adder (AXA3) with Pass Transistor Logic

A	B	C_{in}	C_{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

TABLE III
TRUTH TABLE FOR AXA3

V. TECHNIQUE FOR RESULT EVALUATION

In order to evaluate and compare MV beamformer implementations with conventional arithmetic blocks and AC arithmetic blocks, figures of merit must be established. Comparing the value of an exact result to the value of an incorrect result that was computed faster or with less resources is not trivial because traditional verification methods are based on verifying exact implementation. To address this problem, Venkatesan et. al implemented MACACO, a tool used to find bugs in approximate circuits and compare the outputs to those of the exact circuit implementation [12].

We plan to build a digital beamformer with approximate circuits in a 28/32 nm process and compare the power, area, and resolution using MACACO with those of a beamformer built with exact circuits. The resolution of the beamformer will be evaluated by comparing sidelobe power of each implementation. Additionally, the feasibility of MV beamforming implemented with AC will be evaluated for mobile ultrasound applications based on if the method improves image quality at minimal area and power cost. A review of the literature suggests an expected power savings of 30-45% through AC implementation.

VI. CONCLUSION

Adaptive minimum variance beamforming implemented with approximate compute arithmetic blocks provides a promising beamforming technique for mobile ultrasound applications due to expected power and area savings; moreover, minimum variance beamforming intends to improve image resolution despite expected inaccuracies from approximate compute implementation. A MV beamformer will be designed with approximate computing circuits and exact computing blocks. Using MACACO, the accuracy of the AC beamformer and exact beamformer will be compared. Additionally, the power, area, and image resolution of each implementation will be compared. Finally, adaptive minimum variance beamforming implemented with approximate computing will be evaluated as a beamforming solution for mobile applications. By improving image quality at minimal area and power cost, adaptive minimum variance beamforming implemented with approximate compute can improve portability of medical ultrasonic imagers, as well as enable personal health diagnostics.

ACKNOWLEDGMENT

The authors would like to thank...

REFERENCES

[1] J.-Y. Um, E.-W. Song, Y.-J. Kim, S.-E. Cho, M.-K. Chae, J. Song, B. Kim, S. Lee, J. Bang, Y. Kim *et al.*, "24.8 an analog-digital-hybrid single-chip rx beamformer with non-uniform sampling for 2d-cmut ultrasound imaging to achieve wide dynamic range of delay and small chip area," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE, 2014, pp. 426–427.

[2] C.-H. Hu, X.-C. Xu, J. M. Cannata, J. T. Yen, and K. K. Shung, "Development of a real-time, high-frequency ultrasound digital beamformer for high-frequency linear array transducers," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 53, no. 2, pp. 317–323, 2006.

[3] "With $100 million, entrepreneur sees path to disrupt medical imaging," https://www.technologyreview.com/s/532166/with-100-million-entrepreneur-sees-path-to-disrupt-medical-imaging/.

[4] Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate xor/xnor-based adders for inexact computing," in *Nanotechnology (IEEE-NANO), 2013 13th IEEE Conference on*. IEEE, 2013, pp. 690–693.

[5] J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," in *Test Symposium (ETS), 2013 18th IEEE European*. IEEE, 2013, pp. 1–6.

[6] T. L. Szabo, "Diagnostic ultrasound imaging: Inside out," 2004.

[7] N. Wagner, Y. C. Eldar, and Z. Friedman, "Compressed beamforming in ultrasound imaging," *Signal Processing, IEEE Transactions on*, vol. 60, no. 9, pp. 4643–4657, 2012.

[8] H. Feldkämper, R. Schwann, V. Gierenz, and T. Noll, "Low power delay calculation for digital beamforming in handheld ultrasound systems," in *Ultrasonics Symposium, 2000 IEEE*, vol. 2. IEEE, 2000, pp. 1763–1766.

[9] G. Gurun, J. S. Zahorian, A. Sisman, M. Karaman, P. E. Hasler, and F. L. Degertekin, "An analog integrated circuit beamformer for high-frequency medical ultrasound imaging," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 6, no. 5, pp. 454–467, 2012.

[10] R. Amirtharajah and A. P. Chandrakasan, "A micropower programmable dsp using approximate signal processing based on distributed arithmetic," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 2, pp. 337–347, 2004.

[11] J. Synnevag, A. Austeng, and S. Holm, "Adaptive beamforming applied to medical ultrasound imaging," *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control*, vol. 54, no. 8, p. 1606, 2007.

[12] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, "Macaco: Modeling and analysis of circuits for approximate computing," in *Proceedings of the International Conference on Computer-Aided Design*. IEEE Press, 2011, pp. 667–673.

Josh Kay is a graduate student researcher at the University of California, Berkeley. He is pursuing a Ph.D. under the direction of Professor Berhnard Boser. He received his Bachelor of Science degree in Electrical Engineering from the University of California, Santa Barbara in 2014.

Karthik Gopalan is a graduate student researcher at the University of California, Berkeley. He is pursuing a Ph.D. under the direction of Professor Vladimir Stojanović. He received two Bachelor of Science degrees in Physics and Computer Science from the University of Maryland, College Park in 2015.