Design and Implementation of a Low-Power Current-Starved Voltage-Controlled Oscillator (VCO) in 130-nm IHP CMOS Technology Using the eSim Tool Developed by FOSSEE

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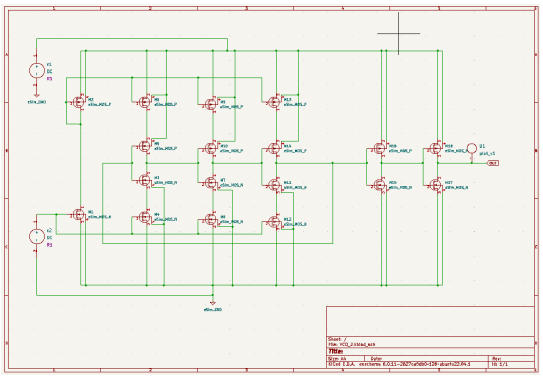
***Abstract*— This paper presents the design and implementation of a three-stage current-starved ring oscillator intended for phase-locked loop (PLL) applications. The proposed voltage-controlled oscillator (VCO) is designed using the 130-nm IHP CMOS technology and implemented in the open-source eSim environment developed by FOSSEE, IIT Bombay. By varying the control voltage from 1.2 V to 3.0 V, the oscillator achieves a frequency tuning range of 120 MHz to 0.99 GHz. The designed VCO exhibits a gain (KVCO) of 496 MHz/V with a center frequency of approximately 550 MHz at a control voltage of 2 V, demonstrating low power consumption and suitability for integration into low-power PLL systems.**

I. INTRODUCTION

A Voltage-Controlled Oscillator (VCO) is an electronic circuit that generates a periodic output signal whose frequency is determined by a control voltage. The oscillation frequency varies proportionally with the applied control voltage, enabling precise frequency modulation. VCOs play a vital role in modern communication systems by providing clock signals for digital circuits and carrier signals for frequency synthesis and transmission. The output frequency of an ideal VCO is a linear function of the control voltage. In practical systems, a variable control voltage is essential to achieve different operating frequencies, making the VCO a key component in frequency-agile designs.

Phase-Locked Loops (PLLs) are among the most common applications of VCOs. In PLL-based frequency synthesizers, widely used in RF transceivers, the VCO provides the tunable frequency required to lock to a reference. For these applications, a wide tuning range and stable oscillation are critical characteristics of VCOs used within PLL architectures.

II. CIRCUIT SCHEMATIC

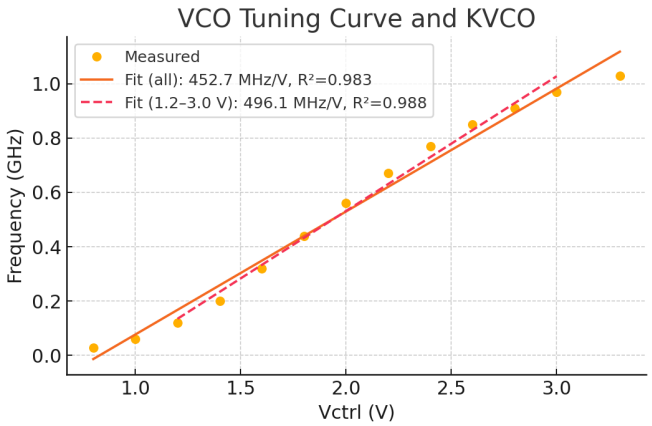


The frequency of oscillation in the proposed design is controlled by the applied control voltage, denoted Vctrl(1.2-3V). The current-starved Voltage-Controlled Oscillator (VCO) is based on a ring oscillator topology, where additional CMOS transistors act as current sources for the inverter stages.

A ring oscillator consists of an odd number of delay stages connected in a loop, with the output of the last stage fed back to the input of the first stage. In the schematic, the middle two transistors form a CMOS inverter, while the upper PMOS and lower NMOS transistors function as current-limiting devices. These transistors regulate the current flowing into the inverter block, effectively 'starving' it of current depending on the applied control voltage Vctrl.

This current-starved configuration provides an advantage of tunability: the oscillation frequency can be varied over a wide range by adjusting the control voltage. As Vctrl increases, the current available to the inverter stages increases, reducing delay and thereby increasing the oscillation frequency.

The circuit was simulated under the typical-typical (TT) process corner using the IHP SG13G2 130-nm high-voltage (HV) device models. Transient analysis was performed in Ngspice using the .tran 20p 100n 0 10p uic command, where the time step was chosen to ensure accurate capture of oscillation frequency and startup behavior. The design files and simulation data are available in the GitHub repository [4].

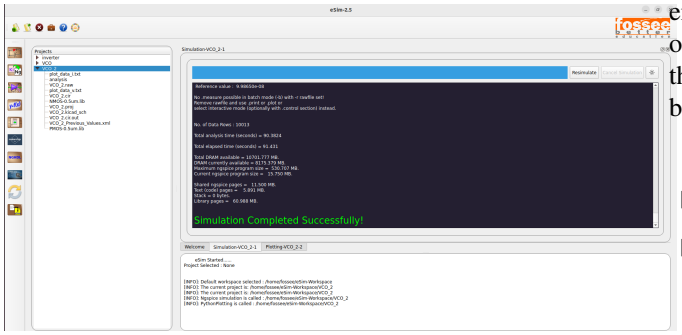


For the dotted line in red, the Vctrl range is 1.2-3.0V For the fit line in orange, the Vctrl range is 0 – 3V. A R(square) value representing linearity is approximately 0.988, which is very close to 1. This high degree of linearity indicates that the VCO exhibits a nearly linear frequency-to-control voltage relationship, indicating that it is suitable for frequency synthesis applications in PLL systems.

A. Specifications

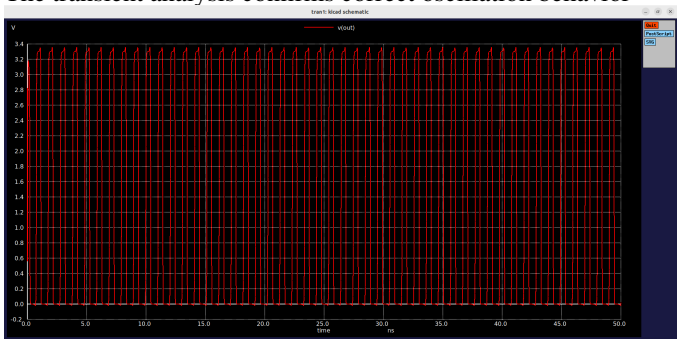
Parameter	Symbol	Value	Remarks
Technology	—	130-nm CMOS	IHP SG13G2
Supply Voltage	VDD	3.3V	HV(High Voltage), thick-oxide CMOS
Operating Temperature Range	T	27C	Characterized at room temperature(-40C to +125C)
Control Voltage	Vctrl	1.2-3V	Maximum linearity observed in this range
Output VCO frequency	Vout	120MHz-1GHz	Maximum frequency of 1.03GHz
Center Frequency	fo	550MHz	@ Vctrl = 2V
Frequency Range	Δf	1 GHz	Wide tuning range
VCO Gain	Kvco	496MHz/V	Linear in 1.2 - 3V range
Power Consumption	P	1.65mW	At VDD=3.3V, Vctrl=2.0V

III. Simulation Results



Simulation using the eSim tool

The transient analysis confirms correct oscillation behavior



Output waveform at Vout.

The transient response converged to a stable oscillation after a brief startup period, consistent with the initialized output node condition of 0.01 V.

IV. Future Scope

Future work will focus on extending the current design to the low-voltage (LV) 1.2 V variant of the IHP SG13G2 process, enabling lower power consumption and compatibility with digital PLL architectures. Further efforts will include detailed phase-noise characterization, which is essential for evaluating timing jitter and spectral purity in PLL systems. Accurate phase-noise performance ensures stable frequency synthesis, minimizes reference spurs, and directly improves the output clock quality in communication and mixed-signal applications.

V. Conclusions

In this work, a VCO with enhanced frequency performance is presented. The circuit achieves a maximum frequency of 1 GHz while consuming only 1.65 mW of power from a 3.3 V DC supply. The center oscillation frequency, currently 550 MHz, is primarily influenced by transistor sizing. These results highlight the potential of the proposed VCO design for integration into phase-locked loops (PLLs) requiring energy efficiency and a wide tuning range. Future integration of this VCO with a charge pump and loop filter will complete the PLL design, enabling closed-loop verification of locking behavior and overall system stability.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 3rd ed. New York, NY, USA: McGraw-Hill, 2016.

[2] A. R. Patil, "Design of Current Starved VCO Using SkyWater 130 nm PDK," *International Research Journal of Engineering and Technology (IRJET)*, vol. 5, no. 3, pp. 1231–1234, Mar. 2018. [Online]. Available: https://www.irjet.net/archives/V5/i3/IRJET-V5I3191.pdf

[3] eSim User Manual, FOSSEE, IIT Bombay. [Online]. Available: https://esim.fossee.in/documentation

[4] Pavan Mantri, "Design files and simulation data for Low-Power Current-Starved VCO in 130-nm IHP CMOS Technology," GitHub repository, 2025. [Online]. Available: https://github.com/pa1mantri/Current_Starved_VCO_IHP