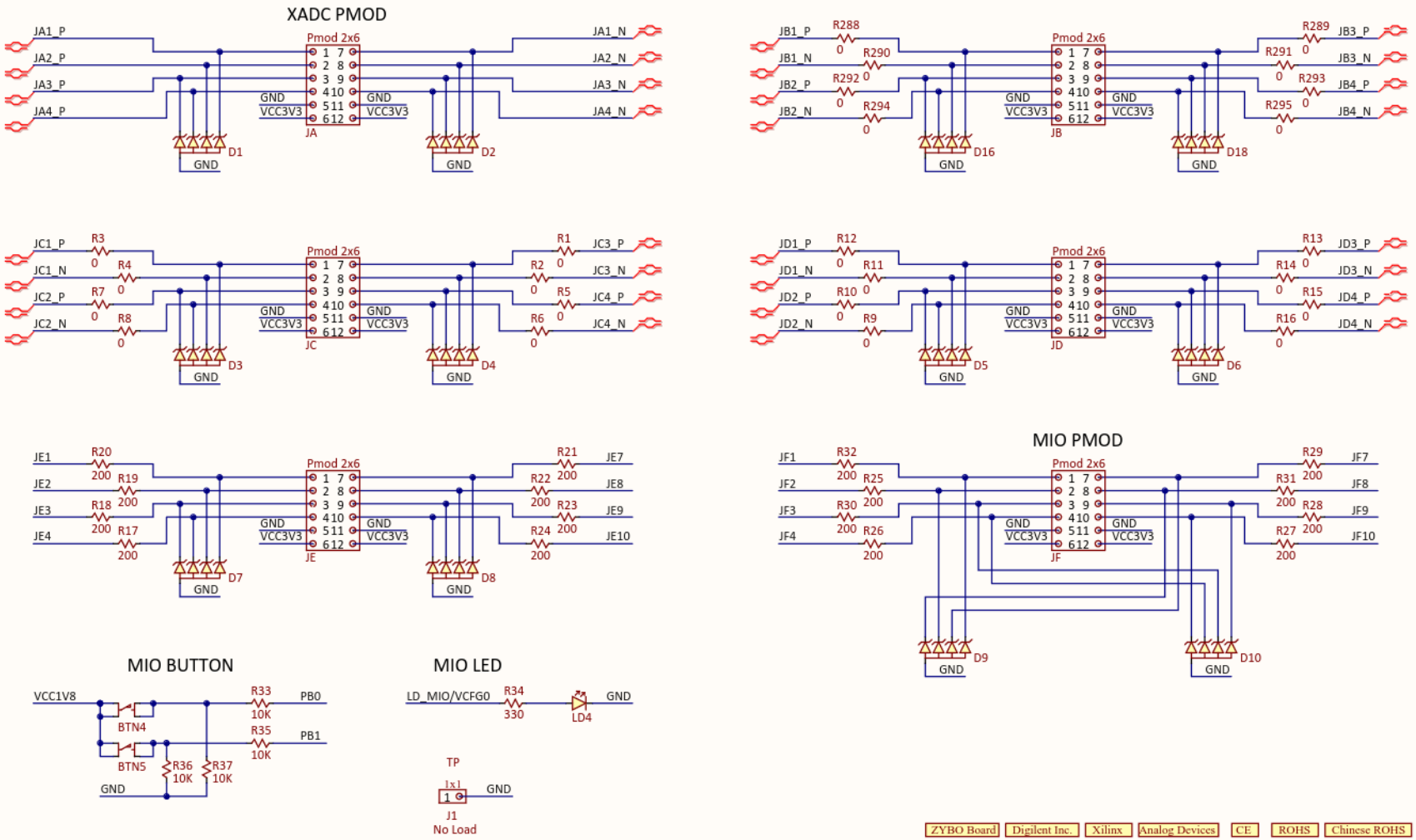
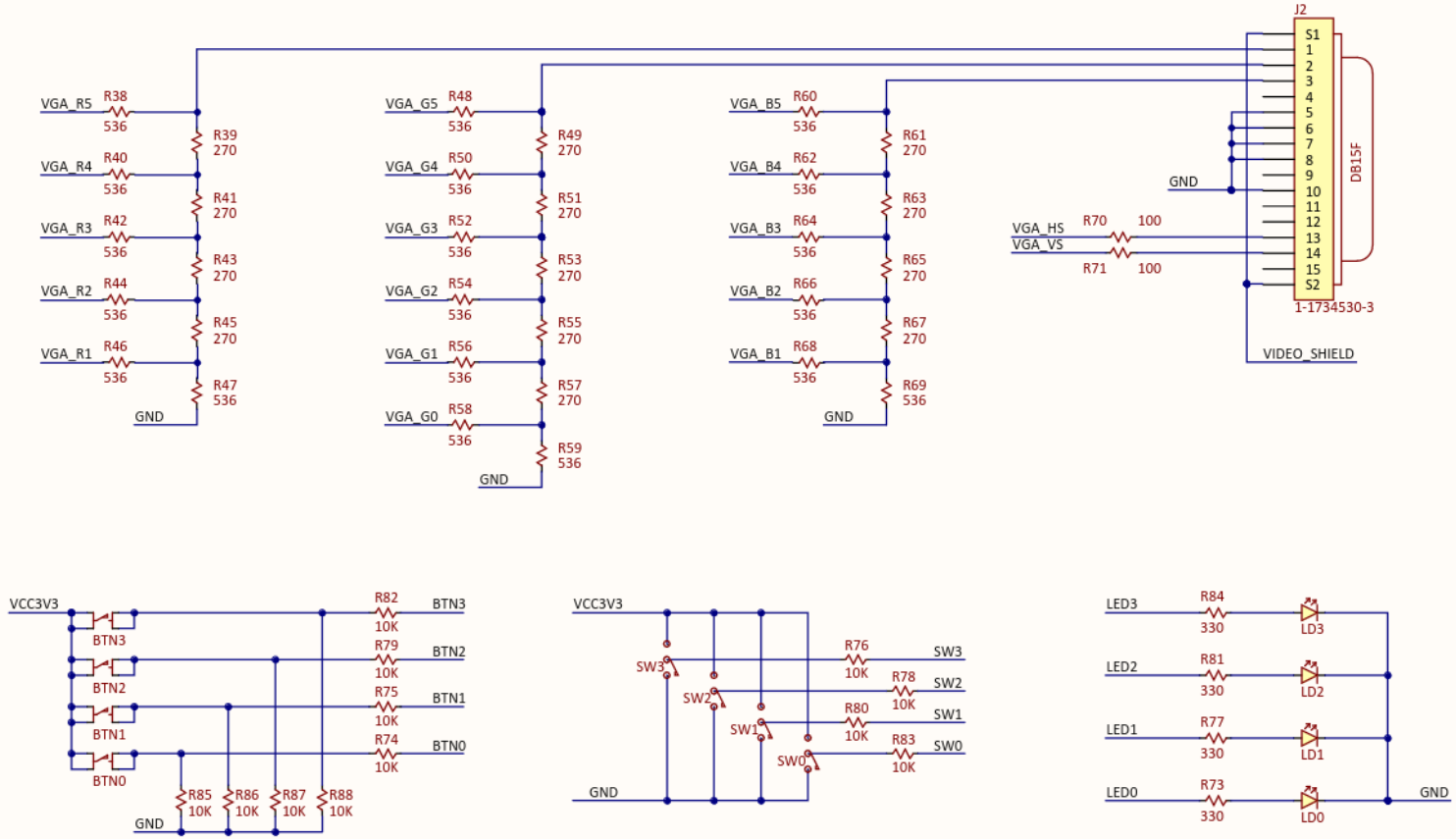
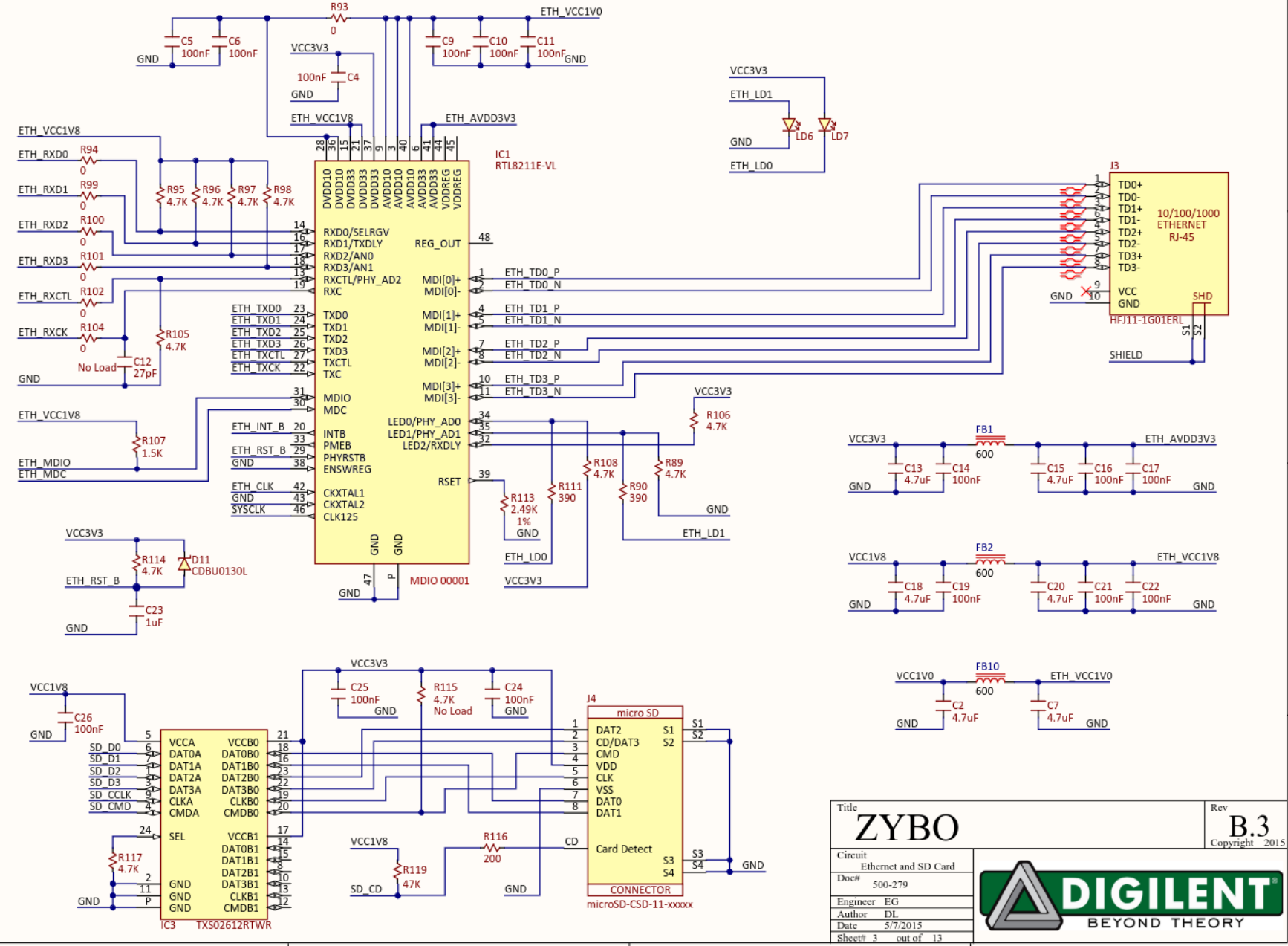

XADC PMOD
JA1_P
JA2_P
JA3_P
JA4_P
Pmod 2x6
GND
VCC3V3
JA
JA1_N
JA2_N
JA3_N
JA4_N
D1
D2
JB1_P
JB1_N
JB2_P
JB2_N
R288
R290
R292
R294
JB
R289
R291
R293
R295
JB3_P
JB3_N
JB4_P
JB4_N
D16
D18
JC1_P
JC1_N
JC2_P
JC2_N
R3
R4
R7
R8
JC
R1
R2
R5
R6
JC3_P
JC3_N
JC4_P
JC4_N
D3
D4
JD1_P
JD1_N
JD2_P
JD2_N
R12
R11
R10
R9
JD
R13
R14
R15
R16
JD3_P
JD3_N
JD4_P
JD4_N
D5
D6
JE1
JE2
JE3
JE4
R20
R19
R18
R17
JE
R21
R22
R23
R24
JE7
JE8
JE9
JE10
D7
D8
MIO PMOD
JF1
JF2
JF3
JF4
R32
R25
R30
R26
JF
R29
R31
R28
R27
JF7
JF8
JF9
JF10
D9
D10
MIO BUTTON
VCC1V8
BTN4
BTN5
R33
R35
R36
R37
10K
PB0
PB1
MIO LED
LD_MIO/VCFG0
R34
330
LD4
TP
1x1
J1
No Load
ZYBO Board
Digilent Inc.
Xilinx
Analog Devices
CE
ROHS
Chinese ROHS
Foot
F1
F2
F3
F4
Title
ZYBO
Rev
B.3
Copyright 2015
Circuit
PMODs, MIO
Doc#
500-279
Engineer EG
Author DL
Date 5/7/2015
Sheet# 1 out of 13
DIGILENT
BEYOND THEORY



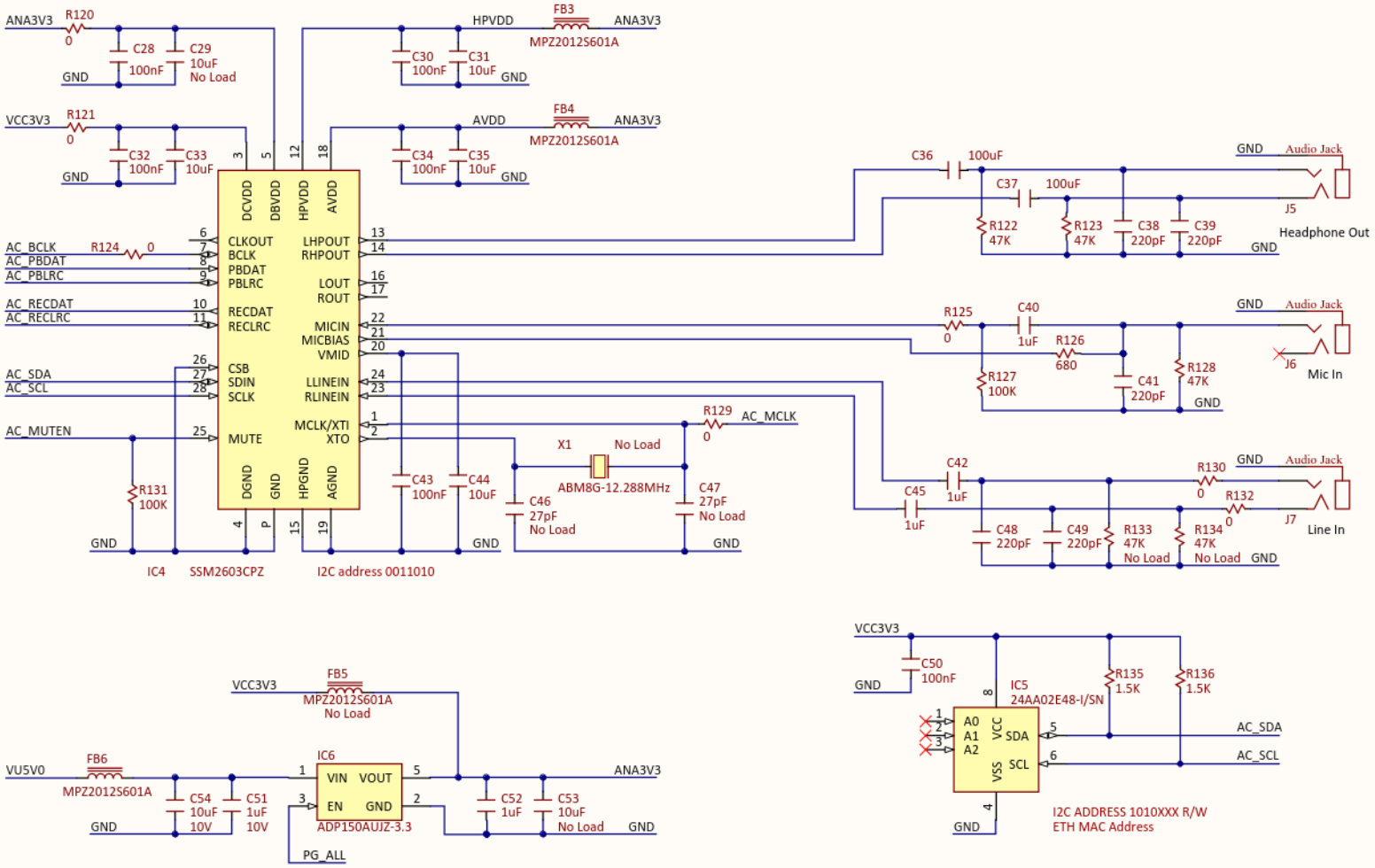
Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	VGA, General I/O
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	2 out of 13

DIGILENT BEYOND THEORY



Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	Ethernet and SD Card
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	3 out of 13

DIGILENT BEYOND THEORY



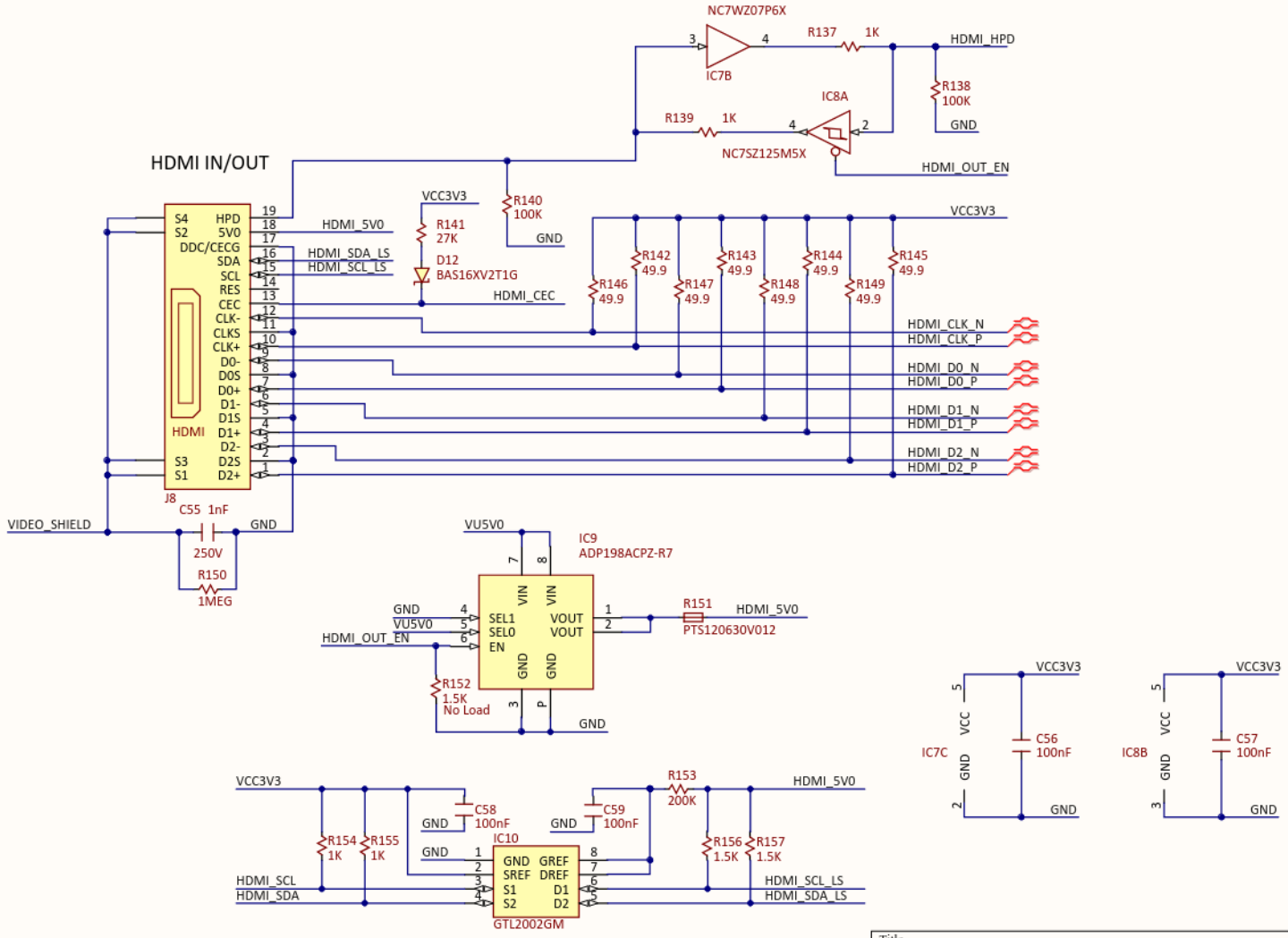
For more information on the parts used in this design, please refer to:

www.analog.com/ssm2603 (Low Power Audio Codec)

www.analog.com/adp150 (Ultra Low Noise, 150 mA CMOS Linear Regulator)

Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	Audio Codec, EUI EEPROM
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	4 out of 13

DIGILENT BEYOND THEORY

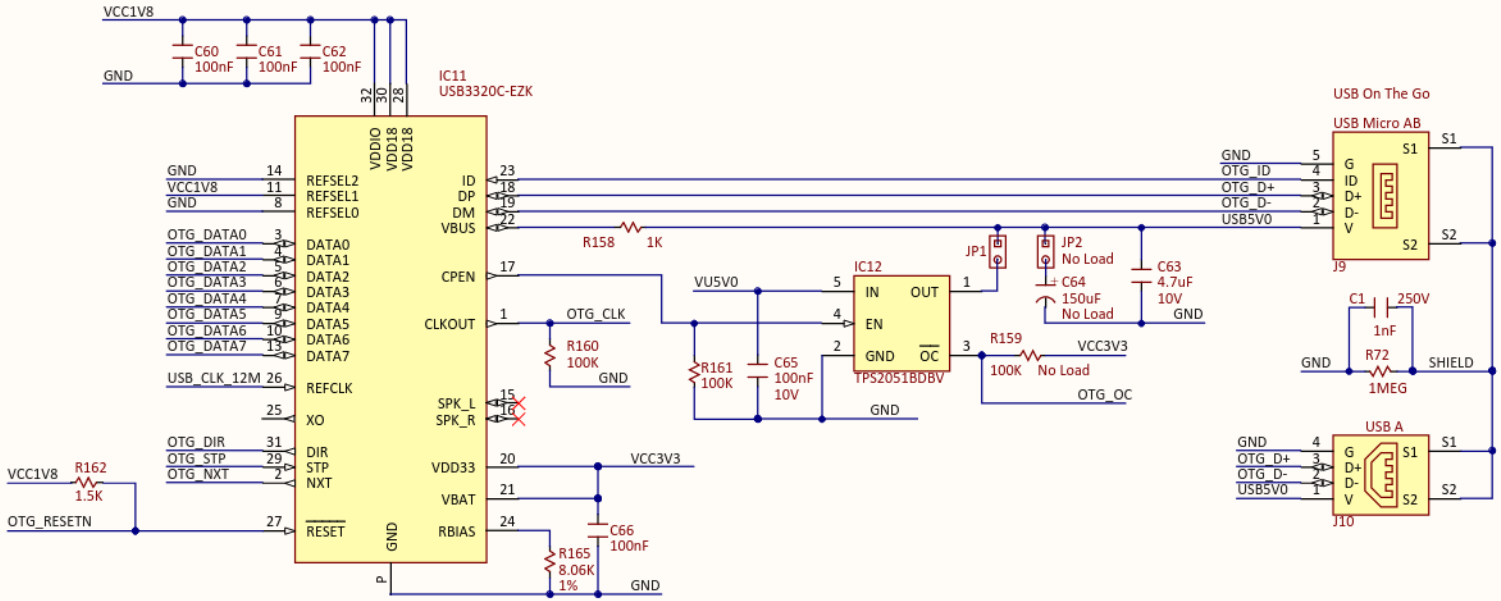


For more information on the parts used in this design, please refer to:

www.analog.com/adp198 (Logic Controlled, 1 A, High-Side Load Switch with Reverse Current Blocking)

Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	HDMI
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	5 out of 13

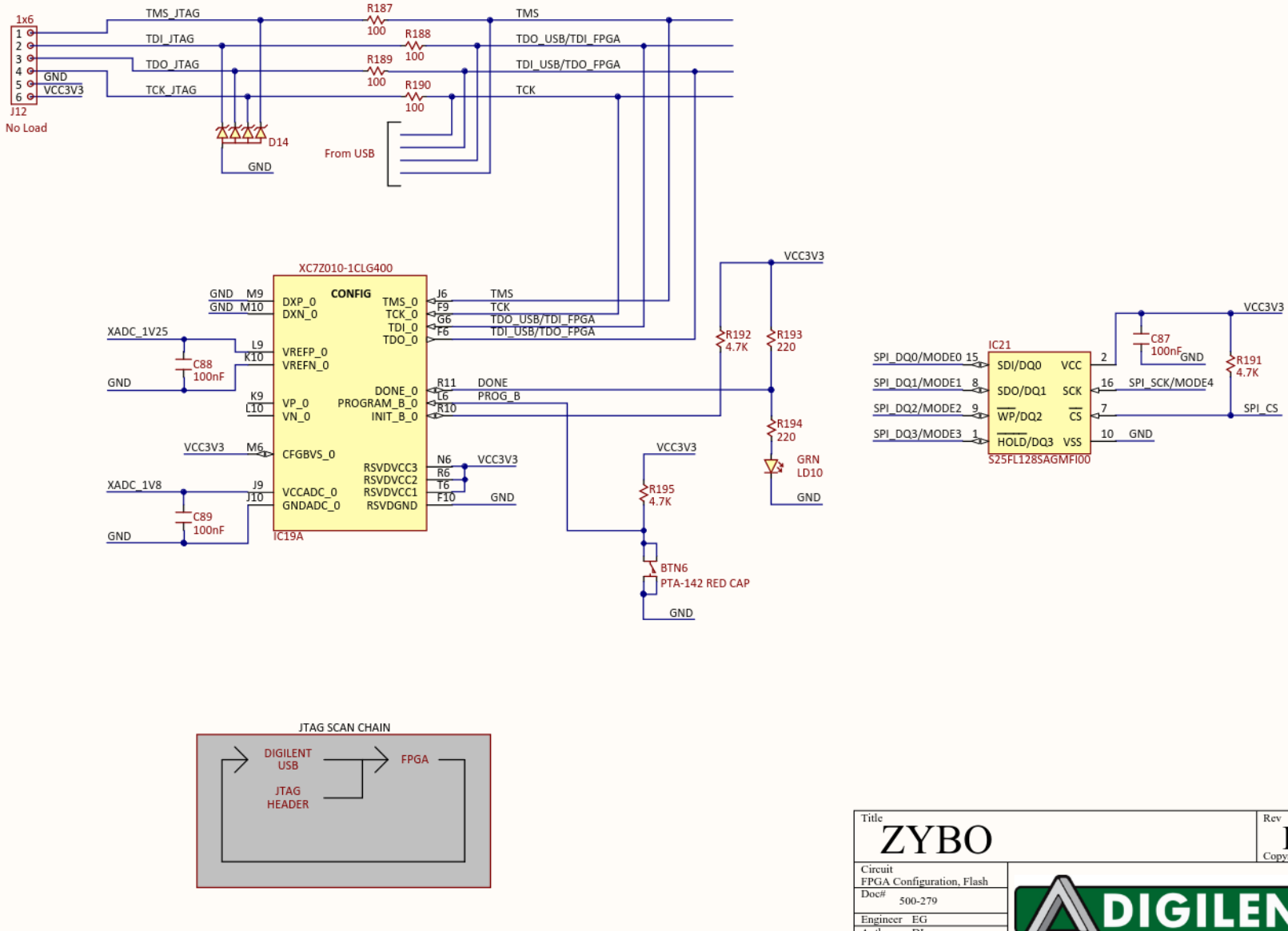
DIGILENT BEYOND THEORY



Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	USB OTG
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	6 out of 13

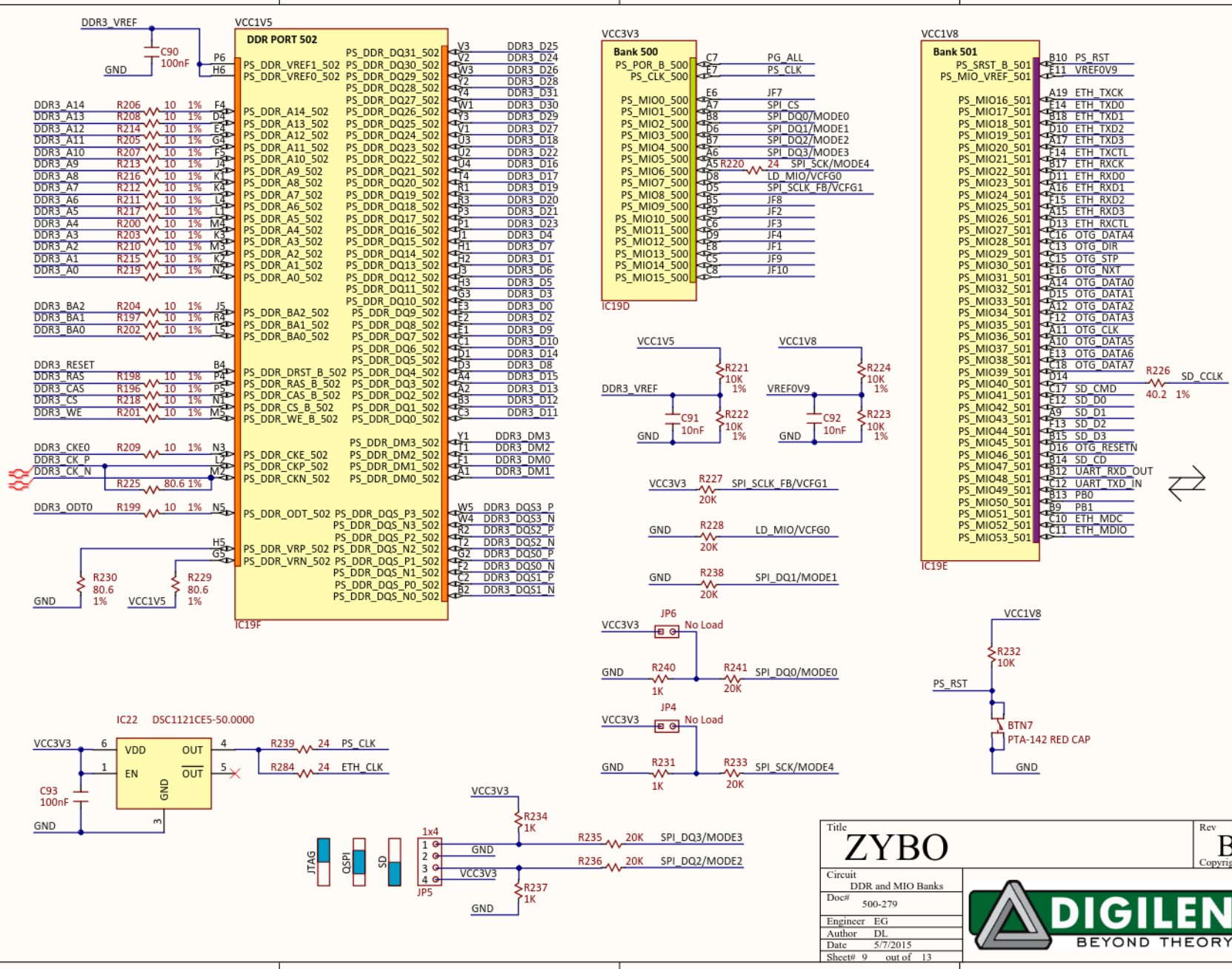
DIGILENT BEYOND THEORY

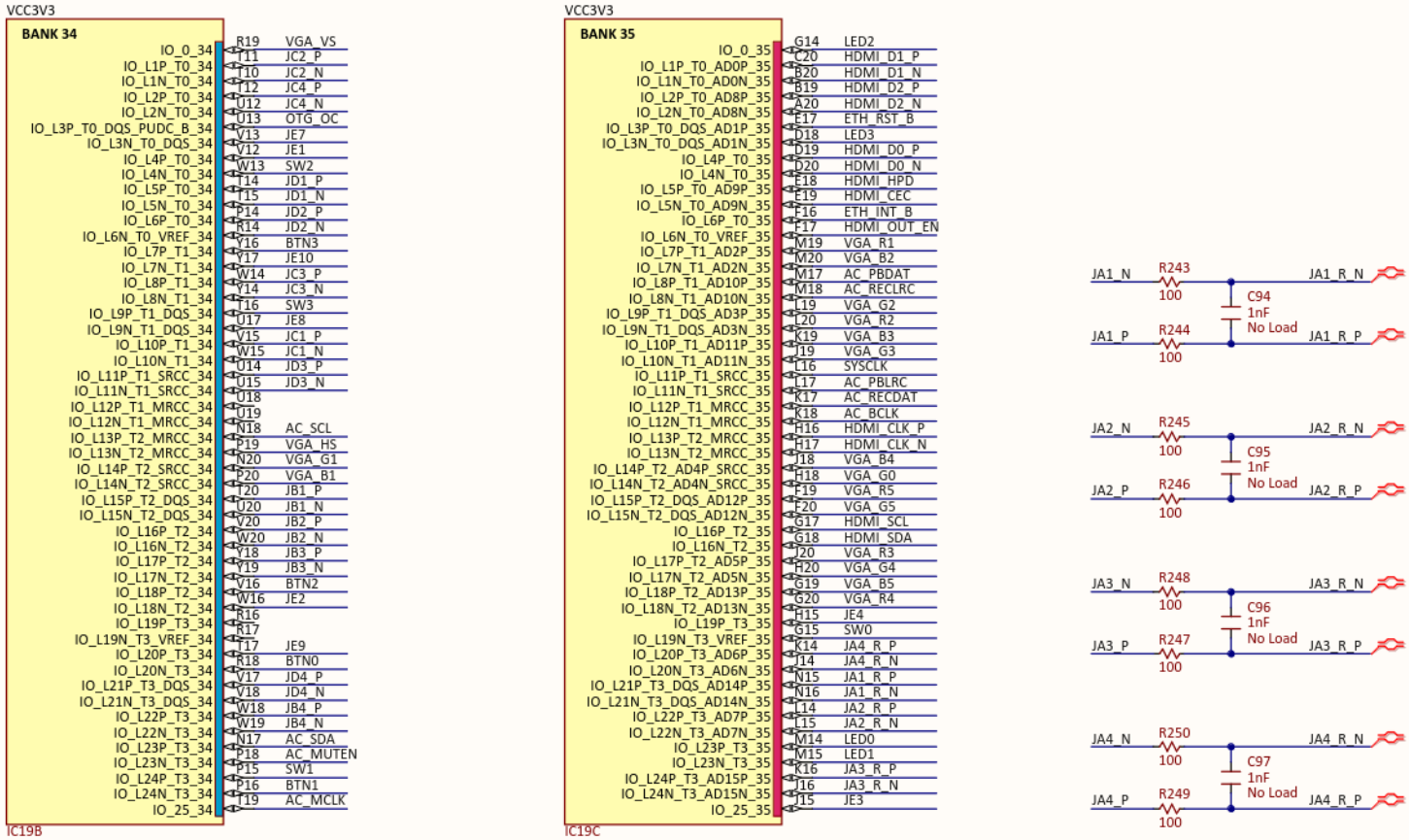
This page intentionally left blank.



Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	FPGA Configuration, Flash
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	8 out of 13

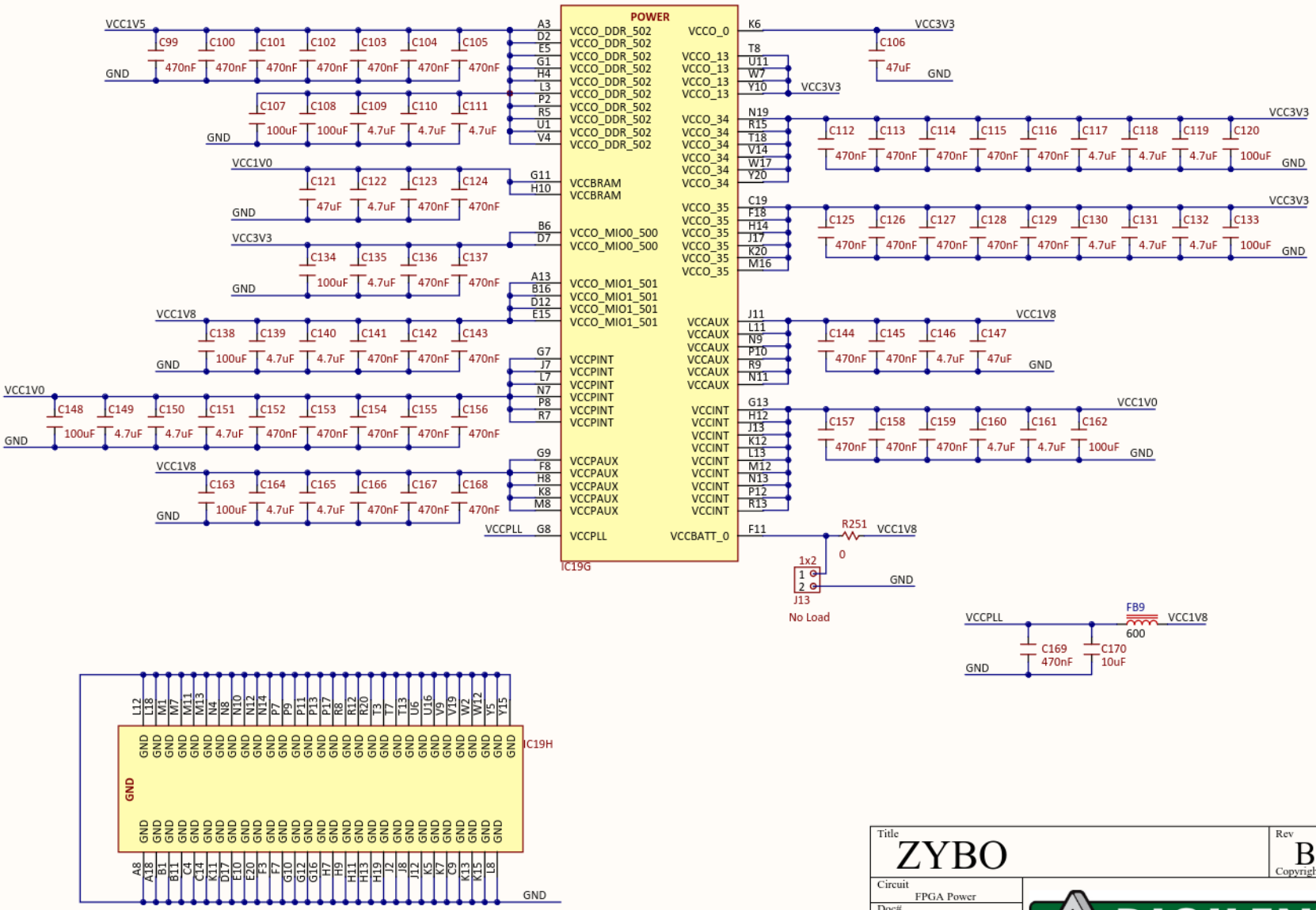
DIGILENT BEYOND THEORY


DDR3_VREF
C90
100nF
GND
VCC1V5
DDR PORT 502
IC19F
DDR3_A14 R206 10 1% F4
DDR3_A13 R208 10 1% D4
DDR3_A12 R214 10 1% E4
DDR3_A11 R205 10 1% G4
DDR3_A10 R207 10 1% F5
DDR3_A9 R213 10 1% J4
DDR3_A8 R216 10 1% K4
DDR3_A7 R212 10 1% K3
DDR3_A6 R211 10 1% L4
DDR3_A5 R217 10 1% L3
DDR3_A4 R200 10 1% M4
DDR3_A3 R203 10 1% K3
DDR3_A2 R210 10 1% M3
DDR3_A1 R215 10 1% K2
DDR3_A0 R219 10 1% N2
DDR3_BA2 R204 10 1% J5
DDR3_BA1 R197 10 1% R4
DDR3_BA0 R202 10 1% L5
DDR3_RESET
DDR3_RAS R198 10 1% P4
DDR3_CAS R196 10 1% P5
DDR3_CS R218 10 1% N1
DDR3_WE R201 10 1% M5
DDR3_CKE0 R209 10 1% N3
DDR3_CK_P
DDR3_CK_N
R225 80.6 1%
DDR3_ODT0 R199 10 1% N5
R230 80.6 1%
R229 80.6 1%
VCC3V3
Bank 500
IC19D
PS_POR_B_500
PS_CLK_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PG_ALL
PS_CLK
SPI_CS
SPI_DQ0/MODE0
SPI_DQ1/MODE1
SPI_DQ2/MODE2
SPI_DQ3/MODE3
SPI_SCK/MODE4
LD_MIO/VCFG0
SPI_SCLK_FB/VCFG1
JF8
JF2
JF3
JF4
JF1
JF9
JF10
R220 24
VCC1V8
Bank 501
IC19E
PS_SRST_B_501
PS_MIO_VREF_501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
PS_MIO30_501
PS_MIO31_501
PS_MIO32_501
PS_MIO33_501
PS_MIO34_501
PS_MIO35_501
PS_MIO36_501
PS_MIO37_501
PS_MIO38_501
PS_MIO39_501
PS_MIO40_501
PS_MIO41_501
PS_MIO42_501
PS_MIO43_501
PS_MIO44_501
PS_MIO45_501
PS_MIO46_501
PS_MIO47_501
PS_MIO48_501
PS_MIO49_501
PS_MIO50_501
PS_MIO51_501
PS_MIO52_501
PS_MIO53_501
PS_RST
VREF0V9
ETH_TXCK
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_RXCK
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
OTG_DATA4
OTG_DIR
OTG_STP
OTG_NXT
OTG_DATA0
OTG_DATA1
OTG_DATA2
OTG_DATA3
OTG_CLK
OTG_DATA5
OTG_DATA6
OTG_DATA7
SD_CCLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
OTG_RESETN
SD_CD
UART_RXD_OUT
UART_TXD_IN
PB0
PB1
ETH_MDC
ETH_MDIO
R226 40.2 1%
R221 10K 1%
R222 10K 1%
C91 10nF
R224 10K 1%
R223 10K 1%
C92 10nF
R227 20K
R228 20K
R238 20K
JP6 No Load
R240 1K
R241 20K
SPI_DQ0/MODE0
JP4 No Load
R231 1K
R233 20K
SPI_SCK/MODE4
R232 10K
BTN7
PTA-142 RED CAP
IC22 DSC1121CE5-50.0000
C93 100nF
R239 24 PS_CLK
R284 24 ETH_CLK
JTAG
QSPI
SD
1x4
JP5
R234 1K
R235 20K SPI_DQ3/MODE3
R236 20K SPI_DQ2/MODE2
R237 1K
Title
ZYBO
Rev
B.3
Copyright 2015
Circuit
DDR and MIO Banks
Doc# 500-279
Engineer EG
Author DL
Date 5/7/2015
Sheet# 9 out of 13
DIGILENT
BEYOND THEORY



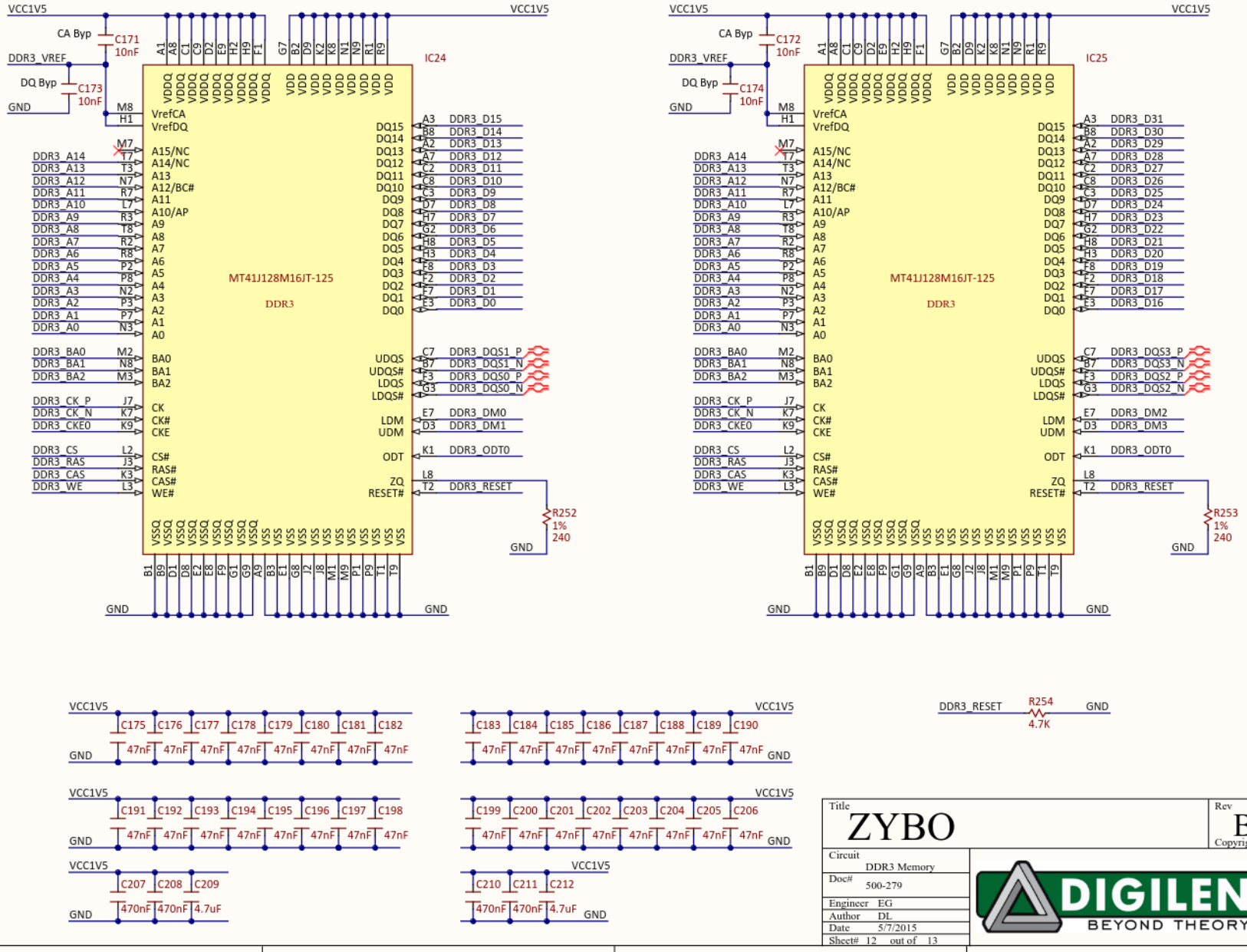
Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	FPGA Banks, Anti Alias Filters
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	10 out of 13

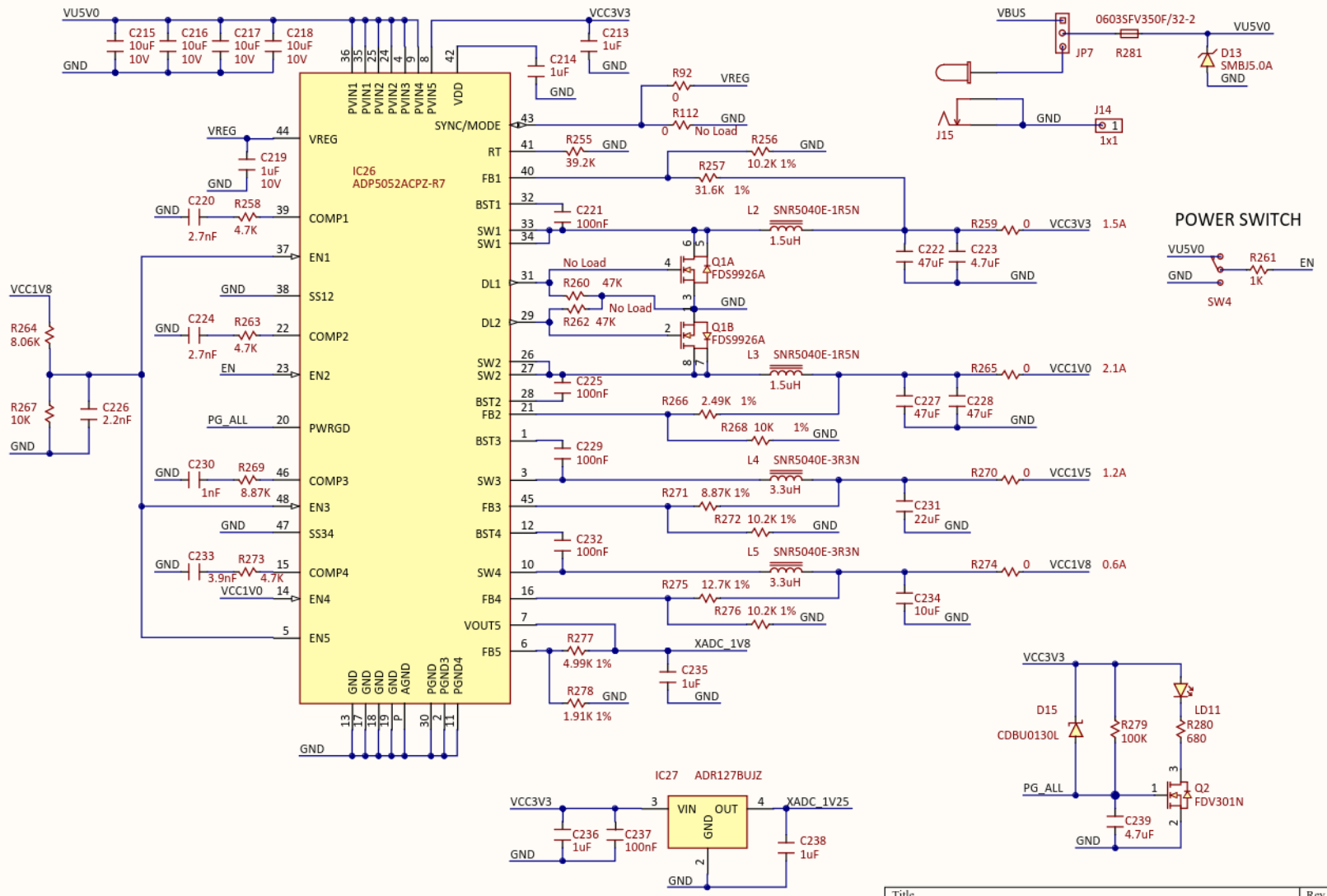
DIGILENT BEYOND THEORY



Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	FPGA Power
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	11 out of 13

DIGILENT BEYOND THEORY


VCC1V5
CA Byp
C171
10nF
DDR3_VREF
DQ Byp
C173
10nF
GND
IC24
MT41J128M16JT-125
DDR3
VrefCA
VrefDQ
A15/NC
A14/NC
A13
A12/BC#
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BA0
BA1
BA2
CK
CK#
CKE
CS#
RAS#
CAS#
WE#
UDQS
UDQS#
LDQS
LDQS#
LDM
UDM
ODT
ZQ
RESET#
DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
DDR3_A14
DDR3_A13
DDR3_A12
DDR3_A11
DDR3_A10
DDR3_A9
DDR3_A8
DDR3_A7
DDR3_A6
DDR3_A5
DDR3_A4
DDR3_A3
DDR3_A2
DDR3_A1
DDR3_A0
DDR3_BA0
DDR3_BA1
DDR3_BA2
DDR3_CK_P
DDR3_CK_N
DDR3_CKE0
DDR3_CS
DDR3_RAS
DDR3_CAS
DDR3_WE
DDR3_D15
DDR3_D14
DDR3_D13
DDR3_D12
DDR3_D11
DDR3_D10
DDR3_D9
DDR3_D8
DDR3_D7
DDR3_D6
DDR3_D5
DDR3_D4
DDR3_D3
DDR3_D2
DDR3_D1
DDR3_D0
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DM0
DDR3_DM1
DDR3_ODT0
DDR3_RESET
R252
1%
240
IC25
DDR3_D31
DDR3_D30
DDR3_D29
DDR3_D28
DDR3_D27
DDR3_D26
DDR3_D25
DDR3_D24
DDR3_D23
DDR3_D22
DDR3_D21
DDR3_D20
DDR3_D19
DDR3_D18
DDR3_D17
DDR3_D16
DDR3_DQS3_P
DDR3_DQS3_N
DDR3_DQS2_P
DDR3_DQS2_N
DDR3_DM2
DDR3_DM3
R253
C172
10nF
C174
10nF
C175 C176 C177 C178 C179 C180 C181 C182
C183 C184 C185 C186 C187 C188 C189 C190
C191 C192 C193 C194 C195 C196 C197 C198
C199 C200 C201 C202 C203 C204 C205 C206
C207 C208 C209
C210 C211 C212
47nF
470nF
4.7uF
DDR3_RESET
R254
4.7K
Title
ZYBO
Rev
B.3
Copyright 2015
Circuit
DDR3 Memory
Doc#
500-279
Engineer EG
Author DL
Date 5/7/2015
Sheet# 12 out of 13
DIGILENT
BEYOND THEORY



For more information on the parts used in this design, please refer to:

www.analog.com/adp5052 (5 - Channel Integrated Power Solution with Quad Buck Regulators and 200 mA LDO Regulator)

www.analog.com/adr127 (Precision, Micropower LDO 1.25 VOUT Voltage Reference)

Title	ZYBO
Rev	B.3
Copyright	2015
Circuit	Power Regulation
Doc#	500-279
Engineer	EG
Author	DL
Date	5/7/2015
Sheet#	13 out of 13

DIGILENT BEYOND THEORY