



## DESCRIPTION

The MP2975 is a dual-loop, digital, multi-phase controller that provides power for the CPU core of VR13.HC platforms and CPU cores based on AVSBus protocol. The device works with MPS and multiple vendors' DrMOS products to provide a total, multi-phase VR solution with a minimal number of external components. It provides 8 pulse-width modulations (PWMs), and can be configured up to 8-phase operation for rail 1 and up to 4-phase operation for rail 2.

The device provides on-chip non-volatile memory (NVM) to store and restore device configurations. Device configurations and fault parameters are easy to configure and monitor via the PMBus/I<sup>2</sup>C interface. The MP2975 monitors and reports the output current through the CS output from DrMOS products.

The MP2975 is based on a unique, digital, multi-phase nonlinear control to provide fast transient response to load transient with a minimum number of output capacitors. With only one power loop control method for both steady state and load transient, the power loop compensation is simple to configure.

The MP2975 is available in a QFN-40 (5mmx5mm) package.

## FEATURES

- Multi-Phase, Dual-Output Digital Controller
- Intel VR13.HC Compliant with PSYS Function
- Backward VR13/VR12.5 Compatible
- PMBus/I<sup>2</sup>C and AVSBus Compliant
- Selectable High Speed Bus: SVID, AVSBus, or PVID
- Switching Frequency Up to 3MHz
- Compatible with DrMOS by Multiple Vendors
- Built-In NVM to Store Custom Configurations
- Pin-Strap Multi-Configuration
- Automatic Loop Compensation
- Minimal External Components
- Overshoot Reduction with Nonlinear Control
- Flexible Phase Assignment for Dual Rails
- Auto Phase-Shedding and IVID Function to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Configurable Offsets for Thermal Balance
- Digital Load-Line Regulation
- DrMOS Fault Detection and Fault Auto-Record to NVM
- Supports Overclocking Mode
- Floating Line Detection
- Standby Mode to Save Power
- Input and Output Voltage, Current and Power, Regulator Temperature Monitoring
- UVLO/OVP/UVP/OCP/UCP/OTP/RVP Protections with Options of No Action, Latch, Retry, or Hiccup
- Enhanced Register Map with Read/Write Protection for Improved Security
- Available in a QFN-40 (5mmx5mm) Package

## APPLICATIONS

- Server Core Voltage
- DDRs
- Telecom and Networking Systems
- Base Stations

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## TYPICAL APPLICATION

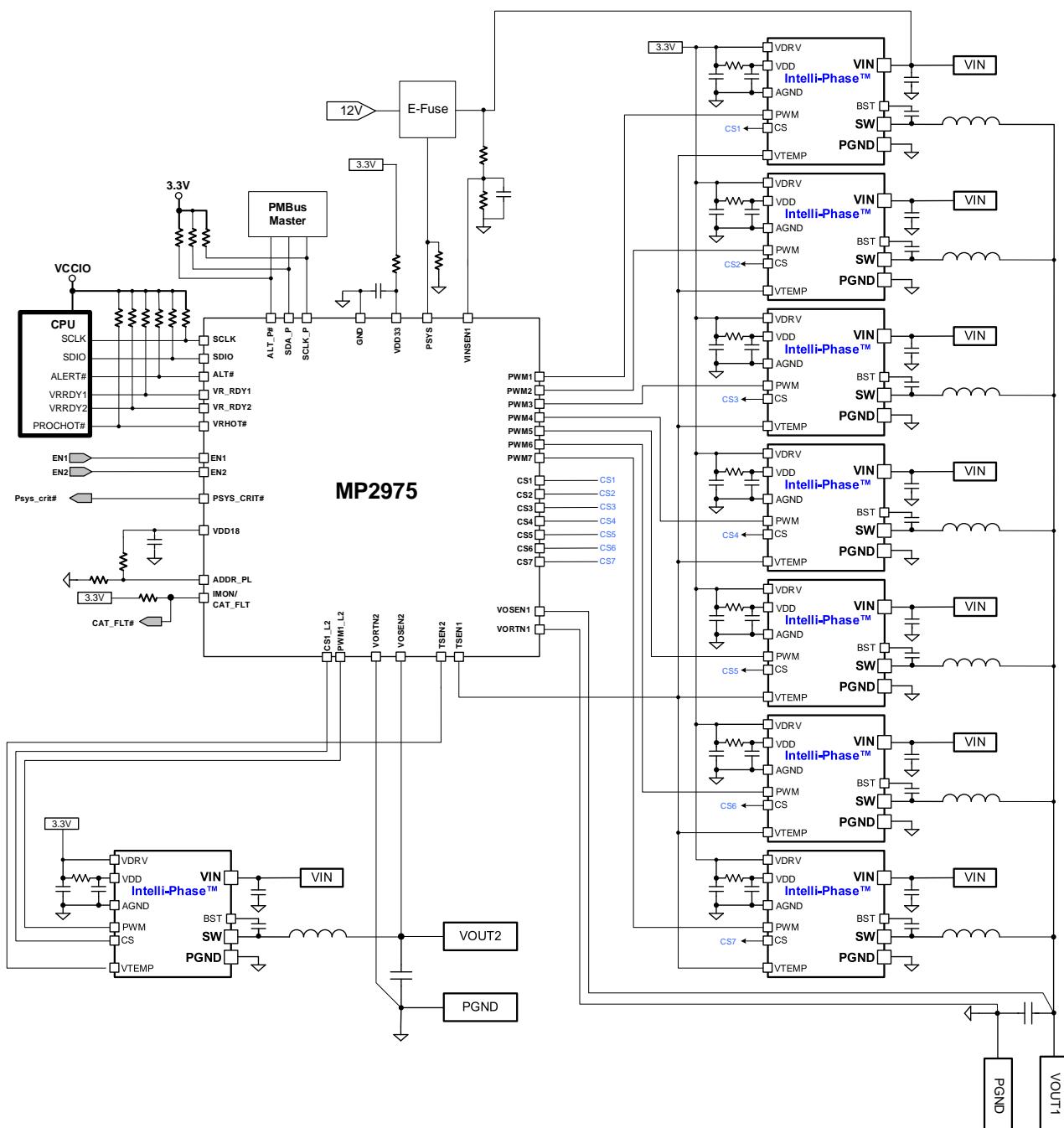


Figure 1: Intel SVID 7+1 Application

## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2975GU-xxxx**	QFN-40 (5mmx5mm)	See Below	3

\* For Tape & Reel, add suffix -Z (e.g. MP2975GU-xxxx-Z).

\*\* "xxxx" is the configuration code identifier for the register settings stored in the NVM. Each "x" is a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number.

## TOP MARKING

**MPSYYWW**  
**MP2975**  
**LLLLLLL**

MPS: MPS prefix

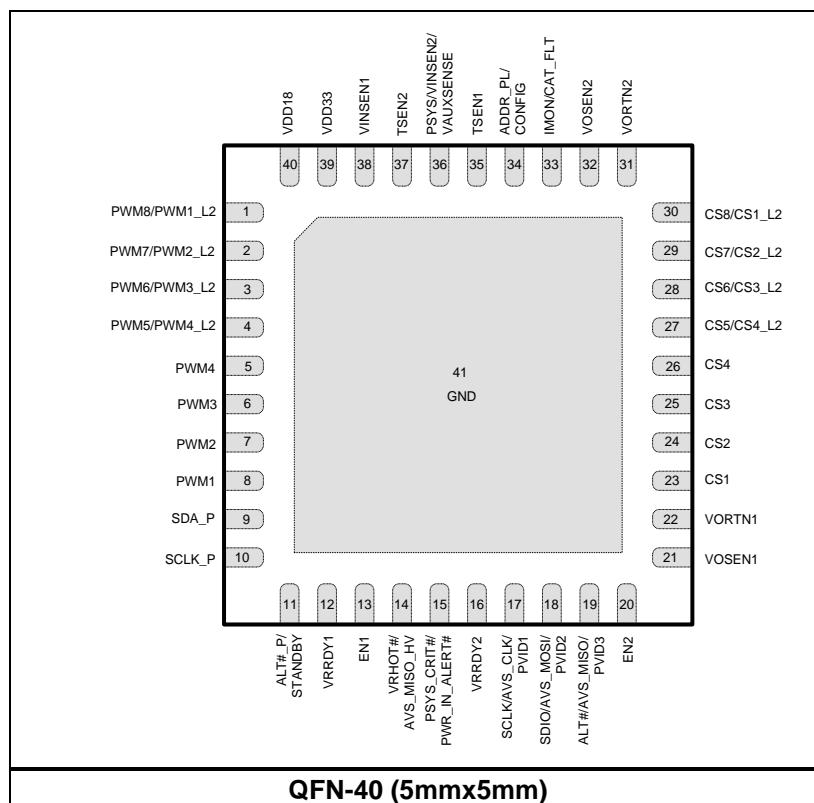
YY: Year code

WW: Week code

MP2975: Part number

LLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	I/O	Description
1	PWM8, PWM1_L2	D [O]	<b>PWM for phase 8 of rail 1, or phase 1 of rail 2.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
2	PWM7, PWM2_L2	D [O]	<b>PWM for phase 7 of rail 1, or phase 2 of rail 2.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
3	PWM6, PWM3_L2	D [O]	<b>PWM for phase 6 of rail 1, or phase 3 of rail 2.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
4	PWM5, PWM4_L2	D [O]	<b>PWM for phase 5 of rail 1, or phase 4 of rail 2.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
5	PWM4	D [O]	<b>PWM for phase 4 of rail 1.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
6	PWM3	D [O]	<b>PWM for phase 3 of rail 1.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
7	PWM2	D [O]	<b>PWM for phase 2 of rail 1.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
8	PWM1	D [O]	<b>PWM for phase 1 of rail 1.</b> The pin is a tri-state, logic-level PWM output, and is connected to the input of the DrMOS PWM pin. Float the pin if the phase is not being used.
9	SDA_P	D [I/O]	<b>PMBus data signal.</b>
10	SCLK_P	D [I]	<b>PMBus synchronous clock from the PMBus host.</b>
11	ALT_P#, STANDBY	D [I/O]	<b>PMBus alert# function.</b> These are open-drain outputs that offer DrMOS standby functionality.
12	VRRDY1	D [O]	<b>VR ready indicator signal for rail 1.</b> VRDDY1 is an open-drain output that stays low until soft start finishes and the output voltage reaches a standard value. This pin has 2-bit NVM configuration. It can be configured as the enable control for rail 2.
13	EN1	D [I]	<b>Active-high enable control for rail 1.</b> With 2-bit NVM configuration, this pin can be configured as an enable control for rail 2 or an enable control for both rail 1 and rail 2. For detailed sequencing, see the Operation section on page 17.
14	VRHOT#, AVS_MISO_ HV	D [O]	<b>Voltage regulator thermal indicator.</b> This pin is an open-drain output that asserts low if the sensed temperature exceeds the programmed over-temperature warning threshold. Or it is the AVSBus data signal when the bus voltage is between 1.8V and 3.3V.
15	PSYS_CRIT#, PWR_IN_ ALERT#	D [O]	<b>System input power exceed threshold alert signal.</b> PSYS_CRIT# is an open-drain output that asserts low when the PSYS voltage is at or above the configured threshold. Or it is the input power alert signal for VR13HC/VR13 protocol. PWR_IN_ALERT# is an open-drain output that asserts low when the input power exceeds the configured input power alert threshold.
16	VRRDY2	D [O]	<b>VR ready indicator signal of rail 2.</b> This pin is an open-drain output that remains low until the soft start finishes and the output voltage reaches a standard value. With 2-bit NVM configuration, it also can be configured as the enable control of rail 1.

**PIN FUNCTIONS (continued)**

Pin #	Name	I/O	Description
17	SCLK, AVS_CLK, PVID1	D [I]	<b>Multi-function pin.</b> Clock for SVID interface, AVSBus, or PVID1 input. Selectable with NVM configuration.
18	SDIO, AVS_MOSI, PVID2	D [I/O]	<b>Multi-function pin.</b> Data line for SVID interface, or master-to-slave data line for AVSBus, or PVID2 input. Selectable with NVM configuration.
19	ALT#, AVS_MISO, PVID3	D [O]	<b>Multi-function pin.</b> Alert# line for SVID interface, or slave-to-master data line for AVSBus with bus voltage up to 1.8V, or PVID3 input. Selectable with NVM configuration.
20	EN2	D[I]	<b>Enable control for rail 2.</b> Short to GND if rail 2 is unused.
21	VOSEN1	A[I]	<b>Positive remote-voltage sense input for rail 1.</b> This pin should be routed differentially with VORTN1.
22	VORTN1	A[I]	<b>Remote-voltage sense return input for rail 1.</b> This pin should be routed differentially with VOSEN1.
23	CS1	A[I]	<b>Current-sense input from phase 1 for rail 1.</b> Float CS1 if the phase is not used.
24	CS2	A[I]	<b>Current-sense input from phase 2 for rail 1.</b> Float CS2 if the phase is not used.
25	CS3	A[I]	<b>Current-sense input from phase 3 for rail 1.</b> Float CS3 if the phase is not used.
26	CS4	A[I]	<b>Current-sense input from phase 4 for rail 1.</b> Float CS4 if the phase is not used.
27	CS5, CS4_L2	A[I]	<b>Current-sense input from phase 5 for rail 1, or phase 4 for rail 2.</b> Float this pin if the phase is not used.
28	CS6, CS3_L2	A[I]	<b>Current-sense input from phase 6 for rail 1, or phase 3 for rail 2.</b> Float this pin if the phase is not used.
29	CS7, CS2_L2	A[I]	<b>Current-sense input from phase 7 for rail 1, or phase 2 for rail 2.</b> Float this pin if the phase is not used.
30	CS8, CS1_L2	A[I]	<b>Current-sense input from phase 8 for rail 1, or phase 1 for rail 2.</b> Float this pin if the phase is not used.
31	VORTN2	A[I]	<b>Remote-voltage sense return input for rail 2.</b> This pin should be routed differentially with VOSEN2.
32	VOSEN2	A[I]	<b>Positive remote-voltage sense input for rail 2.</b> This pin should be routed differentially with VORTN2.
33	IMON, CAT_FLT	D/A [O]	<b>Analog total load current signal for rail 1 or rail 2.</b> This pin is an open-drain output that can function as a voltage regulator fault indicator.
34	ADDR_PL, CONFIG	A[I]	<b>PMBus address bit[3:0] selection pin.</b> This pin allows the user to select six distinct configurations for the device.
35	TSEN1	A[I]	<b>Temperature sensing input 1.</b> TSEN1 reports the VR temperature, VR temperature warning, and over-temperature protection (OTP).
36	PSYS, VINSEN2, VAUXSENSE	A[I]	<b>Multi-function pin.</b> This pin can be configured for one of the following functions: <ul style="list-style-type: none"><li>• <b>PSYS: System input current/power input signal.</b> Calculates input power and asserts PSYS_CRIT# / PWR_IN_ALERT#. Connect to an analog signal that is proportional to the system's input current.</li><li>• <b>VINSEN2: Input voltage sense for rail 2.</b> Connect to an external divider from the input voltage of rail 2 to GND. Determines rail 2's PWM on time, input voltage under-voltage lockout (UVLO), and over-voltage (OV) protections.</li><li>• <b>VAUXSENSE: Auxiliary voltage sense.</b> General-purpose analog voltage sensing input (e.g. input for PSYS digital and analog protections).</li></ul>

**PIN FUNCTIONS (continued)**

Pin #	Name	I/O	Description
37	TSEN2	A[I]	<b>Temperature sensing input 2.</b> TSEN2 can be configured for VR over-temperature protection, or for general-purpose analog voltage sensing.
38	VINSEN1	A[I]	<b>Input voltage sensing.</b> This pin is selectable for rail 1 only, or for both rails.
39	VDD33	Power	<b>3.3V power supply voltage input.</b> Connect a 1µF bypass capacitor between this pin and ground.
40	VDD18	Power	<b>1.8V LDO output for internal digital circuit.</b> Connect a 1µF bypass capacitor between this pin and ground.
41 (PAD)	GND	A	<b>Analog ground.</b>

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

VDD33.....	-0.3V to +4.0V
VDD18.....	-0.3V to +2.2V
VORTN1, VORTN2.....	-0.3V to +0.3V
CS1 to CS8, PWM1 to PWM8, VOSEN1, VOSEN2, VRRDY1, VRRDY2, TSEN1, TSEN2, VRHOT#/AVS_MISO_HV, SCLK_P, SDA_P, ALT_P#/STANDBY, IMON/CAT_FLT,EN1, EN2, PSYS_CRIT#/PWR_IN_ALERT# .....	-0.3V to +4V
.....	-0.3V to +2.2V
SCLK/AVS_CLK/PVID1, SDIO/AVS_MOSI /PVID2, ALT#/AVS_MISO/PVID3, ADDR_PL /CONFIG, PSYS/VINSENSE2/VAUXSENSE, VINSEN1.....	150°C
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup> .....	3.4W
Junction temperature.....	150°C
Lead temperature .....	260°C
Storage temperature.....	-65°C to +150°C

**ESD Rating**

Human body model (HBM) .....	2kV
Charged device model (CDM).....	2kV

**Recommended Operating Conditions <sup>(3)</sup>**

VDD33.....	3.15V to 3.4V
Operating junction temp ( $T_J$ ) ....	-40°C to +125°C

**Thermal Resistance <sup>(4)</sup>       $\theta_{JA}$        $\theta_{JC}$** 

QFN-40 (5mmx5mm) .....	36.....5.....	°C/W
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**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 6-layer PCB.

## ELECTRICAL CHARACTERISTICS

VDD33 = 3.3 V, EN1/2 = 1V, current going into pin is positive. Typical values are at  $T_A = 25^\circ\text{C}$ , min/max values are at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Remote-Sense Amplifier</b>						
Bandwidth <sup>(5)</sup>	$\text{GBW}_{(\text{RSA})}$			20		MHz
VORTN1/2 current	$I_{\text{RTN}1/2}$	$\text{EN1/2} = 1\text{V}$ , $V_{\text{OSEN}1/2} = 3\text{V}$ , $V_{\text{ORTN}1/2} = 0\text{V}$	-60	-40		$\mu\text{A}$
VOSEN1/2 current	$I_{\text{OSEN}1/2}$	$\text{EN1/2} = 1\text{V}$ , $V_{\text{ORTN}1/2} = 0\text{V}$ , $V_{\text{OSEN}1/2} = 3\text{V}$		40	60	$\mu\text{A}$
<b>Oscillator</b>						
Frequency	$f_{\text{OSC}}$	$I_{\text{REF}} = 20\mu\text{A}$		1.56		MHz
<b>EN1, EN2</b>						
Input low voltage	$V_{\text{IL}(\text{EN})}$	EN is falling			0.4	V
Input high voltage	$V_{\text{IH}(\text{EN})}$	EN is rising	0.8			V
Enable high leakage	$I_{\text{IH}(\text{EN})}$	$\text{EN} = 3.3\text{V}$		3.3		$\mu\text{A}$
Enable delay (regular-power mode)	$t_{\text{DLY\_RP}}$	TON_DELAY set to 0, EN high to VRRDY assert, regular-power mode		15		$\mu\text{s}$
Enable delay (low-power mode)	$t_{\text{DLY\_LP}}$	TON_DELAY set to 0, EN high to VRRDY assert, low-power mode		1.5	2.5	ms
<b>Thermal Throttling Control</b>						
VRHOT# low voltage	$V_{\text{OL}(\text{VRHOT}\#)}$	$I_{\text{VRHOT}\#} = 20\text{mA}$		0.2		V
VRHOT# high leakage current	$I_{\text{L}(\text{VRHOT}\#)}$	$V_{\text{VRHOT}\#} = 3.3\text{V}$	-3		+3	$\mu\text{A}$
<b>PSYS_CRIT#, PWR_IN_ALT# Output</b>						
PSYS_CRIT#/PWR_IN_ALT# low voltage	$V_{\text{OL}(\text{PSYS\_CRIT}\#)}$	$I_{\text{PSYS\_CRIT}\#} = 20\text{mA}$		0.2		V
PSYS_CRIT#/PWR_IN_ALT# high leakage current	$I_{\text{L}(\text{PSYS\_CRIT}\#)}$	$V_{\text{PSYS\_CRIT}\#} = 3.3\text{V}$	-3		+3	$\mu\text{A}$
<b>VRRDY Output</b>						
VRRDY low voltage	$V_{\text{OL}(\text{VRRDY})}$	$I_{\text{VRRDY}} = 20\text{mA}$		0.2		V
VRRDY high leakage current	$I_{\text{L}(\text{VRRDY})}$	$V_{\text{VRRDY}} = 3.3\text{V}$	-3		+3	$\mu\text{A}$
<b>CAT_FLT, IMON Output</b>						
CAT_FLT low voltage output	$V_{\text{OL}(\text{CAT\_FLT})}$	$I_{\text{CAT\_FLT(SINK)}} = 1\text{mA}$		0.2		V

**ELECTRICAL CHARACTERISTICS (continued)**

VDD33 = 3.3 V, EN1/2 = 1V, current going into pin is positive. Typical values are at  $T_A = 25^\circ\text{C}$ , min/max values are at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Standby</b>						
Low voltage	$\text{VOL}_{(\text{STANDBY})}$	$I_{\text{STANDBY}(\text{SINK})} = 4\text{mA}$		0.2		V
<b>IMON Rail 1/2</b>						
IMON ADC reading accuracy		Gain = 8/64, 3/64, 10kΩ, $T_A = 25^\circ\text{C}$	-1		+1	%
<b>Load Line Rail 1/2</b>						
$\text{V}_{\text{DROOP}}$		Gain = 75mV/mA, $I_{\text{CS}} = 2\text{mA}$ , $T_A = 25^\circ\text{C}$	146	150	154	mV
<b>PWM Set Signal Comparator</b>						
Propagation delay <sup>(5)</sup>	$t_{\text{PD}}$			10		ns
Common mode range <sup>(5)</sup>			0		1.6	V
<b>VFB- Window Comparator (Rail 1/2, VFB = VDAC - 25mV)</b>						
Propagation delay <sup>(5)</sup>	$t_{\text{PD}}$			10		ns
Common mode range <sup>(5)</sup>			0		1.6	V
Threshold voltage <sup>(5)</sup>	$V_{\text{TH}(\text{VFB}-)}$	Relative to reference DAC voltage		-25		mV
<b>VFB+ Window Comparator (Rail 1/2, VFB = VDAC + 20mV)</b>						
Propagation delay <sup>(5)</sup>	$t_{\text{PD}}$			10		ns
Common mode range <sup>(5)</sup>			0		1.6	V
Threshold voltage <sup>(5)</sup>	$V_{\text{TH}(\text{VFB}+)}$	Relative to Reference DAC voltage		20		mV
<b>Over-Voltage (OV) and Under-Voltage (UV) Protection Comparator (Rail 1/2)</b>						
Under-voltage threshold	UVP DAC	Relative to (VID-LL) or VID		-400		mV
		Resolution <sup>(5)</sup>		50		mV
Over-voltage threshold	OVP2	Relative to reference DAC voltage, OVUV_SEL = 1		140		mV
		Relative to reference DAC voltage, OVUV_SEL = 2		220		mV
		Relative to reference DAC voltage, OVUV_SEL = 3		400		mV
	OVP1 DAC	Full scale range		2.53		
		Resolution <sup>(5)</sup>		10		mV
RVP threshold <sup>(5)</sup>	$\text{V}_{\text{RVP\_TH}(\text{RV})}$	Remote-sense amplifier unit gain		160		mV
		Remote-sense amplifier half-gain		80		mV

## ELECTRICAL CHARACTERISTICS (continued)

VDD33 = 3.3 V, EN1/2 = 1V, current going into pin is positive. Typical values are at  $T_A = 25^\circ\text{C}$ , min/max values are at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>CS Fault Comparator (Rail 1/2, CS Fault Protection)</b>						
CS fault threshold	$V_{CS\_TH}$			200		mV
<b>PWM Outputs</b>						
Output low voltage	$V_{OL\text{(PWM)}}$	$I_{PWM\text{(SINK)}} = 400\mu\text{A}$		10	200	mV
Output middle voltage	$V_{OM\text{(PWM)}}$	$I_{PWM\text{(SOURCE)}} = -100\mu\text{A}$		1.5		V
Output high voltage	$V_{OH\text{(PWM)}}$	$I_{PWM\text{(SOURCE)}} = -400\mu\text{A}$	3.15	VDD33 - 0.02		V
Rise and fall time <sup>(5)</sup>		$C = 10\text{pF}$		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	$\mu\text{A}$
Minimum on time <sup>(5)</sup>	$t_{ON\_MIN}$	Register configurable, (74h [8:6] = 3)		30		ns
Minimum off time <sup>(5)</sup>	$t_{OFF\_MIN}$	Register configurable, (74h [14:9] = 3)		30		ns
Minimum time for middle voltage <sup>(5)</sup>		Register configurable, (74h [5:0] = 10)		100		ns
PWM fault detection source current	$I_{SOURCE\text{(PWM)}}$			130		$\mu\text{A}$
<b>VDD33 Supply</b>						
Supply current	$I_{VDD33}$	EN1/2 = high, 7 + 1-phase configuration		40	55	mA
		EN1/2 = 0V, low-power mode enable		150		$\mu\text{A}$
UVLO threshold voltage	VDD33UVLO	VDD33 is rising		2.85	3.05	V
		VDD33 is falling	2.55	2.75		V
<b>VDD18 Regulator</b>						
1.8V regulator output voltage	VDD18	$I_{VDD18} = 0\text{mA}$	1.75	1.8	1.85	V
1.8V regulator load capability	$I_{VDD18}$	$V_{OL} = VDD18 - 40\text{mV}$		30		mA

**ELECTRICAL CHARACTERISTICS (continued)**

VDD33 = 3.3 V, EN1/2 = 1V, current going into pin is positive. Typical values are at  $T_A = 25^\circ\text{C}$ , min/max values are at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>SVID/AVSBus Interface, PVID Pins</b>						
Interface voltage (SDIO, SCLK) (AVS_MOSI, AVS_CLK) <sup>(5)</sup>	V <sub>IL</sub>	Logic low			0.45	V
	V <sub>IH</sub>	Logic high	0.65			V
	V <sub>HYST</sub>	Hysteresis	50			mV
Leakage current (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO)	I <sub>L</sub>	0V to 1.8V	-10		+10	µA
Pin capacitance <sup>(5)</sup> (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO)	C <sub>PIN</sub>				5	pF
Pin capacitance <sup>(5)</sup> (AVS_MISO_HV)					10	pF
Buffer on resistance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO)	R <sub>ON</sub>			8		Ω
Buffer on resistance (AVS_MISO_HV)				8		Ω
Clock-to-data delay <sup>(5)</sup>			4		8.3	ns
Set-up time <sup>(5)</sup>				7		ns
Hold time <sup>(5)</sup>				14		ns
<b>ADC <sup>(5)</sup></b>						
Voltage range			0		1.6	V
ADC resolution				10		bits
DNL					1	LSB
Sample Rate				780		kHz
<b>VID DAC (Reference Voltage for Rail 1/2) <sup>(5)</sup></b>						
Voltage range	FSVID DAC	5mV/LSB mode, remote-sense amplifier unit gain	0.25		1.6	V
		5mV/LSB mode, remote-sense amplifier half-gain	0.25		2.8	V
		10mV/LSB mode, remote-sense amplifier unit gain	0.2		1.6	V
		10mV/LSB mode, remote-sense amplifier half-gain	0.2		3.2	V
Resolution	ΔVID DAC	5mV/LSB mode		5		mV
		10mV/LSB mode		10		mV
Output voltage slew rate <sup>(5)</sup>				100		mV/µs
<b>OCL-Phase DAC</b>						
Voltage range	FSOC DAC		1.28		2.53	V
Resolution <sup>(5)</sup>	ΔOC DAC			5		mV

**ELECTRICAL CHARACTERISTICS (continued)**

VDD33 = 3.3 V, EN1/2 = 1V, Current going into pin is positive. Typical values are at  $T_A = 25^\circ\text{C}$ , Min/Max values are at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>NCP-Phase DAC</b>						
Voltage range	$\text{FS}_{\text{UC DAC}}$		0.52		1.8	V
Resolution <sup>(5)</sup>	$\Delta_{\text{UC DAC}}$			5		mV
<b>PSYS DAC</b>						
Voltage range	$\text{FS}_{\text{DAC}}$			1.6		V
Resolution <sup>(5)</sup>	$\Delta_{\text{DAC}}$			6.25		mV
<b>TSNS1 Faut</b>						
TSNS1 fault threshold			2	2.2	2.4	V
<b>TSNS2 DAC</b>						
Voltage range	$\text{FS}_{\text{DAC}}$			2.4		V
Resolution <sup>(5)</sup>	$\Delta_{\text{DAC}}$			50		mV
<b>PMBus DC Characteristics (ALT_P, SDA_P, SCL_P)</b>						
Input high voltage	$\text{V}_{\text{IH}}$	SCL_P, SDA_P	2.1			V
Input low voltage	$\text{V}_{\text{IL}}$	SCL_P, SDA_P			0.7	V
Input leakage current		SCL_P, SDA_P, ALT_P	-10		+10	$\mu\text{A}$
Output low voltage	$\text{V}_{\text{OL}}$	ALT_P sinks 2mA			400	mV
Pin capacitance <sup>(5)</sup>	$C_{\text{PIN}}$				10	pF
<b>PMBus Timing Characteristics <sup>(5) (6)</sup></b>						
Operating frequency range	$f_{\text{PMB}}$		10		1000	kHz
Bus free time	$t_{\text{BUF}}$	Between stop and start condition	0.5			$\mu\text{s}$
Hold time after (repeated) start condition	$t_{\text{HD_STA}}$	After this period, the first clock is generated	0.26			$\mu\text{s}$
Repeated start condition set-up time	$t_{\text{SU_STA}}$		0.26			$\mu\text{s}$
Stop condition set-up time	$t_{\text{SU_STO}}$		0.26			$\mu\text{s}$
Data hold time	$t_{\text{HD_DAT}}$		0			ns
Data set-up time	$t_{\text{SU_DAT}}$		50			ns
Clock low timeout	$t_{\text{TIMEOUT}}$		25		35	ms
Clock low period	$t_{\text{LOW}}$		0.5			$\mu\text{s}$
Clock high period	$t_{\text{HIGH}}$		0.26		50	$\mu\text{s}$
Clock/data fall time	$t_F$				120	ns
Clock/data rise time	$t_R$				120	ns

**Notes:**

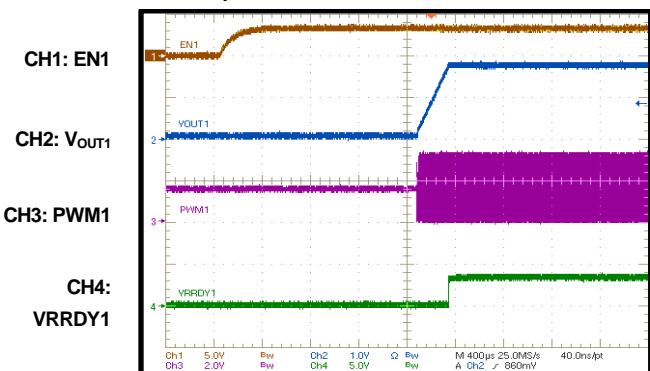
- 5) Guaranteed by design or characterization data. Not tested in production.

## TYPICAL PERFORMANCE CHARACTERISTICS

Rail 1: 7-phase,  $V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{SW1} = 1.2MHz$ ,  $L_1 = 70nH$ ,  $C_{OUT1} = 44 \times 47\mu F + 59 \times 22\mu F$ .  
Rail 2: 1-phase,  $V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ ,  $f_{SW2} = 800kHz$ ,  $L_2 = 180nH$ ,  $C_{OUT2} = 3 \times 47\mu F + 5 \times 22\mu F + 1 \times 470\mu F$ .  $T_A = 25^\circ C$ , unless otherwise noted.

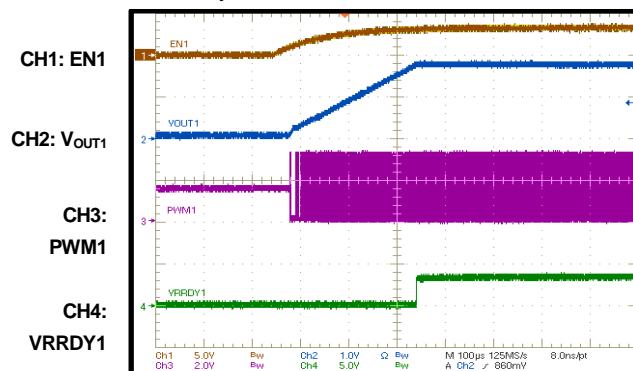
### Rail 1 Enable On

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.7V$ , low-power mode,  
 $t_{ON}$  delay = 0



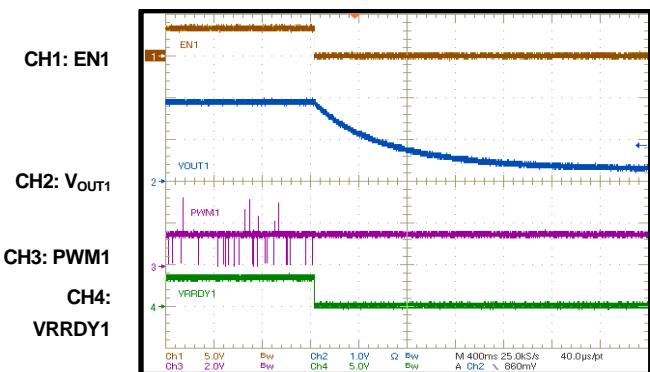
### Rail 1 Enable On

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.7V$ , regular-power mode,  
 $t_{ON}$  delay = 0



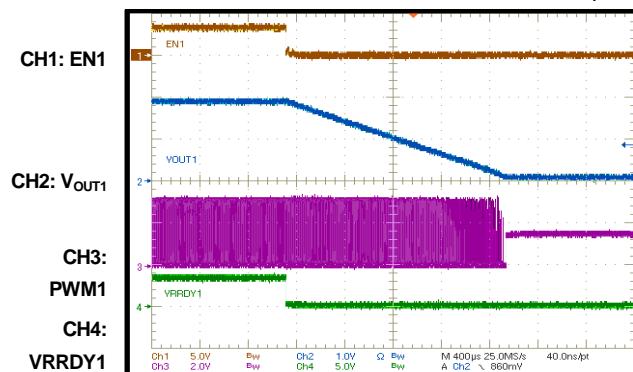
### Rail 1 Enable Off

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , Hi-Z off



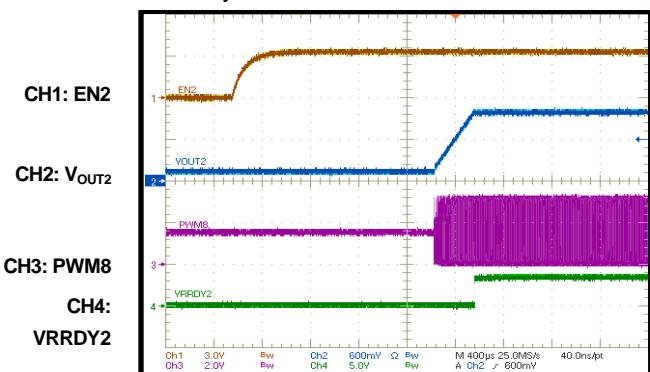
### Rail 1 Enable Off

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , soft off with  $1mV/\mu s$



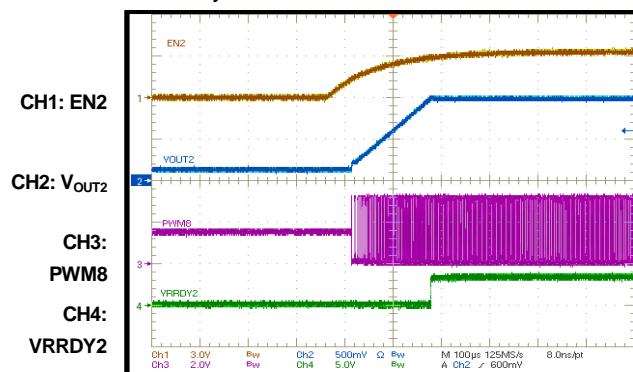
### Rail 2 Enable On

$V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ , low-power mode,  
 $t_{ON}$  delay = 0



### Rail 2 Enable On

$V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ , regular-power mode,  
 $t_{ON}$  delay = 0

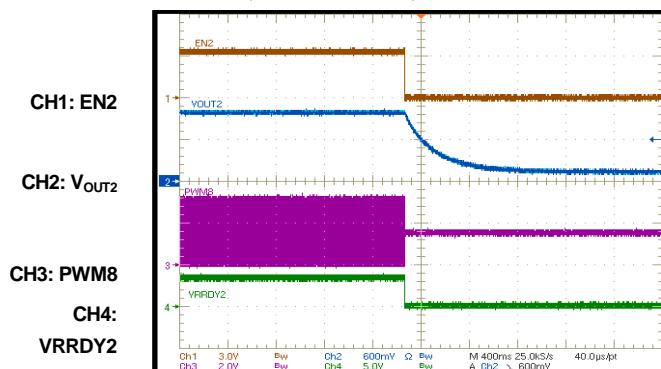


## TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

Rail 1: 6-phase,  $V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{SW1} = 800\text{kHz}$ ,  $L_1 = 100\text{nH}$ ,  $C_{OUT1} = 44 \times 47\mu\text{F} + 59 \times 22\mu\text{F}$ .  
Rail 2: 1-phase,  $V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ ,  $f_{SW2} = 800\text{kHz}$ ,  $L_2 = 180\text{nH}$ ,  $C_{OUT2} = 3 \times 47\mu\text{F} + 5 \times 22\mu\text{F} + 1 \times 470\mu\text{F}$ .  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

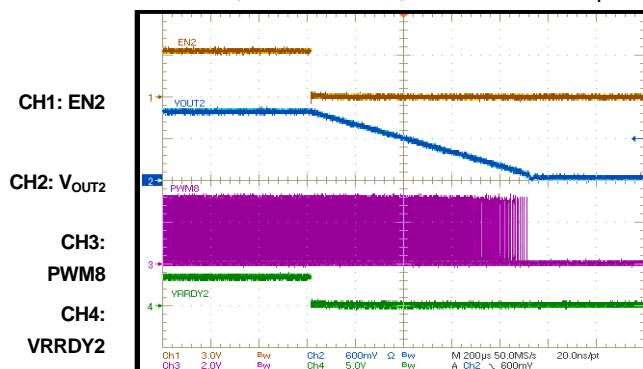
### Rail 2 Enable Off

$V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ , Hi-Z off



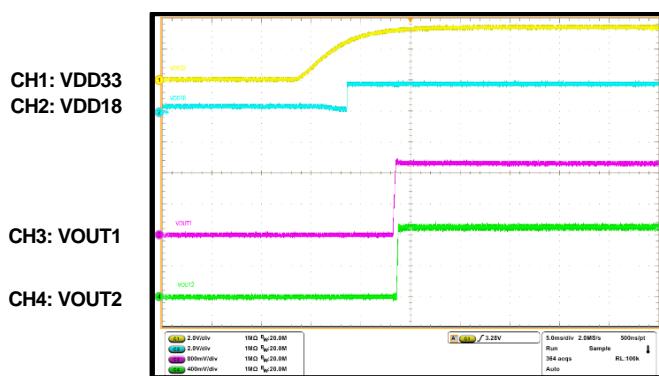
### Rail 2 Enable Off

$V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ , soft off with  $1\text{mV}/\mu\text{s}$



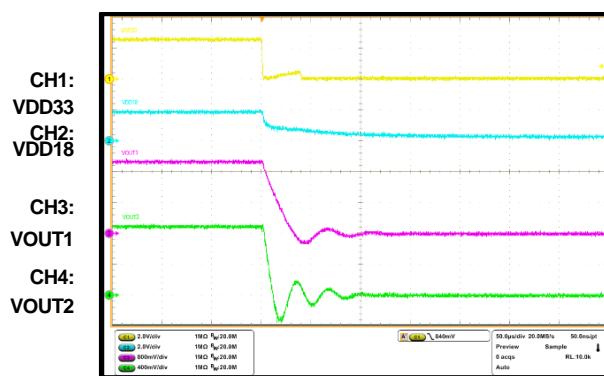
### VDD33 On

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.7V$ ,  $V_{OUT2} = 0.95V$ ,  
VDD33 = 3.3V



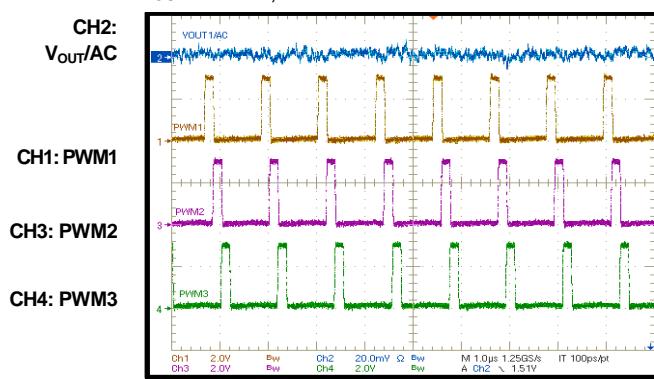
### VDD33 Off

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.7V$ ,  $V_{OUT2} = 0.95V$ ,  
VDD33 = 3.3V



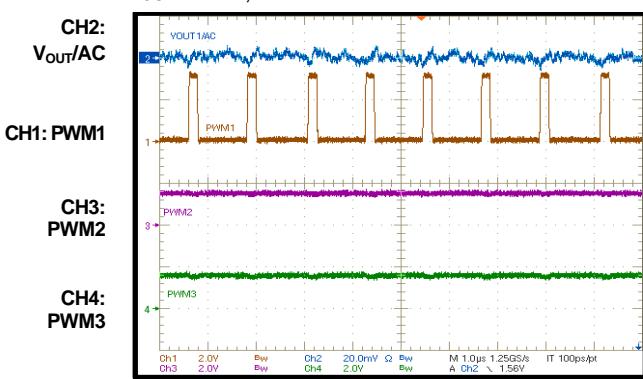
### Steady State

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , 6-phase CCM,  
 $I_{OUT} = 100A$ , PS0



### Steady State

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , 1-phase CCM,  
 $I_{OUT} = 15A$ , PS1

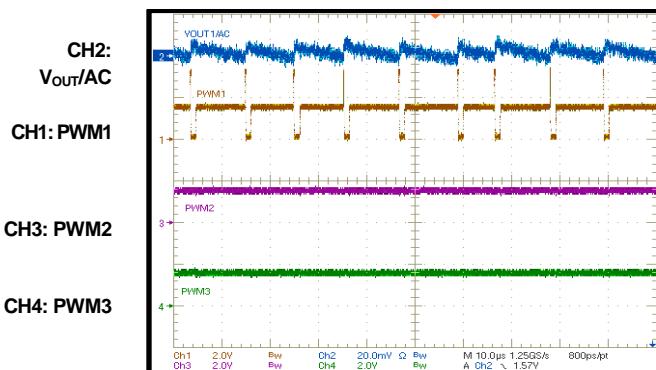


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Rail 1: 6-phase,  $V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{SW1} = 800kHz$ ,  $L_1 = 100nH$ ,  $C_{OUT1} = 44 \times 47\mu F + 59 \times 22\mu F$ .  
Rail 2: 1-phase,  $V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ ,  $f_{SW2} = 800kHz$ ,  $L_2 = 180nH$ ,  $C_{OUT2} = 3 \times 47\mu F + 5 \times 22\mu F + 1 \times 470\mu F$ .  $T_A = 25^\circ C$ , unless otherwise noted.

### Steady State

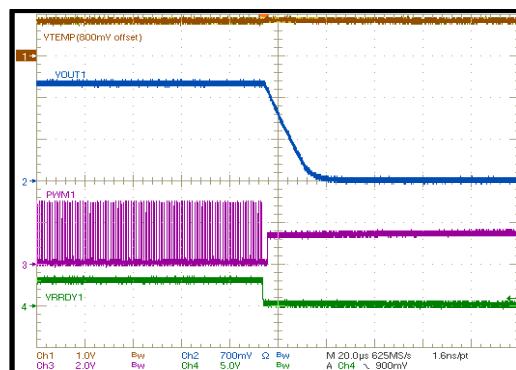
$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$   
1-phase CCM,  $I_{OUT} = 1A$ , PS2



### Over-Temperature Protection (OTP)

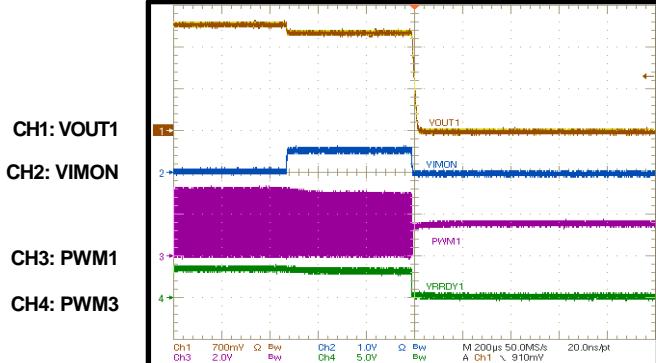
$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , latch-off mode,  
 $T_J = (125^\circ C/V) \times V_{TEMP} - 75^\circ C$   
OTP threshold = 130°C

CH1: PWM1  
CH2: V<sub>OUT</sub>/AC  
CH3: PWM2  
CH4: PWM3



### Over-Current Protection (OCP)

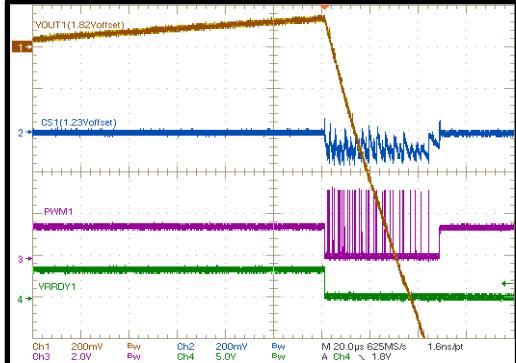
$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , OCP\_Total = 240A,  
OCP action delay = 0.5ms, latch-off mode



### Over-Voltage Protection (OVP)

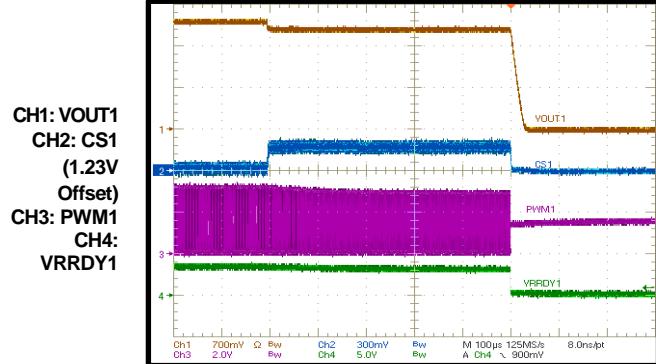
$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{sw} = 800kHz$ ,  
OVP blanking time = 0.5μs

CH1: V<sub>OUT1</sub> (1.82V Offset)  
CH2: CS1 (1.23V offset)  
CH3: PWM1  
CH4: VRRDY1



### Under-Voltage Protection (UVP)

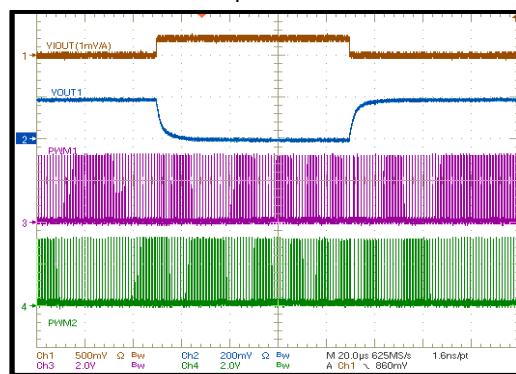
$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{sw} = 800kHz$ ,  
UVP blanking time = 400μs



### Load Transient with DC Load Line

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ , RLL\_DC = 0.9mΩ,  
28A to 228A at 776A/μs

CH1: V<sub>OUT</sub> (1mV/A)  
CH2: V<sub>OUT</sub> (1.6V Offset)  
CH3: PWM1  
CH4: PWM2

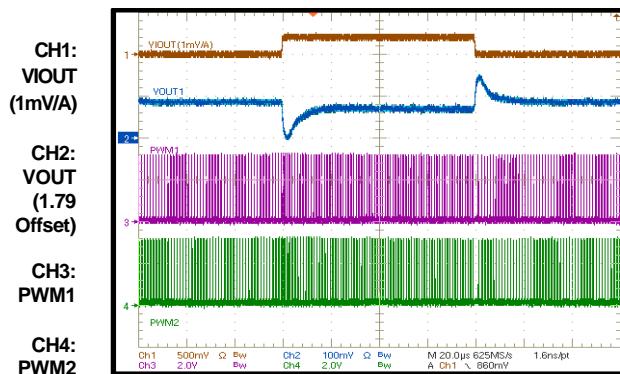


## TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

Rail 1: 6-phase,  $V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $f_{SW1} = 800\text{kHz}$ ,  $L_1 = 100\text{nH}$ ,  $C_{OUT1} = 44 \times 47\mu\text{F} + 59 \times 22\mu\text{F}$ .  
Rail 2: 1-phase,  $V_{IN} = 12V$ ,  $V_{OUT2} = 0.95V$ ,  $f_{SW2} = 800\text{kHz}$ ,  $L_2 = 180\text{nH}$ ,  $C_{OUT2} = 3 \times 47\mu\text{F} + 5 \times 22\mu\text{F} + 1 \times 470\mu\text{F}$ .  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

### Load Transient with AC Load Line

$V_{IN} = 12V$ ,  $V_{OUT1} = 1.82V$ ,  $RLL\_DC = 0\text{m}\Omega$ ,  
 $28A$  to  $228A$  at  $776\text{A}/\mu\text{s}$

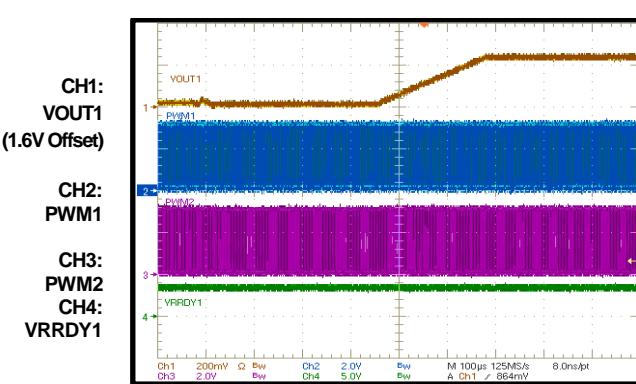


### DVID Up

DVID from  $1.6V$  to  $1.82V$ , SR =  $25\text{mV}/\mu\text{s}$

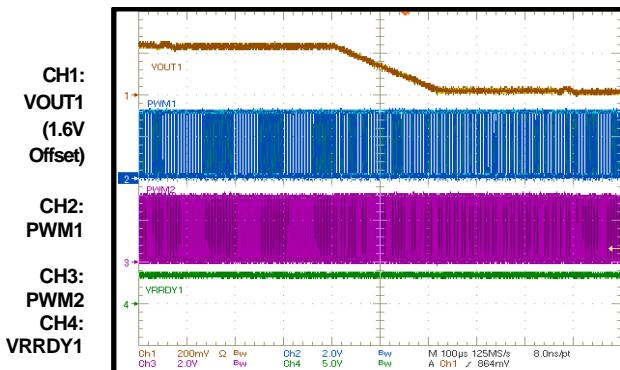
### DVID Up

DVID from  $1.6V$  to  $1.82V$ , SR =  $25\text{mV}/\mu\text{s}$



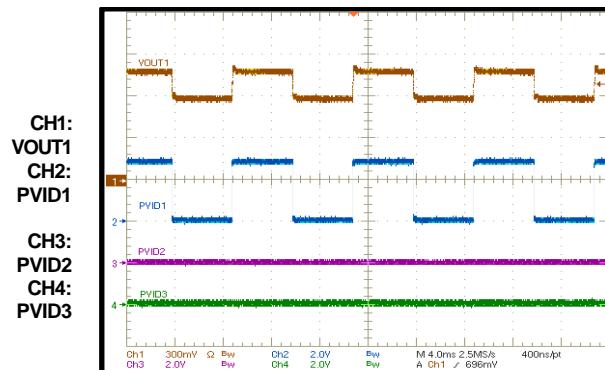
### DVID Down

DVID from  $1.82V$  to  $1.6V$ , SR =  $25\text{mV}/\mu\text{s}$



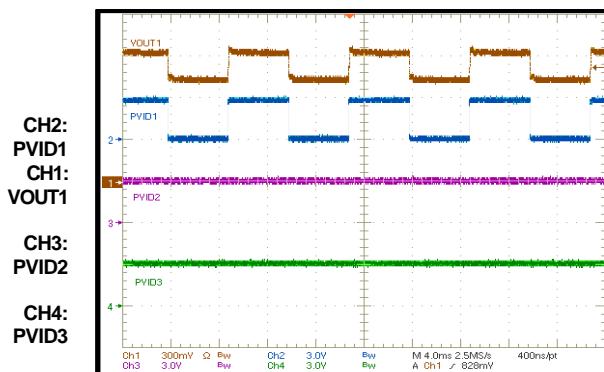
### PVID Transition

$V_{IN} = 12V$ , PVID0 = 0 to 1, PVID2 = PVID3 = 0, PVID\_000 = 0.6V, PVID\_100 = 0.8V



### PVID Transition

$V_{IN} = 12V$ , PVID0 = 0 to 1, PVID2 = PVID3 = 1, PVID\_011 = 0.75V, PVID\_111 = 0.95V



## FUNCTIONAL BLOCK DIAGRAM

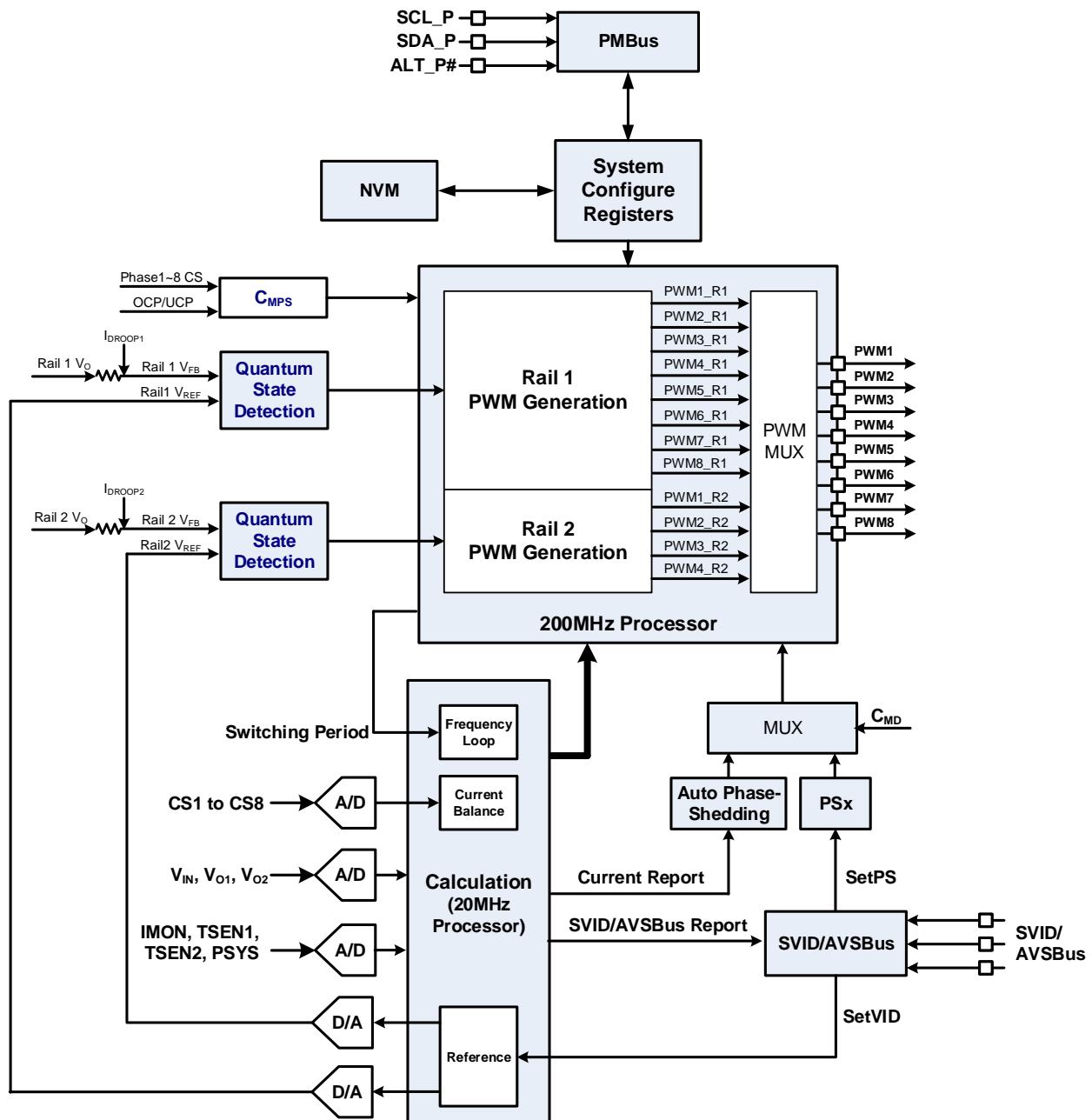


Figure 1: Functional Block Diagram

## OPERATION

The MP2975 is dual-output, digital, multi-phase controller for the Intel VR13.HC platform, and it is compatible with AVSBus communication protocol. It is also backward compatible with Intel VR13 and VR12.5 DC/DC converter specifications. The device adopts a unique loop compensation strategy to balance and optimize the steady and transient performance. It also uses adaptive phase-shedding and phase-adding strategies to optimize the overall VR efficiency according to the load current.

The device contains precise DAC and ADC, a differential remote voltage-sense amplifier, fast comparators, current-sense amplifiers, and internal slope compensation.

The MP2975 provides rich configurable functions via the PMBus 1.3 interface. On-chip, non-volatile memory (NVM) is available to store custom configurations and auto-record fault types when protections occur.

Configurable PMBus functions include phase assignment, switching frequency, reference voltage, loop stability parameters, protection thresholds and behaviors, and load-line parameters.

Fault protection features include  $V_{IN}$  under-voltage lockout (UVLO),  $V_{IN}$  over-voltage protection (OVP),  $V_{OUT}$  OVP,  $V_{OUT}$  under-voltage protection (UVP),  $V_{OUT}$  reverse-voltage protection (RVP), output over-current protection (OCP), under-current protection (UCP), over-temperature protection (OTP), remote-sensing line open detection, and DrMOS fault protection. The controller also has an on-chip thermal shutdown function to prevent the controller from overheating.

The MP2975 can automatically record the last fault into the NVM in case the power supply shuts off after the fault occurs. When working with an MPS Intelli-Phase™ device, the MP2975 can detect the fault type when the Intelli-Phase™ fault occurs.

Figure 2 shows the MP2975 system state machine.

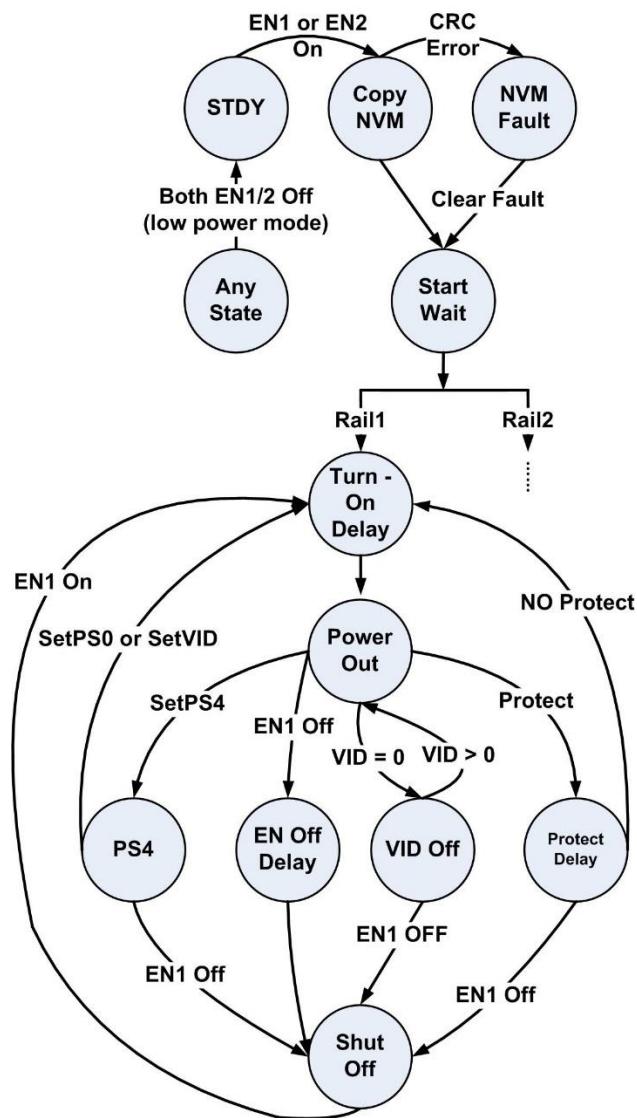


Figure 2: System State Machine

### PWM Control and Switching Frequency

The MP2975 applies MPS's unique digital PWM control to provide fast load transient response and easy loop compensation. The switching frequency can be set via PMBus command MFR\_FS (5Ch).

The PWM on time ( $t_{ON}$ ) of each phase updates adaptively in real-time according to the input voltage, output voltage, and the phase switching frequency.  $t_{ON}$  can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

Where  $V_{OUT}$  is the real-time output voltage (in V),  $V_{IN}$  is the input voltage (in V), and  $f_{SW}$  is the switching frequency set by PMBus (in Hz).

### Reference Voltage

The MP2975 has 9-bit VID DAC, which provides the reference voltage ( $V_{REF}$ ) for the individual output. When VID equals 0,  $V_{REF}$  is 0V while the VR is off. When VID exceeds 0, the relationship between  $V_{REF}$  and the VID value (in decimals) can be estimated with Equation (2):

$$V_{REF}(V) = \frac{(VID + OFFSET) \times VID\_STEP(mV)}{1000} \times G_{RS} \quad (2)$$

Where VID is the commanded voltage identification value from SVID, PMBus, AVSBus interface or PVID control, in decimals.

OFFSET is an offset value. OFFSET = 29 when the Intel IMVP9 10mV VID table is selected via registers 0Dh/1Dh on page 2 (for rail 1 and rail 2, respectively). For others, OFFSET = 49.

VID\_STEP is either 5mV or 10mV, determined by registers 0Dh/1Dh on page 2 (for rail 1 and rail 2, respectively).

$G_{RS}$  is the remote-sense amplifier gain. The value is 1 with a unit gain and 0.5 with half-gain, which is determined by bit[11] in register VOUT\_SENSE\_SET (29h).

In the MP2975, the VID is a 9-bit value, which is selected from the SVID interface, AVSBus interface, PMBus interface, or PVID control. The VID control starts with VID mode selection. Figure 3 shows the VID control related commands.

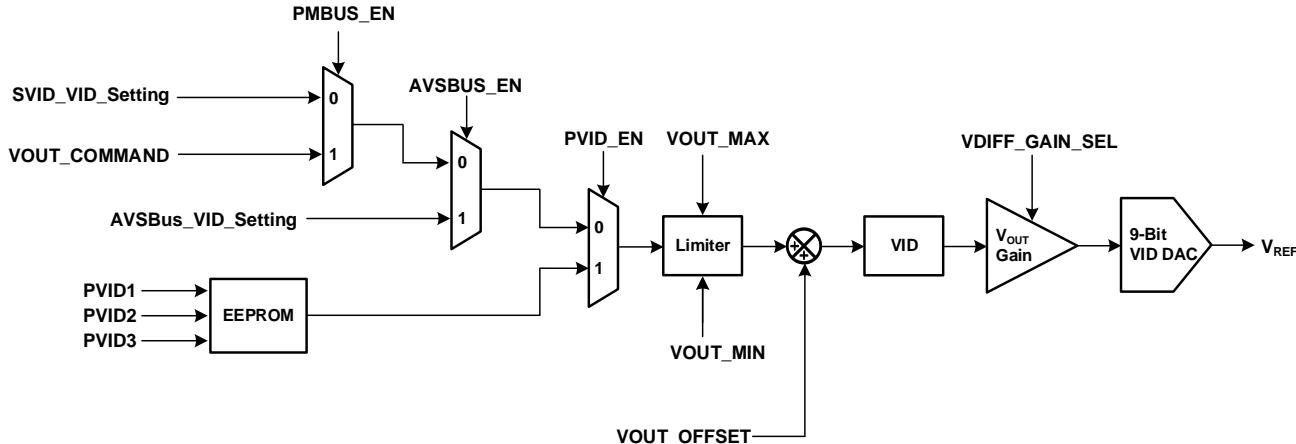


Figure 3: VID Control Related Commands

The register listed below shows the VID mode selection bits and related registers:

- **PMBUS\_EN:** MFR\_VR\_CONFIG2 (5Eh, bit[9])
- **PVID\_EN:** MFR\_VR\_CONFIG2 (5Eh, bit[11])
- **AVSBUS\_EN:** OPERATION (01h)

After the VID mode selection, the commanded voltage developed is compared with the output voltage limits set by the VOUT\_MAX (24h) and VOUT\_MIN (2Bh) commands. If the calculated voltage command creates an output voltage that exceeds the VOUT\_MAX value or is below the VOUT\_MIN value, the PMBus device limits the command voltage to VOUT\_MAX or VOUT\_MIN. Then the PMBus Alert# pin can be asserted as a warning to the master.

After VID limitation, the value from the VOUT\_OFFSET (1Eh on page 2) is added to the VID. The VOUT\_OFFSET register is in two's complement format with 1-VID step/LSB. It can range from -0.64V to +0.635V with the 5mV VID table, and -1.28V to +1.27V with the 10mV VID table.

VOUT\_OFFSET allows the user to adjust target VID to achieve overclocking. After setting VOUT\_OFFSET, the final VID is formed. A unit gain or half-gain calculates the final input value into VID DAC. VID DAC generates the final reference voltage, which is compared with the sensed output voltage to adjust the PWM duty cycle.

### Output Voltage Setting

Figure 4 shows how the voltage at the load is sensed with the differential voltage-sense amplifier. This type of sensing provides improved load regulation. The remote-sense amplifier can be configured with unit gain or half-gain via the PMBus command VOUT\_SENSE\_SET (29h).

The registers 07h/17h on page 2 can add voltage trimming values on rail 1 and rail 2, respectively, to fine-tune the output voltage. They are 0.5mV/LSB with unit gain remote sense, and 0.8mV/LSB with half-gain remote sense. This capability fine-tunes the output voltage, which can either add or subtract an offset from the remotesensed output voltage. This can adjust the output

voltage to improve V<sub>OUT</sub> accuracy for the end user's system.

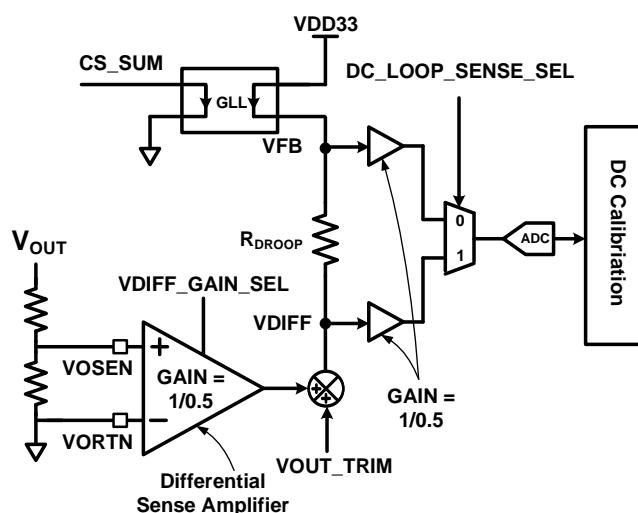
After voltage trim, the MP2975 senses the voltage either on VDIFF or VFB with ADC or DC voltage calibration, thus providing high-accuracy voltage regulation. The ADC sense also provides unit gain or half-gain to ensure the voltage is within the ADC-sensing range.

Table 1 shows the voltage-supporting range for different VID steps and voltage-sensing gains.

**Table 1: Voltage Support Range**

External V <sub>OUT</sub> Divider	VID Table	RS Gain	V <sub>DIFF/VFB</sub> ADC Gain	V <sub>OUT</sub> Range
N	5mV	1	1	0V to 1.55V
N	5mV	0.5	1	0V to 2.155V
N	10mV	1	1	0V to 1.55V
N	10mV	0.5	1	0V to 3.1V
Y	5mV/ 10mV	1	1	>3V

When V<sub>OUT</sub> exceeds 3V in non-Intel applications, an external resistive divider must be connected from VOUT to VORTN, then tapped to VOSEN (see Figure 4). Set the MP2975's resistor dividing ratio using register VOUT\_SENSE\_SET (29h).



**Figure 4: DC Loop Gain Selection**

### Active Voltage Positioning (AVP)

The MP2975 supports active voltage positioning (AVP). With AVP, the output voltage drops gradually as the load current increases. It is also

known as load line. The relationship between the output voltage and load current is estimated with Equation (3):

$$V_{\text{OUT}@I_{\text{OUT}}} = V_{\text{OUT}@\text{NO LOAD}} - I_{\text{OUT}} \times R_{\text{LL}} \quad (3)$$

Where  $R_{\text{LL}}$  is the load-line resistor.

The MP2975 provides a PMBus-configurable load line, calculated with Equation (4):

$$R_{\text{LL}} = \frac{\text{IDROOP\_GAIN\_SET}}{256} \times K_{\text{CS}} \times R_{\text{DROOP}} \times \frac{1}{G_{\text{RS}}} \quad (4)$$

Where  $K_{\text{CS}}$  is the current-sense gain of the Intelli-Phase™ (in A/A), IDROOP\_GAIN\_SET is a decimal value ranging from 0 to 256 (when IDROOP\_GAIN\_SET = 0, AVP is disabled),  $R_{\text{DROOP}}$  is an internal resistor across VFB and VDIFF (in  $\Omega$ ), and  $G_{\text{RS}}$  is the remote-sense gain.  $G_{\text{RS}}$  can be half or unit gain.

Both IDROOP\_GAIN\_SET and  $R_{\text{DROOP}}$  are set by registers 06h/16h on page 2.

For non-load-line VR applications, the MP2975 provides AC-DROOP functionality to increase the phase margin of the loop regulation. The AC-DROOP function injects the AC component of the total inductor current to  $R_{\text{DROOP}}$ , to introduce the current signal to the loop regulation. Enable AC-DROOP via registers 01h/11h on page 2. The AC-DROOP related parameters can be configured via PMBus registers 06h/16h on page 2. See the Register Map on page 43 for more information.

### Set Start-Up Voltage

The MP2975 sets the start-up voltage via registers 0Dh/1Dh on page 2 for rail 1 and rail 2, respectively.

In SVID control mode and PMBus override control mode, the start-up slew rate can be set to either “slow slew rate” or “ $V_{\text{OUT}}$  transition slew rate.” In AVSBus control mode, the start-up slew rate is always slow slew rate.

The slow slew rate is proportional to the fast slew rate. The proportion is determined by bit[11:8] of registers 01h/11h on page 2 (see Table 2).

**Table 2: Slow Slew Rate**

Bit[11:8] of 01h/11h on Page 2	Slow Slew Rate
4'b1xxx	FAST_SR / 16

4'b01xx	FAST_SR / 8
4'b001x and 4'b0000	FAST_SR / 4
4'b0001	FAST_SR / 2

The fast slew rate (FAST\_SR) is estimated with Equation (5):

$$\text{FAST\_SR} = \frac{\text{VID\_STEP}(\text{mV})}{\text{SLEW\_FAST\_CNT} \times 0.05(\mu\text{s})} \quad (5)$$

Where VID\_STEP can be set to 5mV or 10mV, and SLEW\_FAST\_CNT ranges from 1 to 63 (and is determined by bit[5:0] of registers 01/11h on page 2).

The  $V_{\text{OUT}}$  transition slew rate is calculated with Equation (6):

$$\text{TRANS\_SR} = \frac{\text{VID\_STEP}(\text{mV})}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu\text{s})} \quad (6)$$

Where VID\_STEP can be either 5mV or 10mV, and VOUT\_TRANS\_CNT is the decimal value in VOUT\_TRANSITION\_RATE (27h), bit[8:0], which ranges from 1 to 511.

### PVID Mode

The MP2975 supports 3-bit PVID mode to control  $V_{\text{OUT}}$  by setting the PVID\_EN bit in register 5Eh.

The PVID mode pins (PVID1, PVID2, and PVID3) are multiplexed from SCLK, SDIO, and ALT#. In PVID mode, SVID and AVSBus communication are disabled.

When any of the PVID pins toggle, the internal VID value slews to a new target VID.

There are 8 sets of PVID voltages with different combinations of high/low logic on PVID1, PVID2, and PVID3. Registers BAh ~ C1h on page 1 with target voltage values should be pre-configured corresponding to certain logics (see Table 3).

**Table 3: Set PVID Voltage by PVID Pins**

PVID Rail 1	PVID Rail 2	PVID1 (Pin 17)	PVID2 (Pin 18)	PVID3 (Pin 19)
BAh[7:0]	BEh[7:0]	L	L	L
BAh[15:8]	BEh[15:8]	L	L	H
BBh[7:0]	BFh[7:0]	L	H	L
BBh[15:8]	BFh[15:8]	L	H	H
BCh[7:0]	C0h[7:0]	H	L	L
BCh[15:8]	C0h[15:8]	H	L	H
BDh[7:0]	C1h[7:0]	H	H	L
BDh[15:8]	C1h[15:8]	H	H	H

**AVSBus Mode**

The MP2975 supports the AVSBus control mode.

In AVSBus mode, the communication signals AVS\_CLK and AVS\_MOSI are multiplexed from the SCLK and SDIO as input pins. The user must configure the AVS\_MISO pin according to the electrical voltage level on the AVSBus supply.

For applications where the AVSBus supply is  $\leq$  1.8V, the AVS\_MISO pin is multiplexed from the ALT# pin. For applications with the AVSBus supplies is between 1.8V and 3.3V, AVS\_MISO is multiplexed from the VRHOT# pin as AVS\_MISO\_HV. The AVS\_MISO/AVS\_MISO\_HV pin is open-drain, so connect it to the AVSBus supply using a pull-up resistor.

The MP2975 supports all of the AVSBus protocol specified commands:

- Voltage read/write
- $V_{OUT}$  transition rate read/write
- Current read
- Temperature read
- Voltage reset
- Power mode read/write
- AVSBus status read/write
- AVSBus version read

The MP2975 also supports slave interruption.

In AVSBus mode, SVID communication is disabled. The AVSBus address setting is the same as the SVID address with register MFR\_ADDR\_SVID\_AVSBUS (05h on page 2).

**SVID Interface**

To support multiple VR devices on the same SVID bus, register MFR\_ADDR\_SVID\_AVSBUS (05h on page 2) configures the SVID address.

The SVID address is a 4-bit code. There are 14 addresses for up to 14 voltage regulator controllers, or voltage rails. The final addresses (0Eh and 0Fh) are reserved all call addresses, and all the VR controllers will respond to them. The user can configure bit[10:9] in 05h on page 2 to select 0Eh and/or 0Fh as the all call addresses.

The SVID address of rail 1 and rail 2 are set by MFR\_ADDR\_SVID\_AVSBUS (05h on page 2). See the Register Map on page 43 for more details.

If rail 2 does not require an SVID address, the user can set rail 2 to reject all the SVID commands from the processor via bit[13] of register MFR\_VR\_MULTI\_CONFIG\_R2 (1Dh on page 2).

**Dynamic Voltage Identification (DVID)**

The MP2975 supports dynamic output voltage transition by changing the VID code with the PMBus interface, AVSBus interface, or SVID interface, or by toggling the PVID pins.

In PMBus override control mode and PVID control mode, the DVID slew rate is set to the  $V_{OUT}$  transition slew rate, calculated with Equation (6).

In SVID control mode, the DVID slew rate is determined by the SetVID command. The slew rate of the SetVID\_Fast command is calculated with Equation (5), and Table 2 shows the slew rate of the SetVID\_Slow command. The slew rate of the SetVID\_Decay command can be set to slow slew rate or free mode, in which all PWMs turn to tri-state and the  $V_{OUT}$  slew rate is determined by the  $C_{OUT}$  value and the load current. See bit[9] of register MFR\_VR\_CONFIG1 (68h) on page 73 for more details.

In AVSBus control mode, the DVID slew rate is determined by the  $V_{OUT}$  transition rate write command, which is an integer with 1LSB = 1mV/ $\mu$ s. In one  $V_{OUT}$  transition rate command, the rising slew rate is sent first, followed by the falling slew rate. The initial rising and falling slew rates are determined by VOUT\_TRANSITION\_RATE (27h), calculated with Equation (7):

$$\text{AVS\_SR\_INI} = \frac{100(\text{mV}/\mu\text{s})}{\text{VOUT\_TRANS\_CNT}} \quad (7)$$

Where VOUT\_TRANS\_CNT is the decimal value in VOUT\_TRANSITION\_RATE (27h), bit[8:0], which ranges from 1 to 511.

During a VID transient, the MP2975 forces the VR into full-phase CCM, regardless of the power state setting. For example, if the controller is configured in 6-phase mode but is running in 1-phase DCM due to auto phase-shedding, a VID transition command forces the controller to run into 6-phase CCM immediately.

### Overclocking

The MP2975 supports two overclocking modes:

- Tracking mode:** In tracking mode, the VR controller adds an offset VID via the PMBus command VOUT\_OFFSET (1Eh on page 2). When the CPU changes VID, the VR provides an output by summing the VID from the CPU SetVID command and VID offset from VOUT\_OFFSET. One exception is when the VR receives a SetVID to 0V command from the CPU, during which the output voltage goes to 0V, and the VID offset is ineffective.

VOUT\_OFFSET (1Eh on page 2) sets the VID steps offset from -128 to +127. At 5mV VID, the maximum offset is 0.635V, and the maximum V<sub>OUT</sub> is 2.155V. At 10mV VID, the maximum offset is 1.27V, and the maximum V<sub>OUT</sub> is 3V.

Tracking mode is effective with SVID, PMBus, PVID, and AVSBus modes. Write a non-zero value in the VOUT\_OFFSET register to enable overclocking tracking mode. If the VR is operating while updating VOUT\_OFFSET, the output voltage slews to the new target immediately.

- Fixed mode:** Fixed voltage margining is used in extreme overclocking applications, where a fixed voltage can provide additional stability. In this mode, a fixed voltage is commanded via the PMBus command VOUT\_COMMAND (21h), and the VR output voltage is fixed at this voltage, regardless of a VID changing command from the CPU. When the CPU issues a SetVID command, the VR acknowledges the command and asserts

ALERT# immediately, but maintains the voltage commanded by VOUT\_COMMAND (21h), while the VR output voltage stays at the fixed VID.

Fixed mode is only available during SVID override mode. To enable fixed mode, set MFR\_VR\_CONFIG1 (68h on page 0), bit[0] = 1. At 5mV VID, the maximum V<sub>OUT</sub> is to 2.72V with the VID table extending. At 10mV VID, the maximum V<sub>OUT</sub> is 3V.

### Inductor Current Sensing and Reporting

The MP2975 works with the Intelli-Phase™ to enable inductor current sensing (see Figure 5). The cycle-by-cycle sensed inductor current is used for multi-phase current balancing, thermal balancing, and per-phase current limitation.

When working with DrMOS, which requires an external reference voltage for current sensing, the MP2975's VDD18 can be used as the reference voltage.

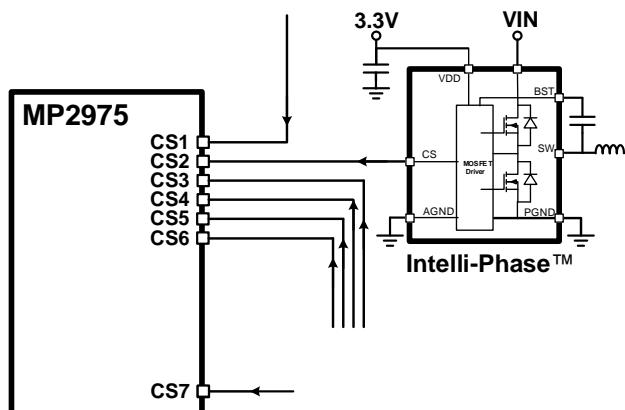


Figure 5: Phase Current Sense

By using the Intelli-Phase™, the MP2975 does not require applied temperature compensation and impedance matching (like traditional DCR sensing) to achieve accurate current sense.

### Total Current Sense

All sensed currents from the CS pins are summed, and generate a configurable, proportional current that is applied to an internal resistor — which is also configurable — to get the IMON voltage (V<sub>IMON</sub>). Configure the current gain and resistor value in registers 0Ch/1Ch on page 2.

V<sub>IMON</sub> is sampled, calculated, and stored in the I<sub>OUT</sub> reporting register. The value in the I<sub>OUT</sub> register is reported by the processor to avoid exceeding the

thermal design point and the system's maximum current capability.

If the auto phase-shedding function is enabled, the  $I_{OUT}$  report determines the real-time phase count that flattens the overall efficiency over the whole operating current range.

The MP2975 provides a user-configurable scaling factor and a user-configurable current offset. The configurable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range, and maximizes the performance of the processor turbo.

Figure 6 shows the MP2975 IMON sense and report block diagram.

GAIN\_PMBUS, GAIN\_EXPONENT and OFFSET\_PMBUS convert the ADC-sensed  $V_{IMON}$  to the direct format with 1A/LSB, then reports it via the PMBus command READ\_IOUT (8Ch). See the

page 2 registers (0Bh/1Bh) and IOUT\_CAL\_OFFSET (54h) on page 60 for more details.

IMON\_DGTL\_GAIN fine-tunes the output current report gain for SVID and AVSBus with a 0.1% resolution. It is in page 2 registers 0C/1Ch.

GAIN\_SVID and OFFSET\_SVID convert the fine-tuned value (IMON\_TRIM) to the SVID current reported format ( $FFh = I_{CCMAX}$ ,  $I_{CCMAX}$  can be set to exceed 255A and to be compliant with VR13.HC spec). GAIN\_AVIS, GAIN\_AVIS\_RES, and OFFSET\_AVIS convert IMON\_TRIM to the AVSBus current-reported format.

The SVID and AVSBus current report share the same gain/offset registers. See the page 2 registers 08h/09h/18h/19h on page 43 for more details. The GAIN\_SVID for VR13. HC is in page 2 register 0Ah.

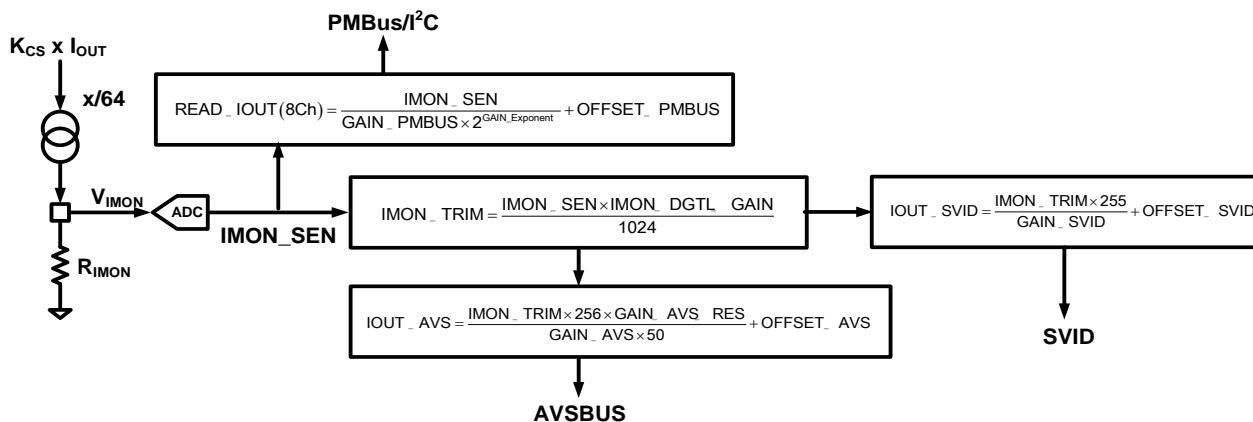


Figure 6: Total Current Sense and Report

### Phase Number Configuration

The MP2975 provides a total of 8 PWM pins, and can be configured to different phase count applications for rail 1 and rail 2. Table 4 shows phase setting examples. Applications include but are not limited to these examples.

Table 4: Phase Count Configuration and Active PWM Pins

Phase Count Registers		Active PWM Pins	
0Dh on page 2, Bit[3:0]	1Dh on page2, Bit[2:0]	Rail 1	Rail 2
4'b1000	3'b000	1 – 8	N/A
4'b0111	3'b001	1 – 7	8
4'b0110	3'b010	1 – 6	7, 8
4'b0101	3'b011	1 – 5	6, 7, 8
4'b0100	3'b100	1 – 4	5 – 8
4'b0011	3'b100	1, 2, 3	5 – 8
4'b0010	3'b111	1, 2	5 – 8
4'b0010	3'b100	1, 2	5 – 8
4'b0010	3'b011	1, 2	6, 7, 8
4'b0010	3'b010	1, 2	7, 8
4'b0010	3'b001	1, 2	8
4'b0001	3'b111	1	5 – 8
4'b0001	3'b100	1	5 – 8
4'b0001	3'b001	1	8

Rail 2 can only be set to 4 phases at most. When rail 1's phase count is configured as 0, rail 1 operates with 1-phase DCM. When rail 2's phase count is configured as 0, rail 2 is disabled.

Any unused PWM pin enters tri-state. The active phase interleaves automatically. Float the unused PWM and CS pins.

When rail 2 of the MP2975 is unused, tie EN2 to AGND, and connect VOSEN2 and VORTN2 to AGND.

### Auto Phase-Shedding (APS)

To improve the efficiency over the entire load range, the MP2975 supports automatic phase-shedding (APS) according to the load current report. If APS mode is enabled, any SVID SetPS commands will be acknowledged, but will not affect the operating phase count.

In APS mode, the VR can be optimized to adjust the phase count to balance the performance between transient and power consumption.

Figure 7 shows how the VR optimizes efficiency by working in 7-phase CCM under heavy loads, and 1-phase CCM at light loads. The VR enters 1-phase DCM at extreme light-load to further reduce switching loss.

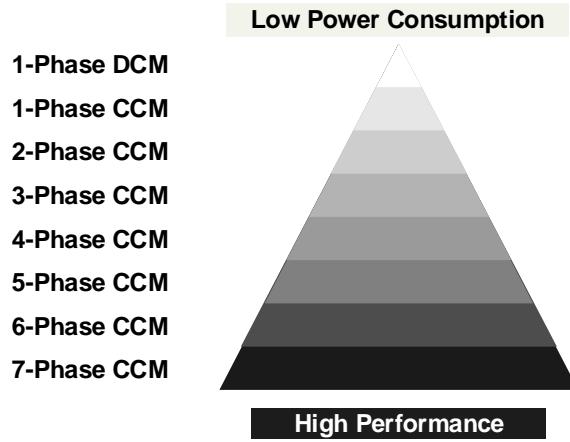


Figure 7: APS in 7-Phase Mode

APS is implemented by comparing the sensed load current with each power state's current threshold. Program drop-phase current thresholds for rail 1 and rail 2 in registers 06h/07h/08h/0Ah/0Bh/0Ch on page 1.

To prevent the converter from changing the power state back and forth at a steady load current, the hysteresis for all APS levels is set with register 09h/0Dh on page 1. Figure 8 shows the APS current threshold setting from 4-phase CCM to 3-phase CCM.

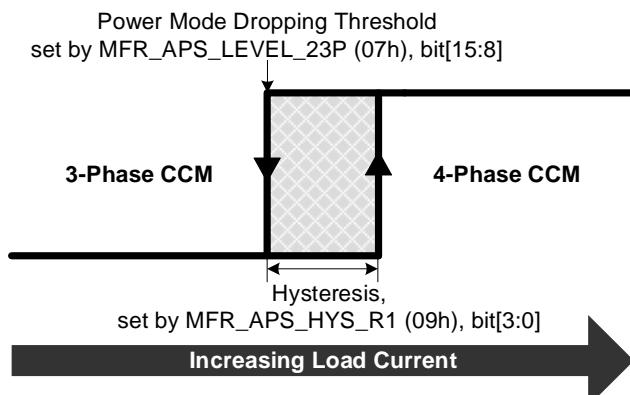


Figure 8: APS Threshold Setting between 4-Phase CCM and 3-Phase CCM

Table 5 lists the phase-shedding and phase-adding entry conditions based on the current report for 7-phase applications.

Table 5: Phase-Shedding/Adding Based on Current Report for 7-Phase Applications on Rail 1

Condition	Power State
$I_{LOAD} > DROP\_LEVEL\_6P + MFR\_APS\_HYS$	7-phase CCM
$DROP\_LEVEL\_5P + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_6P$	6-phase CCM
$DROP\_LEVEL\_4P + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_5P$	5-phase CCM
$DROP\_LEVEL\_3P + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_4P$	4-phase CCM
$DROP\_LEVEL\_2P + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_3P$	3-phase CCM
$DROP\_LEVEL\_1P + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_2P$	2-phase CCM
$DROP\_LEVEL\_DCM + MFR\_APS\_HYS < I_{LOAD} \leqslant DROP\_LEVEL\_1P$	1-phase CCM
$I_{LOAD} < DROP\_LEVEL\_DCM$	1-phase DCM

The MP2975 exits auto phase-shedding and runs in full-phase CCM under three conditions. This capability accelerates load transient response and reduces output voltage undershoot. The conditions are listed below:

1. On-the-fly VID (DVID) forces the controller into full-phase CCM. After the output voltage settles to the target value, the new power state is determined by the load current.
2. Load step-up causes VFB- window tripping, which triggers full-phase CCM to reduce output voltage undershoot.
3. Load step-up causes the frequency changes to exceed a configurable, limited threshold, and triggers full-phase running.

#### VFB Window

The MP2975 has a VFB window ( $V_{REF} - 25mV$  to  $V_{FB} + 20mV$ ) that provides advanced nonlinear loop control to fasten the transient performance.

When the feedback voltage ( $V_{FB}$ ) exceeds  $V_{REF} + 20mV$  ( $V_{FB+}$  window), all PWMs pull low and blank the set PWM signal until  $V_{FB}$  falls below the  $V_{FB+}$  window. The  $V_{FB+}$  window reduces overshoot when the load releases, especially during multi-phase operation.

When VFB is below  $V_{REF} - 25\text{mV}$  ( $V_{FB}$ - window), the VR exits auto-power state mode immediately and enters full-phase running to improve transient response.

### Current Balance and Thermal Balance Loop

The MP2975 provides a current balance loop to achieve fair current sharing during multi-phase mode when different circuit impedances lead to phase-current differences.

The phase current is sensed and calculated with the current reference in the current loop. Each phase's PWM on time is adjusted individually to balance the currents accordingly.

The MP2975 applies sigma-delta ( $\Sigma-\Delta$ ) modulation and delay line-loop (DLL) technology for current-balance modulation to increase the resolution of the current-balance modulation and reduce PWM jitter. The time resolution of the digital system is 5ns. By applying  $\Sigma-\Delta$  modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

With current balance loop, the MP2975 provides current offsets on the ADC-sensed voltages from CS2 to CS12 to achieve thermal balance. The offsets are set with PMBus registers 99h/9Ah/9Bh/9DhA on page 1. The phases that have better cooling capability can take more phase current by adding an offset to the sensed CS voltage.

The bandwidth of the current loop is relatively lower than the output voltage regulation loop, so that it will not impact the output voltage regulation.

### Input Voltage Sensing

The input power supply voltage can be sampled at the VINSEN1 and VINSEN2 pins for rail 1 and rail 2, respectively (see Figure 9). The sensed input voltage is used for PWM on-time calculations,  $V_{IN}$  under-voltage lockout (UVLO) and  $V_{IN}$  over-voltage protection (OVP),  $V_{IN}$  under-voltage (UV) warning, and input voltage monitoring. Connect a 16:1 resistive divider between the VINSEN1 and VINSEN2 pins to proportionally reduce the input voltage signal within a 1.6V ADC-sense range.

For applications where rail 1 and rail 2 share the same input power supply, VINSEN2 can be omitted and pin 36 can be reused as the PSYS pin. In this case, VINSEN1 senses the input voltage on both rails.

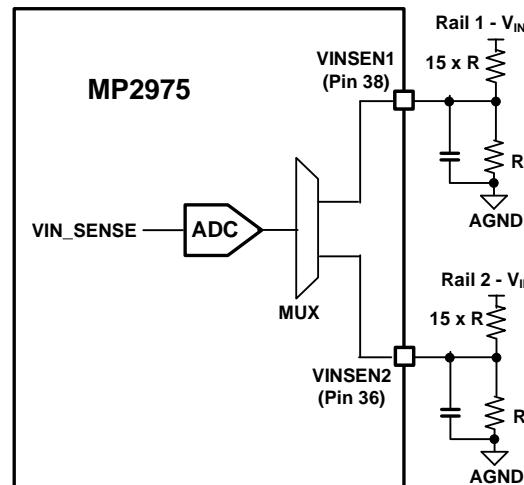


Figure 9: VIN-Sensing Block Diagram

### Input Current and Input Power Sensing

The MP2975 supports two methods to sense the input current and input power. The first method is by working with the current-shunt monitor (see Figure 10). The current-shunt monitor converts the differential voltage of the shunt to a small current (or voltage) signal that is proportional to the input current. Apply this current (or voltage) signal on  $R_{PSYS}$ , which is connected between the PSYS pin and AGND. The device senses this voltage and uses it to calculate input current, then calculates input power by multiplying the input current and input voltage.

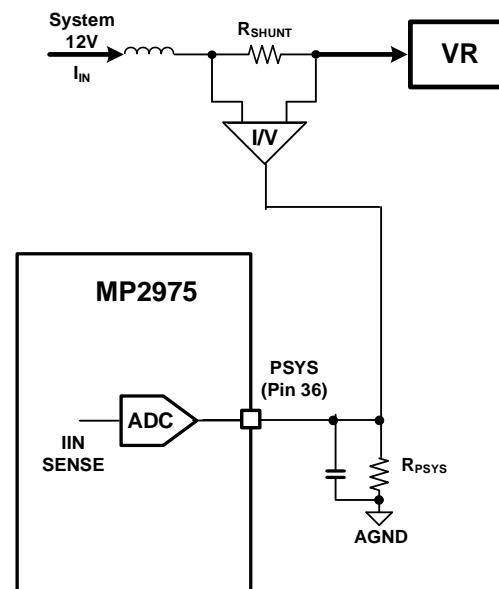


Figure 10: Input Current Sense Block Diagram

Another method is to calculate input power via one real-time PWM period, then divide that value by the input voltage to calculate the input current. In this case, short the PSYS pin to AGND.

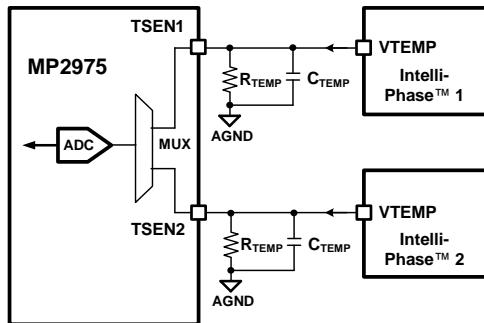
The methods selection bit is bit[9] of register MFR\_IIN\_CAL\_IMON\_OFFSET\_R1 (09h on page 2).

### Temperature Sensing

The MP2975 senses the Intelli-Phase's™ temperature by connecting the Intelli-Phase™ VTEMP pin to the MP2975's TSEN1 or TSEN2 pin (see Figure 11).

The sensed temperature via TSEN1 is used for over-temperature fault protection, over-temperature warning (assert VRHOT# pin), and power stage temperature monitoring.

The TSEN2 serves as a general purpose analog input. The MP2975 provides TSEN2 analog fault protection and digital fault protection. Programming the analog/digital fault threshold allows the TSEN2 to monitor over-temperature protection. However, temperature sensing via TSEN2 is not used for temperature reporting, and will not assert VR\_HOT# once an analog or digital fault is triggered on TSEN2



**Figure 11: Temperature Sense with Intelli-Phase™**

$C_{TEMP}$  is a filtering capacitor on the VTEMP pin. It is recommended to use a low (about 1nF to 10nF) ceramic capacitor for  $C_{TEMP}$ .

$R_{TEMP}$  is a discharging resistor ranging from 10kΩ to 49.9kΩ.

The VTEMP pin of the Intelli-Phase™ reports a voltage output proportional to the junction temperature( $T_J$ ), estimated with Equation (8):

$$T_J(^{\circ}\text{C}) = a \times V_{\text{TEMP}}(\text{V}) + b \quad (8)$$

Where  $a$  is the temperature gain (in  $^{\circ}\text{C}/\text{V}$ ), and  $b$  is the temperature offset (in  $^{\circ}\text{C}$ ). For example, when  $a = 100^{\circ}\text{C}/\text{V}$ ,  $b = 10^{\circ}\text{C}$ , and VTEMP's voltage is 700mV, the junction temperature ( $T_J$ ) of the Intelli-Phase™ is 80°C. Refer to the Intelli-Phase™ datasheet for more details on the  $a$  and  $b$  values.

### Low-Power Mode

The MP2975 can be configured to low-power mode or regular-power mode with PMBus command MFR\_VR\_CONFIG3 (35h), bit[4].

When low-power mode is enabled and both EN1 and EN2 are low, PMBus communication is disabled and the VDD33 supply current can be extremely reduced.

In regular-power mode, PMBus communication is available, so the user can change the configurations in the MTP when both EN1 and EN2 are low.

### DrMOS Standby

The MP2975 can force the DrMOS into power-saving mode by asserting the STANDBY pin to low or Hi-Z. STANDBY can be asserted when both rails are in PS4 state, or when both rails are off due to EN off (in regular-power mode) or OPERATION command off. See register MFR\_VR\_CONFIG4 (B0h on page 1) on page 164 for more details.

### Start-Up

The VDD33 pin supplies the MP2975 with a 3.3V voltage. It provides the bias supply for the analog circuit and internal 1.8V LDO. The 1.8V LDO produces the 1.8V supply for digital circuits.

The system is reset by the internal power-on reset (POR) signal after the VDD33 supply is ready. After the system exits POR, the data in the MTP is loaded into the operating registers to configure VR operation.

Figure 12 shows the MP2975's start-up sequence in regular-power mode. Details are below:

t0 to t1: At t0, VDD33 is supplied with a 3.3V voltage that reaches the VDD33 under-voltage lockout (UVLO) on threshold at t1. VDD18 reaches 1.8V when the VDD33 pin exceeds 1.8V.

t1 to t2: At t1, the data in the MTP starts loading into the operating registers. The entire MTP

copying process typically takes about 1.5ms. During this stage, the PMBus address is detected if the user selected the voltage on the ADDR\_PL pin to set the PMBus address.

t<sub>2</sub> to t<sub>3</sub>: At t<sub>2</sub>, the MP2975 waits for either EN pin to pull high after MTP copying finishes. The PMBus is available at this stage.

t<sub>3</sub> to t<sub>4</sub>: If the PMBus command OPERATION (01h, page 0) is preset to “off” after the EN1 pin pulls high, rail 1 halts at this stage and waits for an OPERATION on command. If the OPERATION command is pre-configured to “on,” the turn-on delay time ( $t_{ON}$  delay) starts counting. The  $t_{ON}$  delay time is configurable from 0ms to 3276.75ms via PMBus command TON\_DELAY (60h on page 0).

t<sub>4</sub> to t<sub>5</sub>: When the  $t_{ON}$  delay expires, the rail 1 VID DAC starts ramping up with the configured slew rate to V<sub>REF1</sub>, which is the start-up voltage. During soft start, OCP\_TOTAL protection, OVP2, and UVP are masked until VREF1 reaches the target value. Rail 1’s start-up is completed at t<sub>5</sub>. After t<sub>5</sub>, rail 1 is ready to output power, do DVIDs, and take other power actions.

t<sub>6</sub> to t<sub>7</sub>: At t<sub>6</sub>, EN2 asserts, and OPERATION (01h at page 1) is set to on. Rail 2 begins the  $t_{ON}$  delay, which is configurable with register TON\_DELAY (60h at page 1).

t<sub>7</sub> to t<sub>8</sub>: When the  $t_{ON}$  delay expires, the rail 2 VID DAC output starts ramping up VREF2. This is the soft start for rail 2. At t<sub>8</sub>, the start-up sequence for both rails is complete.

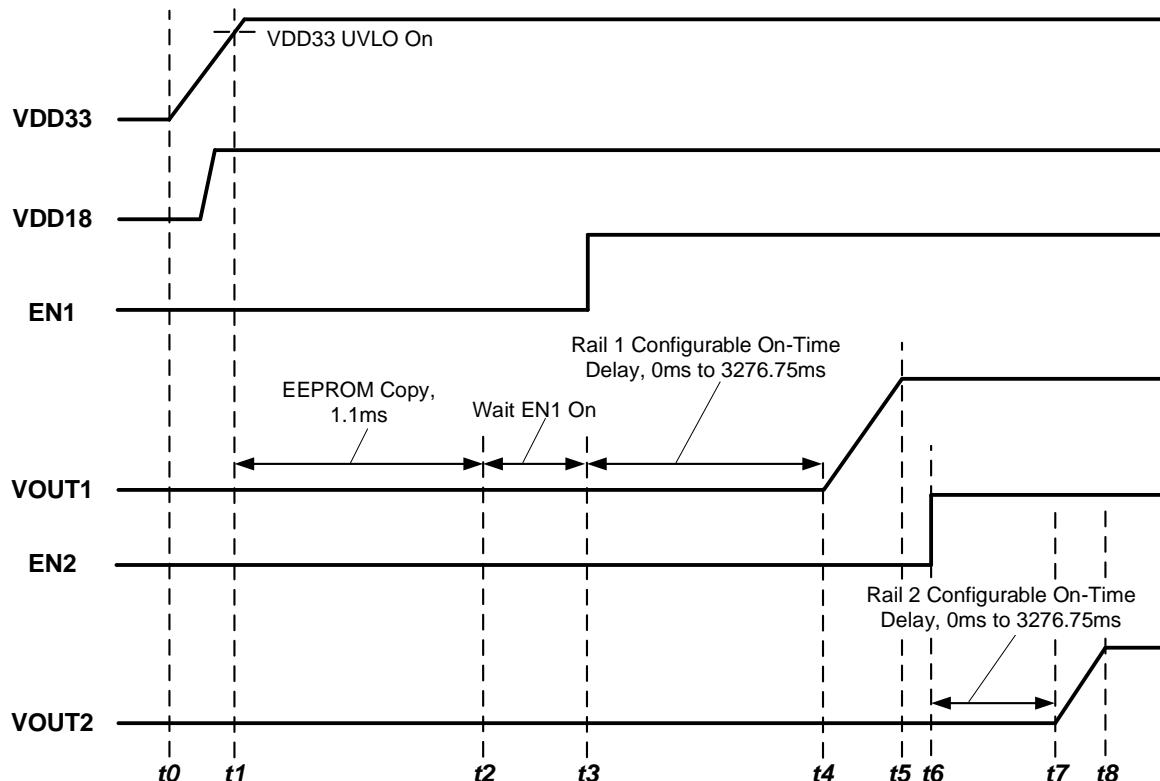


Figure 12: Start-Up in Regular-Power Mode

Figure 13 shows start-up in low-power mode. Details are below:

t0 to t1: At t0, VDD33 is supplied by a 3.3V voltage, and it reaches VDD33's under-voltage lockout (UVLO) on threshold at t1. VDD18 reaches 1.8V when the VDD33 pin exceeds 1.8V.

t1 to t2: At t1, VDD33 exceeds the UVLO on threshold, then the MP2975 waits for either EN pin to pull high. The PMBus is unavailable at this stage.

t2 to t3: At t2, EN1 pulls high and the data in the MTP starts loading into the operating registers. The entire MTP copy process typically takes about 1.5ms. During this stage, the PMBus address is detected if the user selected the voltage on the ADDR\_PL pin to set the PMBus address.

t3 to t4: If OPERATION (01h, page 0) is preset to "off" after MTP copying is finished, rail 1 halts at this stage and waits for an OPERATION on command. If OPERATION is pre-configured to "on," the turn-on delay time ( $t_{ON}$  delay) starts counting.

t4 to t5: When the  $t_{ON}$  delay expires, VID DAC starts ramping up VREF1 to the start-up voltage with the configured slew rate. During soft start, OCP\_Total protection, OVP2, and UVP are masked until VREF1 reaches the target value.

t6 to t8: At t6, EN2 asserts. The start-up for rail 2 follows the same sequence that is initiated during regular-power mode.

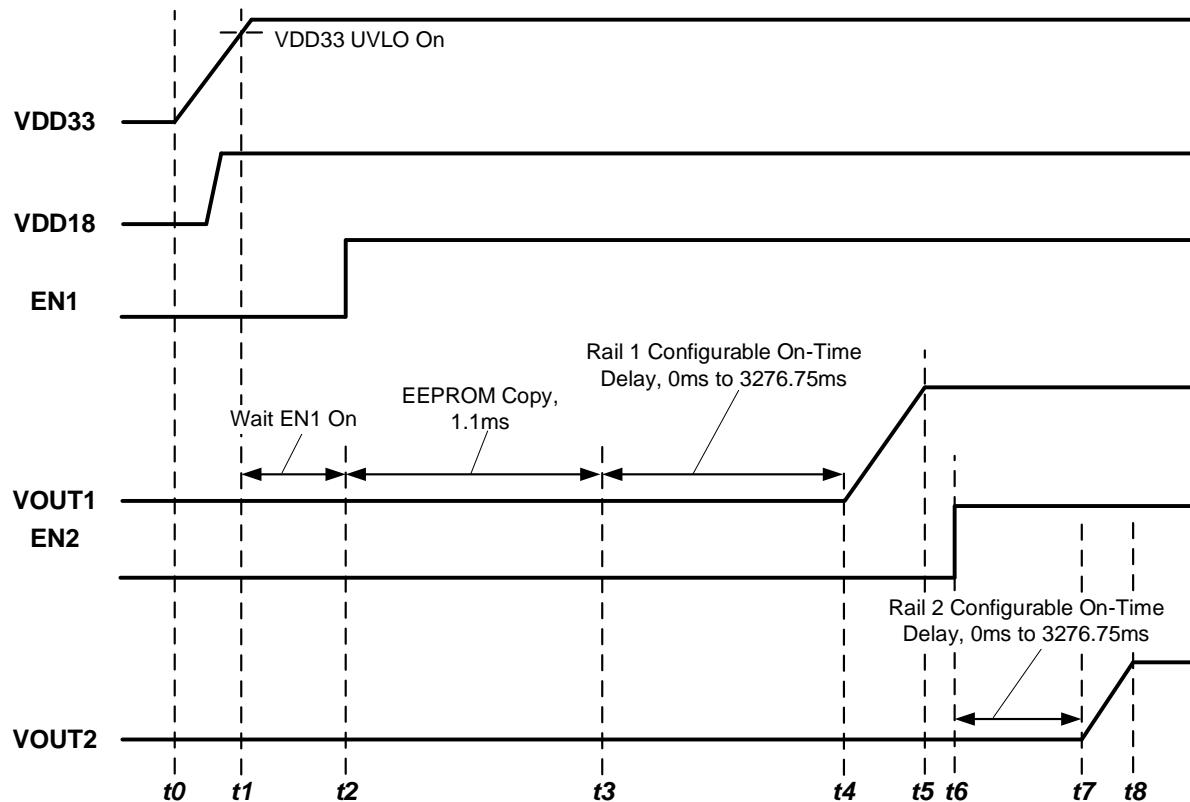


Figure 13: Start-Up in Low-Power Mode

## Shutdown

The MP2975 can be powered off by VDD33 under-voltage lockout (UVLO), the EN pin, the OPERATION command, SVID command, or protection shutdown. Each is described below:

**VDD33 UVLO:** Once the power supply on the VDD33 pin falls below the VDD33 under-voltage lockout (UVLO) falling threshold, the MP2975 shuts down immediately.

**EN pin off:** The MP2975 provides Hi-Z off and soft-off with a selectable slew rate when the EN pin toggles low in regular-power mode. See SVID\_PHSHD\_VR\_CONFIG (15h on page 2) on page 192 for more details. During soft-off, VOUT ramps down with the selected slew rate until  $V_{REF}$  falls to the VID shutdown level, which is set by register MFR\_VR\_CONFIG2 (5Eh), bit[8:0]. Then all PWMs enter tri-state.

A turn-off delay time can be added via register TOFF\_DELAY (64h).

When both EN pins are off during low-power mode, the MP2975 initiates Hi-Z off immediately without a turn-off delay and enters standby mode with minimal power consumption. The PMBus is unavailable until either EN pin pulls high.

**Operation command off:** The MP2975 provides Hi-Z off and soft-off when the OPERATION command is set to off. When the OPERATION command is set to Hi-Z off, all PWMs enter tri-state when the command is received, and VOUT

is discharged by the load current. When the OPERATION command is soft-off, VOUT begins soft shutdown with the slow slew rate until  $V_{REF}$  reaches the VID shutdown level. Then all PWMs enter tri-state.

A turn-off delay time can be added at OPERATION command soft-off via register TOFF\_DELAY (64h).

**SVID command off:** When the MP2975 receives the SetVID command to 0V, the MP2975 begins to shut down immediately. After the MP2975 enters the VID off state, it waits for the next SetVID command to exceed 0V before starting up again without the  $t_{ON}$  delay.

**Protection shutdown:** If  $V_{IN}$  over-voltage protection (OVP),  $V_{IN}$  under-voltage lockout (UVLO),  $V_{OUT}$  under-voltage protection (UVP),  $I_{OUT}$  over-current protection (OCP), over-temperature protection (OTP), CS fault, or VTEMP fault from Intelli-Phase™ are triggered, the VR enters Hi-Z off immediately.

When  $V_{OUT}$  OVP is triggered, the VR turns on all the active low-side MOSFETs to discharge  $C_{OUT}$ . The device shuts down immediately until  $V_{OUT}$  falls below the reverse-voltage protection (RVP) level (about 150mV).

Figure 14 shows the EN pin's soft-off sequence in regular-power mode.

Figure 15 shows the EN pin's Hi-Z off sequence in low-power mode. When both EN pins are pulled low, the device shuts down immediately without a  $t_{OFF}$  delay.

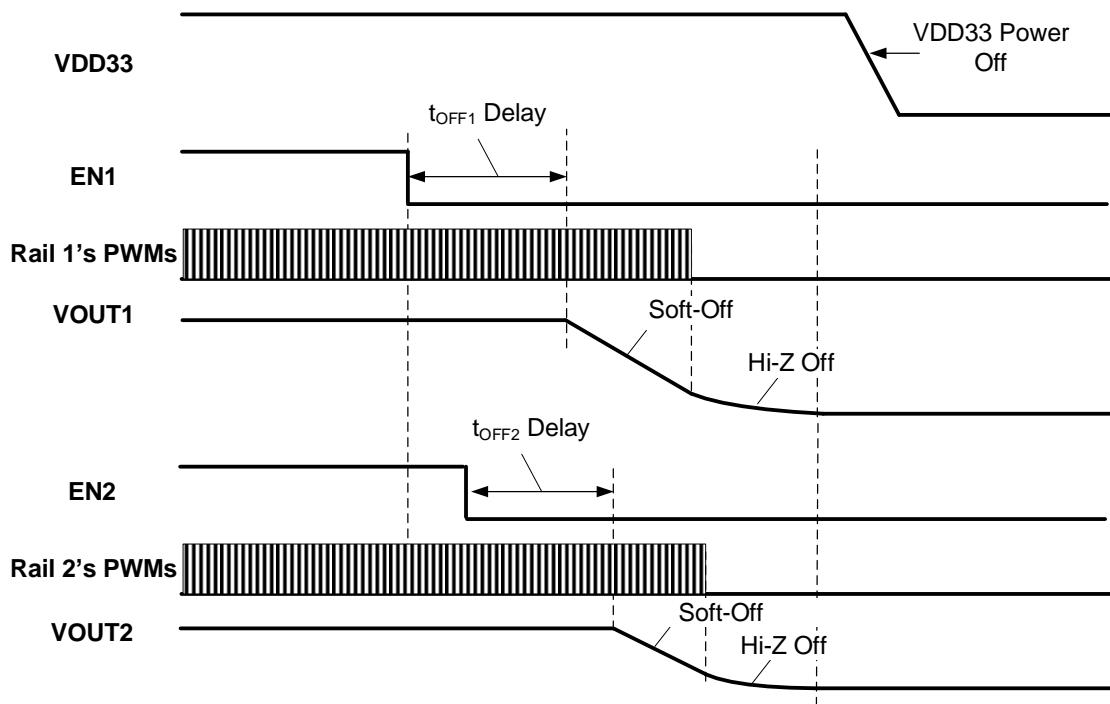


Figure 14: Shutdown in Regular-Power Mode with Soft Off

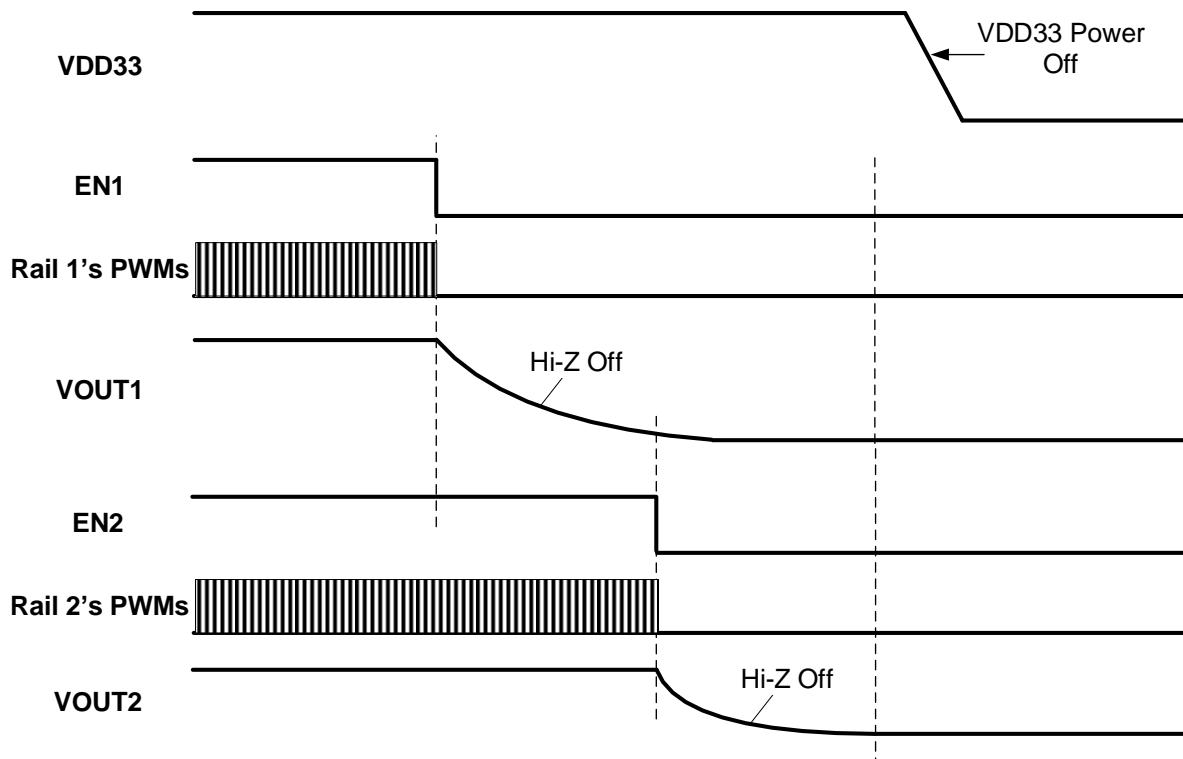


Figure 15: Shutdown in Low-Power Mode with Hi-Z Off

## Power Good (PG) Indication

The MP2975 indicates power good with VRRDY1 (rail 1) and VRRDY2 (rail 2). There are 2 modes available for VRRDY pin assertion:

Non-Intel mode: The power good on/off thresholds are configurable via registers POWER\_GOOD\_ON (6Eh) and POWER\_GOOD\_OFF (6Fh).

When  $V_{REF}$  rises above the POWER\_GOOD\_ON threshold during soft start, the MP2975 starts counting the delay time, and asserts VRRDY when the delay ends. The delay time is

configurable via the register MFR\_PGOOD\_SET (6Dh).

When  $V_{REF}$  is below the POWER\_GOOD\_OFF threshold after start-up finishes, the MP2975 de-asserts the VRRDY pin immediately. Set the POWER\_GOOD\_OFF threshold below the VID value that is regulated during normal operation.

If the MP2975 is in Hi-Z off for the fault protections, the PMBus OPERATION command is off, or the EN pin pulls low, the VRRDY pin de-asserts immediately.

Figure 16 shows power good indication during regular-power mode.

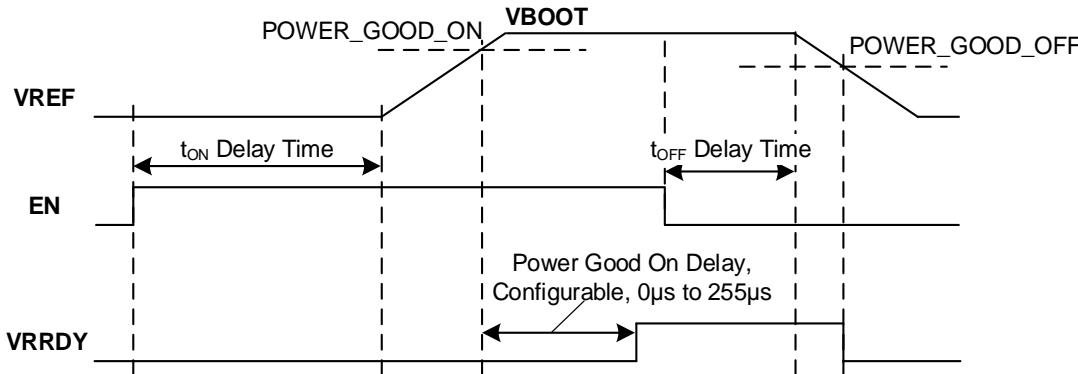


Figure 16: Power Good On/Off Sequence during Regular-Power Mode and EN Soft-Off

Intel mode: The VRRDY pin asserts when the MP2975's start-up voltage is 0V and TON\_DELAY expires.

When the MP2975's start-up voltage exceeds 0V, the VRRDY pin asserts once the start-up voltage settles.

If start-up has ended and the CPU sends the VID command to 0V when register SVID\_PSHED\_VR\_CONFIG (15h) bit[1:0] is 0, the VRRDY pin de-asserts immediately. If register SVID\_PSHED\_VR\_CONFIG (15h) bit[1:0] is 1, the VRRDY pin continues asserting with VID = 0V.

In PG Intel mode, the associated VRRDY is de-asserts immediately when the VR shuts off for the fault protections, PMBus OPERATION command is off, or the EN pin pulls low.

## Faults and Protections

The MP2975 supports flexible fault monitoring. Protections are described below:

## $V_{IN}$ Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

If the sensed input voltage drops below the  $V_{IN\_OFF}$  threshold, the VR shuts off immediately by forcing the PWM signals to tri-state. The VR restarts again when the sensed input voltage exceeds the  $V_{IN\_ON}$  threshold. The  $V_{IN}$  under-voltage lockout (UVLO) threshold is configurable via registers  $V_{IN\_ON}$  (35h) and  $V_{IN\_OFF}$  (36h) with 0.125V/LSB.

The VR shuts off if the input voltage rises above the  $V_{IN}$  over-voltage protection (OVP) threshold, set via register  $V_{IN\_OV\_FAULT\_LIMIT}$  (55h).  $V_{IN}$  OVP can be selected to trigger either latch-off or auto-retry mode.

## Input Over-Power Alert

The MP2975 supports two modes of input over-power alert (PSYS\_CRIT# and PWR\_IN\_ALT#). Bit[2] of MFR\_VR\_CONFIG3 (35h on page 1) indicates which mode the device uses.

**PWR\_IN\_ALT# mode:** When the calculated input power exceeds the preset input over-power threshold, the MP2975 asserts the PWR\_IN\_ALT# pin. The initial threshold is determined by register MFR\_PIN\_MAX (10h on page 2). The CPU updates the threshold via the SVID command.

**PSYS\_CRIT# mode:** There are two sub-modes (PSYS and VSYS), which are chosen by bit[3] of SVID\_PHSHD\_VR\_CONFIG (15h on page 2). If PSYS mode is selected, the MP2975 asserts the PSYS\_CRIT# pin when the voltage on the PSYS pin exceeds a preset threshold (the initial threshold is 1.6V). If VSYS mode is selected, the MP2975 asserts the PSYS\_CRIT# pin when the voltage on the PSYS pin drops below a preset threshold (the initial threshold is 0V). The CPU updates the threshold via the SVID command.

See the Register Map on page 43 for more details.

### Over-Current Protection (OCP)

Over-current protection (OCP) uses a dual-OCP mechanism with two types of thresholds. Each type is described below:

**OCP\_TOTAL:** OCP\_TOTAL is a time- and current-based threshold with a limit that is configurable via PMBus command MFR\_OCP\_TOTAL\_SET (5Fh). OCP\_TOTAL triggers when the sensed average output current exceeds the set threshold for a preset time (OCP blanking time). OCP\_TOTAL can be configured to no action, hiccup, latch-off, or retry 6 times mode via the PMBus.

In no action mode, the device switches until it trips other protections. The fault indication bit in registers STATUS\_IOUT (7Bh) and STATUS\_WORD (79h) are not set for no action mode.

In hiccup mode, the controller forces PWM signals to tri-state to disable the output, and attempts to restart after a 12.5ms protection delay.

In retry 6 times mode, the VR restarts a maximum of 6 times. If the fault is removed within 6 restarts, the VR resumes normal operation. If the fault continues after 6 retries, the VR shuts down until VDD33's power is cycled, EN is toggled, or a PMBus command is received.

In latch mode, the VR shuts down until the VDD33's power is cycled, EN is toggled, or PMBus is commanded off and on again.

The four protection modes above are available for OCP\_TOTAL, V<sub>OUT</sub> UVP, and V<sub>OUT</sub> OVP2.

**OCP\_PHASE:** OCP\_PHASE is a current-based limitation protection. The MP2975 monitors phase current cycle by cycle. If the phase current exceeds the OCP\_PHASE threshold during its PWM off time, PWM remains low to discharge the inductor current. If the load current continues to rise, the output voltage drops since the inductor current is limited. OCP\_PHASE is generally implemented along with UVP protection. The OCP\_PHASE threshold is set by register MFR\_OCP\_UCP\_PHASE\_SET (65h).

### Under-Voltage Protection (UVP)

The MP2975 provides under-voltage protection (UVP) and over-voltage protection (OVP) by monitoring the VDIFF voltage (V<sub>DIFF</sub>).

When V<sub>DIFF</sub> is below the UVP threshold for a given time (the UVP blanking time), the controller forces the PWMs to tri-state to disable the output power. Register MFR\_OVP\_UVP\_MODE (61h) determines the UVP protection mode. Similar to OCP\_TOTAL protection, UVP also provides no action, hiccup, retry 6 times, and latch off options.

The UVP threshold is configured with PMBus command MFR\_UVP\_SET (E6h). See the Register Map on page 43 for more details.

### Over-Voltage Protection (OVP)

The MP2975 uses dual over-voltage protection (OVP) approaches: OVP1 and OVP2. When any OVP is tripped, the MP2975 turns on all low-side MOSFETs to discharge COUT until V<sub>OUT</sub> falls below 150mV, and then triggers Hi-Z off.

OVP2 is the OVP type that is referred to VREF. It is tripped when the VDIFF voltage exceeds the OVP2 threshold for the set blanking time. The OVP2 threshold is configured via PMBus command MFR\_OV\_SET (E5h), bit[5:3].

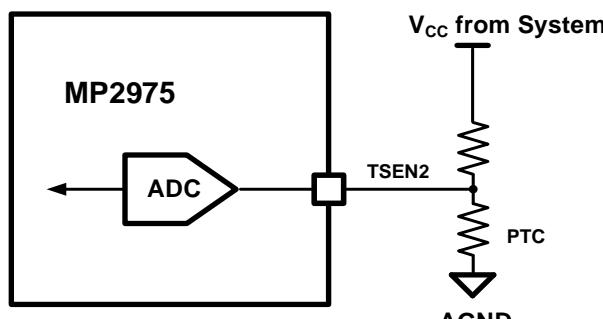
Similar to UVP, the MP2975 provides no action, hiccup, retry 6 times, and latch-off protection modes for OVP2.

The second type is OVP1, which is triggered when the VDIFF voltage exceeds the OVP1 threshold without triggering a delay time. The OVP1

threshold is determined by VOUT\_MAX (24h) and MFR\_OV\_SET (E5h) bit[2:0]. The OVP1 fault is always in latch mode.

### Over-Temperature (OT) Warning and Protection

The MP2975 monitors the junction temperature of the Intelli-Phase™ by connecting the VTEMP (TOUT) pin from the power stage to the controller (see Figure 11). Moreover, TSEN2 can achieve over-temperature protection (OTP) for any thermal area of the system by connecting to the thermistor (PTC or NTC) to the thermal area. Figure 17 shows an example of temperature-sensing via TSEN2.



**Figure 17: Temperature Sensing via TSEN2 with PTC**

If the sensed temperature via TSEN1 exceeds the OT\_WARN\_LIMIT (51h) register, the VRHOT# pin asserts and informs the processor to reduce power dissipation. When the sensed temperature falls below OT\_WARN\_LIMIT - 3°C, the VRHOT# pin de-asserts.

If the sensed temperature via TSEN1 exceeds the threshold set in register MFR OTP\_SET (4Fh), the VR initiates Hi-Z off. OTP can be programmed as either latch-off or auto-retry mode with PMBus command MFR OTP\_RESPONSE (50h).

If the sensed temperature via TSEN2 exceeds (or falls below) the preset threshold, the VR shuts down. There are analog and digital thresholds for TSEN2 OTP. The analog OTP is faster than digital OTP. See registers MFR\_TSEN2\_ANA\_FAULT (51h on page 1) and MFR\_TSEN2\_DGTL\_FAULT (55h on page 1) on page 130 for more details.

### Floating Line Detection

The MP2975 supports remote line-sensing (VOSEN, VORTN) floating detection at system initialization, after VDD33 starts up or EN starts up from low-power mode. The MP2975 latches down if a floating line is detected, and reports the fault via PMBus command STATUS\_VOUT (7Ah), bit[1]. Floating line detection can be enabled with MFR\_LINE\_FLOAT\_EN (66h on page 0).

### CS Fault and TEMP Fault

The MP2975 supports TEMP fault and CS fault to initiate fast protections when any phase's DrMOS experiences a fault. When the device detects that the voltage on TSEN1 exceeds 2.4V, the output is disabled for a TEMP fault. If any CS pin is pulled below 150mV, a CS fault shuts off the output.

Figure 18 shows a CS fault example when the MP2975 works with the Intelli-Phase product™, the MP86945A. The FAULT# signal of each MP86945A is tied to its own CS pin. When a fault occurs on any MP86945A, its FAULT# signal asserts and pulls CS low.

Figure 19 shows a TEMP fault example when the MP2975 works with the Intelli-Phase product™, the MP86956. When a fault occurs on any MP86956, its TOUT/FLT signal asserts and pulls TSEN1 high to 3.3V.

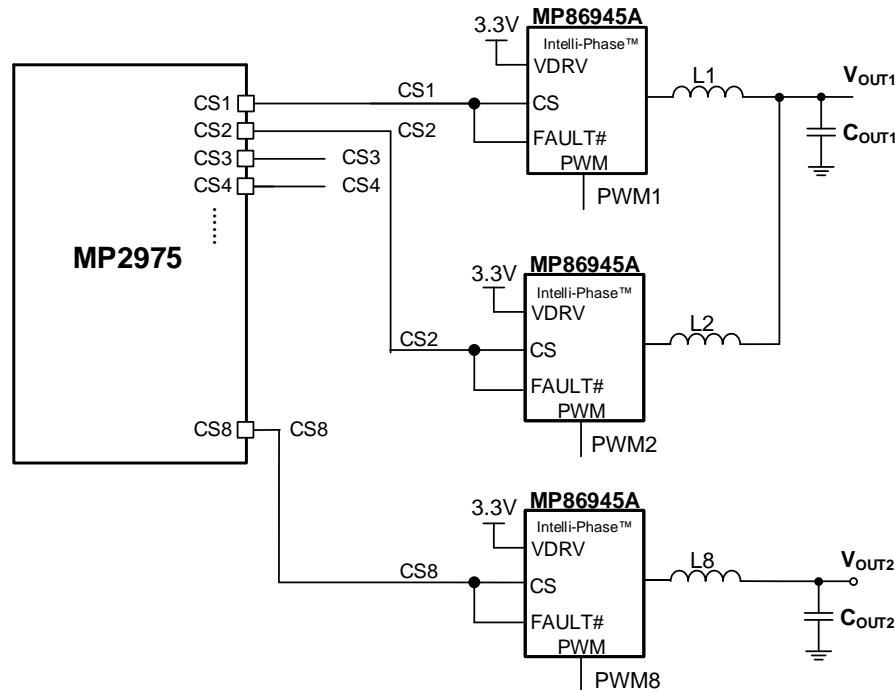


Figure 18: CS Fault for the MP86945A

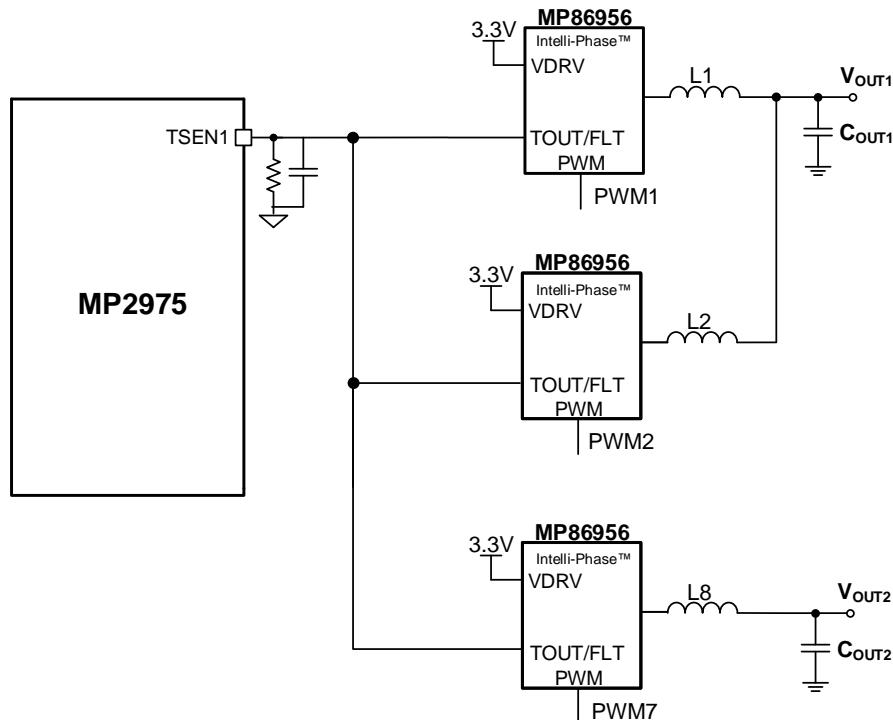


Figure 19: TEMP Fault for the MP86956

### Intelli-Phase™ Fault Detection

The MP2975 supports Intelli-Phase™ fault type detection. There are several types of Intelli-Phase™ faults:

- Over-current limit (OCL)
- Over-temperature (OT)
- Low-side MOSFET (LF-FET) short
- High-side MOSFET (HS-FET) short

MPS Intelli-Phase™ products support some or all the fault types above. Some Intelli-Phase™ products can report the fault type by setting the unique PWM impedance. Refer to the Intelli-Phase™ datasheet for additional details.

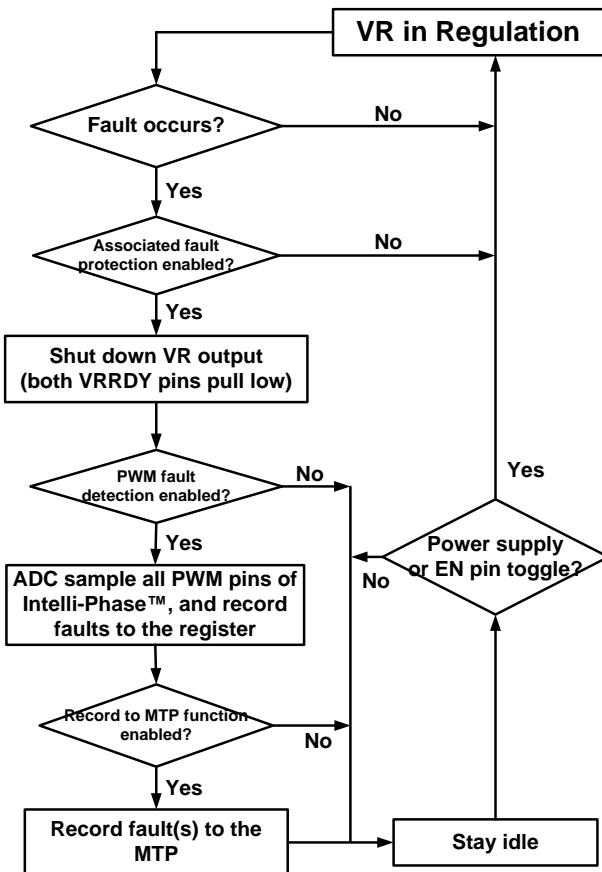
The MP2975 scans the PWM impedance after any of the following faults occurs:  $V_{IN}$  under-voltage lockout (UVLO),  $V_{IN}$  over-voltage protection (OVP), over-temperature protection (OTP),  $V_{OUT}$  under-voltage protection (UVP),  $V_{OUT}$  OVP, OCP\_TOTAL, TEMP fault, and CS fault.

Figure 20 shows the actions the MP2975 takes when there is a fault, described below:

1. Shut off the associated rail(s).
2. Start the Intelli-Phase™ fault type scan for related rail(s) by detecting the impedance on the PWM pins if this function is enabled via register MFR\_VR\_PROTECT\_SET (5Dh on page 0), bit[9].
3. Fault types are reported to PMBus registers A8h, A9h, and AAh on page 1.
4. Fault types are recorded to the MTP if the fault recording function is enabled via register MFR\_MTP\_PMBUS\_CTRL (C5h on page 0) bit[1]. The user can read back the fault types at the next start-up cycle. To provide fault storing into the MTP, the EN signal should be kept high for at least 20ms after a fault occurs.

### Catastrophic Fault Indication

The MP2975 can assert the CAT\_FLT pin to indicate any fault, including over-voltage protection (OVP), over-current protection (OCP), and over-temperature protection (OTP). The device can be configured to assert the CAT\_FLT pin to low or Hi-Z, and to choose which faults can assert it. See register MFR\_VR\_CONFIG4 (B0h on page 1) and MFR\_CAT\_FLT\_MASK (B3h on page 1) on page 166 for more details.



**Figure 20: Intelli-Phase™ Fault Detection Flowchart**

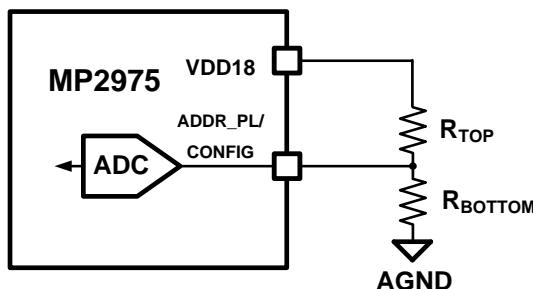
### Multi-Configuration

The MP2975 supports different load base configurations from the MTP during the MTP copy process. See the Start-Up section on page 26 for more details about MTP copying.

There are 6 configuration group registers saved in the MTP on page 2, which consist of key VR features. Each group has the same register number and definition. The Register Map on page 43 shows the definition of the first group registers (01h~1Eh on page 2).

Bit[10] of MFR\_VR\_CONFIG5 (C6h on page 1) is the enable bit for multi-configuration. If the function is enabled, the MP2975 loads specific configurations according to the voltage on the ADDR\_PL/CONFIG pin. If it is disabled, the MP2975 always loads group 1 as the initial setting.

Figure 21 shows the circuit design for multi-configuration applications via the ADDR\_PL/CONFIG pin.



**Figure 21: Recommended Circuit Design for Multi-Configuration**

Table 6 lists the required voltage range on the ADDR\_PL/CONFIG pin and recommended resistor divider values for specific configuration groups. (Groups 5 and 6 have two voltage ranges).

The ADDR\_PL/CONFIG pin can also be used to set the PMBus address when multi-configuration is enabled. The last column shows the corresponding PMBus address 4LSB settings. See the PMBus/I<sup>2</sup>C Address section on page 37 for more details about setting addresses.

**Table 6: Multi-Configuration Groups**

Config. Group	Registers on page 2	Voltage on Pin (V)	R <sub>TOP</sub> (kΩ) 1%	R <sub>BOTTOM</sub> (kΩ) 1%	PMBus Addr (4LSB)
1	01h~1Eh	0	-	0	0h
		0.031	3.32	0.059	1h
2	21h~3Eh	0.057	3.32	0.11	2h
		0.084	3.32	0.162	3h
3	41h~5Eh	0.116	3.32	0.226	4h
		0.156	3.32	0.316	5h
4	61h~7Eh	0.205	3.32	0.43	6h
		0.266	3.32	0.576	7h
5	81h~9Eh	0.340	3.32	0.768	8h
		0.430	3.32	1.05	9h
6	A1h~BEh	0.540	3.32	1.43	Ah
		0.675	3.32	2	Bh
5	81h~9Eh	0.844	3.32	2.94	Ch
		1.048	3.32	4.64	Dh
6	A1h~BEh	1.301	3.32	8.66	Eh
		1.500	3.32	16.5	Fh

### **Multi-Time Programmable (MTP) Operation**

The MP2975 provides multi-time programmable (MTP) to store custom configurations. A 4-digit, part number suffix is assigned for each application. The default configuration values can be preconfigured at the MPS factory. The user can also program the configuration by using a specific PMBus command via the I<sup>2</sup>C master or PMBus kit.

If multi-configuration is disabled, the STORE\_USER\_CODE (17h) command can be used to program registers in the MTP. Then all multi-configuration groups are configured with same setting. It requires 1s of waiting time for the process to store data to the MTP.

If multi-configuration is enabled, the STORE\_MULTI\_CODE (F3h) command can be sent at the beginning, and then multi-configuration

registers can be written to the MTP one by one. A 2ms waiting time is required for each address. Other registers that are not in multi-configuration groups can be programmed by the STORE\_NORMAL\_CODE (F1h) command.

Refer to the MP2975's MTP Program Guide (AN140) for more details.

The register values in the MTP include the selected group of multi-configuration to be read automatically during start-up or by the RESTORE\_USER\_CODE (18h) command via the PMBus. There is a 4ms waiting time for the process to restore data from the MTP.

Accessing the MTP can be easily accomplished with MPS GUI software. Refer to the MP2975's GUI application note for more details.

Use the PMBus command WRITE\_PROTECT (10h) ≠ 0x63 to enable MTP write protection.

The MTP can be written and erased about 1,000 times. When the MTP is write-protected, writing to the MTP actions is ineffective.

#### MTP CRC Fault

If the data from the MTP is invalid by checking the cyclic redundancy code (CRC) during system initialization, the system enters an MTP CRC fault state and disables the outputs of both rails to wait for the clear error command. The configuration from the MTP is ignored.

There are two methods to clear the MTP fault and reinitiate start-up:

1. Storing the correct configuration into the MTP.
2. Restarting with a VDD33 power recycle, or toggling EN in low-power mode.

### PMBus/PC Communication

#### General Description

Power management bus (PMBus) is an open-standard power management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device connects to the line, then generates the SCL signal and device address, and finally arranges the communication sequence. It is based on the I<sup>2</sup>C operation principles.

The MP2975 supports 100kHz, 400kHz, and 1MHz bus timing requirements. Timing and

electrical characteristics of the PMBus can be found in the Electrical Characteristics section on page 7, or in the PMBus Power Management Protocol Specification, part 1, revision 1.3, which is available at <http://PMBus.org>.

#### PMBus/I<sup>2</sup>C Address

To support multiple VR devices with the same PMBus/I<sup>2</sup>C interface, the MP2975 provides a 7-bit address code that ranges from 0x00 to 0x7F. The 3MSB bits can only be set by register MFR\_PMBUS\_ADDR\_IIN\_OFFSET (1Ah on page 2). The 4LSB bits can be set either by the register 1Ah on page 2 or by the ADDR\_PL pin. The selection bit is in MFR\_VR\_CONFIG5 (C6h on page 1), bit[11]. See the Register Map on page 43 for more details.

Address 00h is reserved as the all call address. Do not use it as the MP2975 unique device address.

The ADDR\_PL voltage can be configured by the resistive divider from VDD18 to AGND, and tapped to ADDR\_PL. Figure 22 shows the recommended connection. Table 7 shows the recommended resistor values for 4LSB addresses.

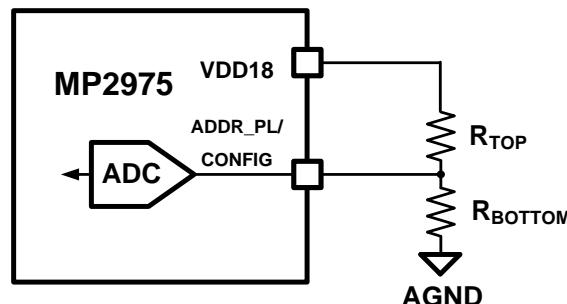


Figure 22: Recommend Circuit for PMBus Address Pin Set

**Table 7: Recommended Resistor Values for 4LSB Addresses**

Voltage on ADDR_PL(V)	R <sub>TOP</sub> (kΩ) 1%	R <sub>BOTTOM</sub> (kΩ) 1%	Addr_4LSB
0	-	0	0h
0.031	3.32	0.059	1h
0.057	3.32	0.11	2h
0.084	3.32	0.162	3h
0.116	3.32	0.226	4h
0.156	3.32	0.316	5h
0.205	3.32	0.43	6h
0.266	3.32	0.576	7h
0.340	3.32	0.768	8h
0.430	3.32	1.05	9h
0.540	3.32	1.43	Ah
0.675	3.32	2	Bh
0.844	3.32	2.94	Ch
1.048	3.32	4.64	Dh
1.301	3.32	8.66	Eh
1.500	3.32	16.5	Fh

## Data and Numerical Format

The MP2975 uses an internal, direct format to represent real-world values, such as voltage, current, power, temperature, and time.

For the voltage in VID format, the real-world voltage can be estimated with Equation (9):

$$V_{REAL}(V) = \begin{cases} \frac{(VID + 29) \times VID\_STEP(mV)}{1000} & \text{IMVP9\_10mV} \\ \frac{(VID + 49) \times VID\_STEP(mV)}{1000} & \text{others} \end{cases} \quad (9)$$

Where  $V_{REAL}$  is the real-world voltage, VID\_STEP is the VID voltage resolution (in 5mV or 10mV), and VID is the register value (in decimal).

IMVP9\_10mV is the Intel IMVP9 VID table with 10mV VID resolution. The Intel IMVP9 VID table can be enabled by bit[13] of 0Dh on page 2 for rail 1, and bit[12] of 1Dh on page 2 for rail 2.

All numbers with no suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in binary format are indicated by prefix “n'b”, where n is the binary count, and b is binary format. For example, 3'b000 means it is 3-bit binary data, and the binary data is 000.

The suffix “h” indicates hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates hexadecimal format, which is used for the value in the register. For example, 0x88 is a 1-byte number whose decimal value is 136.

## PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, listed below:

- Sending too little data
- Reading too little data
- The host sends too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the register STATUS\_CML (7Eh).

The CLEAR\_FAULTS (03h) command can be used to clear the fault record.

### PMBus/I<sup>2</sup>C Transmission Structure

The MP2975 supports five kinds of transmission structures with or without PEC:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

The MP2975 supports the packet error checking (PEC) mechanism, which can improve reliability and communication robustness. PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). The MP2975 only processes the

message if the PEC result is correct.

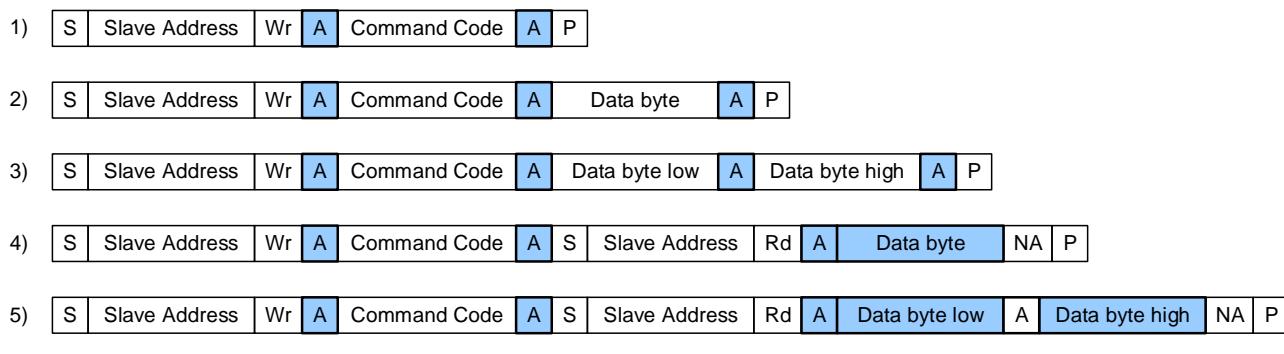
PEC is calculated in CRC-8 and represented by a polynomial, calculated with Equation (10).

$$C(x) = x^8 + x^2 + x^1 + 1 \quad (10)$$

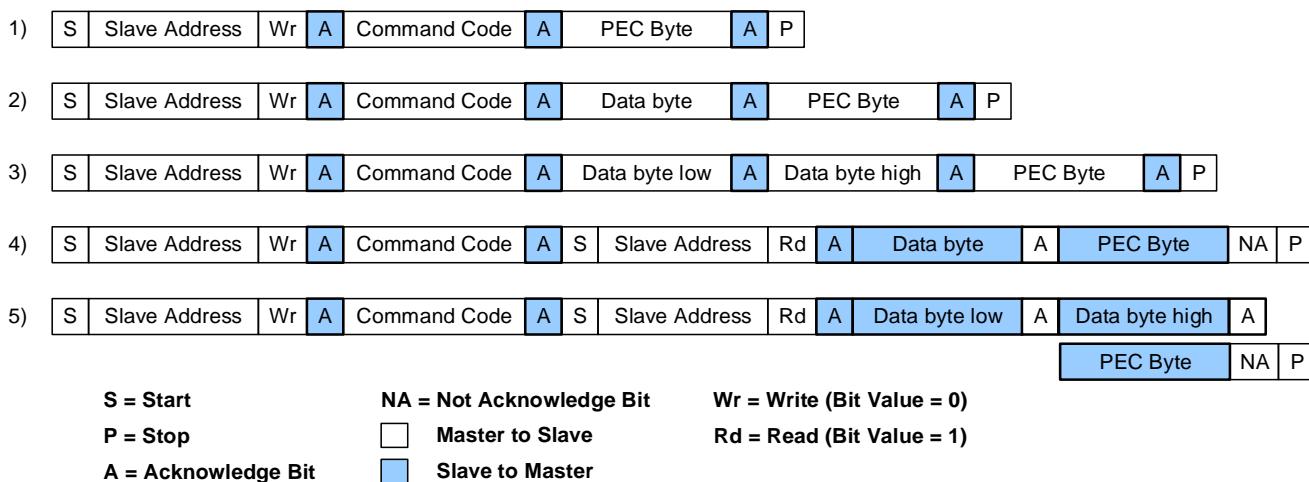
Figure 23 shows the supported PMBus/I<sup>2</sup>C transmission structure without PEC.

Figure 24 shows the supported PMBus/I<sup>2</sup>C transmission structure with PEC.

To read or write the registers of the MP2975, the PMBus/I<sup>2</sup>C command must be compliant with the byte number of the register in the table of register map. Refer to AN140 for additional details.



**Figure 23: Supported PMBus/I<sup>2</sup>C Transmission Structure without PEC**



**Figure 24: Supported PMBus/I<sup>2</sup>C Transmission Structure with PEC**

### PMBus Reporting and Status Monitoring

The MP2975 supports real-time monitoring for the VR operation parameters and statuses with the PMBus interface.

Table 8 lists the monitored parameters.

**Table 8: PMBus-Monitored Parameters**

Parameter	PMBus	Register
Input voltage	0.25V/LSB	88h
Input current	0.25A/LSB	89h
Output voltage	VID or 1mV/LSB	8Bh
Output current	1A/LSB	8Ch
Temperature	1/LSB	8Dh
Peak output current	0.25A/LSB	90h
Peak output power	0.25W/LSB	91h
Output power	1W/LSB	96h
Input power	1W/LSB	97h
Phase current	Refer to register map 82h~87h	
Power good	✓	79h
V <sub>OUT</sub> OV fault	✓	7Ah
V <sub>OUT</sub> UV fault	✓	7Ah
OC fault	✓	7Bh
V <sub>IN</sub> UVLO fault	✓	7Ch
V <sub>IN</sub> OVP fault	✓	7Ch
OT fault	✓	7Dh
PMBus Fault	✓	7Eh
MTP fault	✓	7Eh
VID max/min extend warning	✓	7Ah
V <sub>in</sub> uv warning	✓	7Ch
Input over-power warning	✓	7Ch
OT warning	✓	7Dh
PMBus PEC Error	✓	7Eh
MTP CRC error	✓	7Eh

### PMBus Write/Read (W/R) Limitation

The MP2975 supports PMBus write (W) protection or both read and write (R/W) protection by writing a non-zero 16-bit code to MFR\_PWD\_USER (02h at page 1) that is stored to the MTP to enable the function. After the device restarts, the PMBus registers have limited access until the user enters the correct 16-bit password via PMBus command PWD\_CHECK\_CMD (F8h on page 0).

The PMBUS COMMAND LIST in this document shows which registers support write (W) and/or read/write (R/W) protection mode in columns “W PRT” and “R/W PRT.” Register MFR\_MTP\_PMBUS\_CTRL (C5h on page 0), bit[6] and bit[7] are the enable bits for these two modes, respectively. See the Register Map on page 43 for more details.

## PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1)

The MP297x (MP2972, MP2975, MP2976, and MP2978) family is a collection of dual-loop, digital multi-phase controllers that provides power for the CPU core and memory of VR13, VR13.HC, and AVSBus. It works with MPS and multiple vendors' DrMOS products to provide a multi-phase VR total solution with minimal external components.

The MP297x family provides on-chip NVM to store and restore device configurations. Device configurations and fault parameters are easy to configure and monitor via the PMBus/I<sup>2</sup>C interface. These devices can monitor and report output current through the current-sense output from DrMOS products.

The MP2972 provides 12 PWMs, and can be configured up to 12-phase operation for rail 1 and up to 6-phase operation for rail 2.

The MP2975 provides 8 PWMs, and can be configured up to 8-phase operation for rail 1 and up to 4-phase operation for rail 2.

The MP2976 provides 2 PWMs, and can be configured up to 1-phase operation for rail 1 and up to 1-phase operation for rail 2.

The MP2978 provides 5 PWMs, and can be configured up to 4-phase operation for rail 1 and up to 1-phase operation for rail 2.

Table 9 shows the total PWM count and maximum phase count of rail 1 and rail 2 for each part.

**Table 9: PWM Count and Phase Count**

Part Number	Total PWM Count	Rail 1 Maximum Phase Count	Rail 2 Maximum Phase Count
MP2972	12	12	6
MP2975	8	8	4
MP2976	2	1	1
MP2978	5	4	1

The register description in this document is based on the MP2972. “MP297x” in this document refers to the MP2972, MP2975, MP2976, or MP2978. For those registers with phase numbers that the MP2975, MP2976, or MP2978 cannot support, the register value is ineffective and does not affect applications on these controllers.

Registers that are related to phase numbers are listed below:

1. Auto phase-shedding, current-level setting registers on page 1: 06h, 07h, 08h, 09h, 0Ah, 0Bh, and 0Ch.

For example, the MFR\_APS\_LEVEL\_1011P (0Ch on page 1) command sets rail 1's auto phase-shedding current threshold to 10-phase or 11-phase, or rail 2's auto phase-shedding current threshold to 1-phase. The MP2975, MP2976, and MP2978 do not support 10-phase, 11-phase, or 12-phase operation on rail 1, so the setting for rail 1 is ineffective for these three parts. The register setting for rail 2 is effective if rail 2 is above 1-phase operation.

**Table 10: MFR\_APS\_LEVEL\_1011P bit description**

Bits	Bit Name	Description
15:8	DROP_LEVEL_11P_R1 DROP_LEVEL_DCM_R2	Sets the rail 1 auto phase-shedding current threshold to 11-phase CCM, or the rail 2 auto phase-shedding current threshold to 1-phase DCM. 1A/LSB.
7:0	DROP_LEVEL_10P_R1 DROP_LEVEL_1P_R2	Sets the rail 1 auto phase-shedding current threshold to 10-phase CCM, or the rail 2 auto phase-shedding current threshold to 1-phase CCM. 1A/LSB.

## PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (*continued*)

2. The frequency limit setting registers (0Eh, 0Fh, 11h, 12h, 13h, and 14h) are all on page 1.

For example, the MFR\_FS\_LIMIT\_56P (11h at page 0) command sets the FS\_LIMIT at 5-phase and 6-phase operation to detect fast load insertion and exit phase-shedding. It is for rail 1 only. The MP2976 and MP2978 do not support 5-phase or 6-phase phase operation, so the register setting is ineffective for them.

**Table 11: MFR\_FS\_LIMIT\_56P Bit Description**

Bits	Bit Name	Description
15:8	FS_LIMIT_6P_R1	Sets the exit phase-shedding PWM interval time for rail 1 6-phase operation. Figure 5(b) shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_5P_R1	Sets the exit phase-shedding PWM interval time for rail 1 5-phase operation. Figure 5(b) shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

3. Slope voltage trim setting registers on page 1: 1Ch, 1Dh, 1Eh, and 1Fh.
4. Slope compensation setting registers on page 1: 38h, 39h, 3Ah, 3Bh, 3Ch, 3Dh, 3Eh, 3Fh, 40h, 41h, 42h, 43h, 44h, 45h, 46h, 47h, 48h, 49h, 4Ah, 4Bh, 4Ch, 4Eh, and 4Fh.
5. Blanking time setting registers on page 0 and page 1: 69h, 6Ah, and 72h.
6. Read-only CS voltage report registers on page 0: 82h, 83h, 84h.
7. Read-only CS voltage report registers on page 0 and page 1: 85h, 86h, and 87h.
8. Read-only fault report registers on page 0: A6h, A8h, A9h, and AAh.

**PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (continued)**

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT	R/W PRT
00h	PAGE	R/W	1	✓	✓		
01h	OPERATION	R/W	1	✓	✓	✓	✓
02h	MFR_PWD_USER	R/W	2		✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	✓	✓	
04h	MFR_VR_CONFIG6	R/W	2		✓	✓	✓
06h	MFRAPS_LEVEL_1P	R/W	2		✓	✓	✓
07h	MFRAPS_LEVEL_23P	R/W	2		✓	✓	✓
08h	MFRAPS_LEVEL_45P	R/W	2		✓	✓	✓
09h	MFRAPS_HYS_R1	R/W	2		✓	✓	✓
0Ah	MFRAPS_LEVEL_67P	R/W	2		✓	✓	✓
0Bh	MFRAPS_LEVEL_89P	R/W	2		✓	✓	✓
0Ch	MFRAPS_LEVEL_1011P	R/W	2		✓	✓	✓
0Dh	MFRAPS_HYS_R2	R/W	2		✓	✓	✓
0Eh	MFR_FS_LIMIT_12P	R/W	2		✓	✓	✓
0Fh	MFR_FS_LIMIT_34P	R/W	2		✓	✓	✓
10h	MTP_WRITE_PROTECT	R/W	1	✓		✓	✓
	MFR_PROTECT_DELAY_TIME				✓	✓	✓
11h	MFR_FS_LIMIT_56P	R/W	2		✓	✓	✓
12h	MFR_FS_LIMIT_78P	R/W	2		✓	✓	✓
13h	MFR_FS_LIMIT_910P	R/W	2		✓	✓	✓
14h	MFR_FS_LIMIT_1112P	R/W	2		✓	✓	✓
17h	STORE_USER_CODE	Send	0	✓	✓	✓	✓
18h	RESTORE_USER_CODE	Send	0	✓	✓	✓	
19h	DEVICE_CAPABILITY	R	1	✓			
1Ah	MFR_SLOPE_TRIM1	R/W	2		✓	✓	✓
1Bh	SMBALERT_MASK	R/W	2	✓		✓	✓
	MFR_PS34_EXIT_LAT				✓	✓	✓
1Ch	MFR_SLOPE_TRIM2	R/W	2		✓	✓	✓
1Dh	MFR_SLOPE_TRIM3	R/W	2		✓	✓	✓
1Eh	MFR_SLOPE_TRIM4	R/W	2		✓	✓	✓
1Fh	MFR_SLOPE_TRIM5	R/W	2		✓	✓	✓
20h	VOUT_MODE	R	1	✓			
21h	VOUT_COMMAND	R/W	2	✓	✓	✓	✓
22h	MFR_IDROOP_OFFSET	R/W	2	✓	✓	✓	✓
24h	VOUT_MAX	R/W	2	✓	✓	✓	✓
25h	VOUT_MARGIN_HIGH	R/W	2	✓	✓	✓	✓
26h	VOUT_MARGIN_LOW	R/W	2	✓	✓	✓	✓
27h	VOUT_TRANSITION_RATE	R/W	2	✓	✓	✓	✓
29h	VOUT_SENSE_SET	R/W	2	✓	✓	✓	✓
2Bh	VOUT_MIN	R/W	2	✓	✓	✓	✓
35h	VIN_ON	R/W	2	✓		✓	✓
	MFR_VR_CONFIG3				✓	✓	✓

**PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (continued)**

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT	R/W PRT
36h	VIN_OFF	R/W	2	✓		✓	✓
	MFR_VIN_SCALE_OFFSET				✓	✓	✓
38h	MFR_SLOPE_SR_1P	R/W	2		✓	✓	✓
39h	MFR_SLOPE_CNT_1P	R/W	2		✓	✓	✓
3Ah	MFR_SLOPE_SR_2P	R/W	2		✓	✓	✓
3Bh	MFR_SLOPE_CNT_2P	R/W	2		✓	✓	✓
3Ch	MFR_CONFIG_REV_MPS	R/W	2	✓		✓	✓
	MFR_SLOPE_SR_3P	R/W	2		✓	✓	✓
3Dh	MFR_SLOPE_CNT_3P	R/W	2		✓	✓	✓
3Eh	MFR_SLOPE_SR_4P	R/W	2		✓	✓	✓
3Fh	MFR_SLOPE_CNT_4P	R/W	2		✓	✓	✓
40h	MFR_SLOPE_SR_5P	R/W	2		✓	✓	✓
41h	MFR_SLOPE_CNT_5P	R/W	2		✓	✓	✓
42h	MFR_SLOPE_SR_6P	R/W	2		✓	✓	✓
43h	MFR_SLOPE_CNT_6P	R/W	2		✓	✓	✓
44h	MFR_SLOPE_SR_7P	R/W	2		✓	✓	✓
45h	MFR_SLOPE_CNT_7P	R/W	2		✓	✓	✓
46h	MFR_SLOPE_SR_8P	R/W	2		✓	✓	✓
47h	MFR_SLOPE_CNT_8P	R/W	2		✓	✓	✓
48h	MFR_SLOPE_SR_9P	R/W	2		✓	✓	✓
49h	MFR_SLOPE_CNT_9P	R/W	2		✓	✓	✓
4Ah	MFR_SLOPE_SR_10P	R/W	2		✓	✓	✓
4Bh	MFR_SLOPE_CNT_10P	R/W	2		✓	✓	✓
4Ch	MFR_SLOPE_SR_11P	R/W	2		✓	✓	✓
4Dh	MFR_SLOPE_CNT_11P	R/W	2		✓	✓	✓
4Eh	MFR_SLOPE_SR_12P	R/W	2		✓	✓	✓
4Fh	MFR_OTP_SET	R/W	2	✓		✓	✓
	MFR_SLOPE_CNT_12P				✓	✓	✓
50h	MFR_OTP_RESPONSE	R/W	1	✓		✓	✓
	MFR_TEMP_CAL		2		✓	✓	✓
51h	OT_WARN_LIMIT	R/W	2	✓		✓	✓
	MFR_TSEN2_ANA_FAULT				✓	✓	✓
52h	MFR_IDROOP_LIMIT_SET	R/W	2	✓	✓	✓	✓
53h	MFR_IMON_CONFIG	R/W	2	✓	✓	✓	✓
54h	IOUT_CAL_OFFSET	R/W	2	✓	✓	✓	✓
55h	VIN_OV_FAULT_LIMIT	R/W	2	✓		✓	✓
	MFR_TSEN2_DGTL_FAULT				✓	✓	✓
56h	MFR_APS_DECAY_ADV	R/W	2	✓	✓	✓	✓
57h	MFR_APS_CTRL	R/W	2	✓	✓	✓	✓
58h	MFR_APS_FS_CTRL	R/W	2	✓	✓	✓	✓
59h	MFR_DC_LOOP_CTRL	R/W	2	✓	✓	✓	✓
5Ah	MFR_CB_LOOP_CTRL	R/W	2	✓	✓	✓	✓
5Bh	MFR_FS_LOOP_CTRL	R/W	2	✓	✓	✓	✓
5Ch	MFR_FS	R/W	2	✓	✓	✓	✓

**PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (continued)**

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT	R/W PRT
5Dh	MFR_VR_PROTECT_SET	R/W	2	✓	✓	✓	✓
5Eh	MFR_VR_CONFIG2	R/W	2	✓	✓	✓	✓
5Fh	MFR_OCP_TOTAL_SET	R/W	2	✓	✓	✓	✓
60h	TON_DELAY	R/W	2	✓	✓	✓	✓
61h	MFR_OVP_UVP_MODE	R/W	2	✓	✓	✓	✓
62h	MFR_CUR_GAIN	R/W	2	✓	✓	✓	✓
63h	MFR_CUR_OFFSET	R/W	2	✓	✓	✓	✓
64h	TOFF_DELAY	R/W	2	✓	✓	✓	✓
65h	MFR_OCP_UCP_PHASE_SET	R/W	2	✓	✓	✓	✓
66h	MFR_LINE_FLOAT_EN	R/W	2	✓		✓	✓
	MFR_PSYS_ANA_FAULT				✓	✓	✓
67h	MFR_PSYS_DGTL_FAULT	R/W	2		✓	✓	✓
68h	MFR_VR_CONFIG1	R/W	2	✓	✓	✓	✓
69h	MFR_BLANK_TIME2	R/W	2	✓	✓	✓	✓
6Ah	MFR_BLANK_TIME3	R/W	2	✓	✓	✓	✓
6Bh	MFR_DROOP_CMPN1	R/W	2	✓	✓	✓	✓
6Ch	MFR_DROOP_CMPN2	R/W	2	✓	✓	✓	✓
6Dh	MFR_PGOOD_SET	R/W	2	✓	✓	✓	✓
6Eh	POWER_GOOD_ON	R/W	2	✓	✓	✓	✓
6Fh	POWER_GOOD_OFF	R/W	2	✓	✓	✓	✓
72h	MFR_BLANK_TIME1	R/W	2	✓	✓	✓	✓
73h	MFR_OSR_SET	R/W	2	✓	✓	✓	✓
74h	MFR_PWM_MIN_TIME1	R/W	2	✓	✓	✓	✓
75h	MFR_PWM_MIN_TIME2	R/W	2	✓	✓	✓	✓
76h	MFR_SLOPE_ANA_CTRL	R/W	2	✓	✓	✓	✓
78h	STATUS_BYTE	R	1	✓	✓		
79h	STATUS_WORD	R	2	✓	✓		
7Ah	STATUS_VOUT	R	1	✓	✓		
7Bh	STATUS_IOUT	R	1	✓	✓		
7Ch	STATUS_INPUT	R	1	✓			
7Dh	STATUS_TEMPERATURE	R	1	✓			
7Eh	STATUS_CML	R	1	✓			
80h	DRMOS_FAULT	R	1	✓			
82h	READ_CS1_2	R	2	✓			
83h	READ_CS3_4	R	2	✓			
84h	READ_CS5_6	R	2	✓			
85h	READ_CS7_8	R	2	✓			
	READ_CS1_2_L2				✓		
86h	READ_CS9_10	R	2	✓			
	READ_CS3_4_L2				✓		
87h	READ_CS11_12	R	2	✓			
	READ_CS5_6_L2				✓		
88h	READ_VIN	R	2	✓			

**PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (continued)**

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT	R/W PRT
89h	READ_IIN	R	2	✓			
8Bh	READ_VOUT	R	2	✓	✓		
8Ch	READ_IOUT	R	2	✓	✓		
8Dh	READ_TEMPERATURE	R	2	✓			
90h	READ_IOUT_PK	R	2	✓	✓		
91h	READ_POUT_PK	R	2	✓	✓		
94h	READ_TON	R	2	✓	✓		
95h	READ_TS	R	2	✓	✓		
96h	READ_POUT	R	2	✓	✓		
97h	READ_PIN	R	2	✓			
98h	PMBUS_REVISION	R	1	✓			
99h	SVID_VENDOR_ID	R/W	2	✓		✓	
	MFR_CS_OFFSET1				✓	✓	
9Ah	SVID_PRODUCT_ID	R/W	2	✓		✓	
	MFR_CS_OFFSET2				✓	✓	
9Bh	PRODUCT_REV_USER	R/W	2	✓		✓	
	MFR_CS_OFFSET3				✓	✓	
9Dh	CONFIG_ID	R/W	2	✓		✓	
	MFR_CS_OFFSET4				✓	✓	
9Eh	SVID_LOT_CODE_PROTOCOL_ID	R/W	2	✓		✓	
	MFR_AVSBUS_CONFIG				✓	✓	
9Fh	SVID_PROTOCOL_ID2	R/W	2	✓		✓	
	MFR_CUR_OFFSET_SVID				✓	✓	
A0h	READ_SVID_AVSBUS_ADDR	R	2	✓			
A3h	READ_PIN_ALERT_THRESHOLD	R	2	✓			
A4h	READ_VOUT_MIN	R	2	✓	✓		
A5h	READ_VOUT_MAX	R	2	✓	✓		
A6h	MFR_FAULTS1	R	2		✓		
A7h	MFR_FAULTS2	R	2		✓		
A8h	MFR_FAULTS3	R	2		✓		
A9h	MFR_FAULTS4	R	2		✓		
AAh	MFR_FAULTS5	R	2		✓		
ABh	MFR_CRC_NORMAL_CODE	R	2		✓		
ADh	MFR_CRC_MULTI_CONFIG	R	2		✓		
B0h	MFR_VR_CONFIG4	R/W	2		✓	✓	✓
B1h	MFR_PIN_OFFSET	R/W	2		✓	✓	✓
B2h	RESERVED	R/W	2		✓	✓	✓
B3h	MFR_CAT_FLT_MASK	R/W	2		✓	✓	✓
B4h	MFR_PSYS_LEVEL	R/W	2		✓	✓	✓
B5h	MFR_PIN_OFFSET_TUNE2	R/W	2		✓	✓	✓
B6h	MFR_PIN_OFFSET_TUNE3	R/W	2		✓	✓	✓
B7h	TRIM_ZCD	R/W	2	✓		✓	✓
	MFR_PIN_OFFSET_TUNE4				✓	✓	✓
B8h	MFR_SLOPE_SR_CNT_DCM_R1	R/W	2		✓	✓	✓
B9h	MFR_SLOPE_SR_CNT_DCM_R2	R/W	2		✓	✓	✓

**PMBUS COMMANDS/REGISTERS (PAGE 0 AND PAGE 1) (continued)**

Command Code	Command Name	Type	Bytes	Page 0	Page 1	W PRT	W/R PRT
BAh	PVID_VID12_R1	R/W	2		✓	✓	✓
BBh	PVID_VID34_R1	R/W	2		✓	✓	✓
BCh	PVID_VID56_R1	R/W	2		✓	✓	✓
BDh	PVID_VID78_R1	R/W	2		✓	✓	✓
BEh	PVID_VID12_R2	R/W	2		✓	✓	✓
BFh	MFR_PRODUCT_SEL	R/W	2	✓		✓	✓
	PVID_VID34_R2	R/W	2		✓	✓	✓
C0h	PVID_VID56_R2	R/W	2		✓	✓	✓
C1h	PVID_VID78_R2	R/W	2		✓	✓	✓
C2h	SVID_VOUT_MAX	R/W	2	✓	✓	✓	✓
C3h	SVID_VR_TVRRDY_TOLERANCE1	R/W	2	✓		✓	✓
	SVID_VR_TOLERANCE_PS4_DLY				✓	✓	✓
C4h	SVID_TEMP_OFFSET	R/W	2		✓	✓	✓
C5h	MFR_MTP_PMBUS_CTRL	R/W	2	✓		✓	✓
C6h	MFR_VR_CONFIG5	R/W	2		✓	✓	✓
D0h	PWD_LOCK_TOG	Send	0	✓	✓	✓	✓
E1h	SVID_LAST_CMD_DATA	R	2	✓	✓		
E2h	SVID_SECOND_LAST_CMD_DATA	R	2	✓	✓		
E5h	MFR_OVP_TH_SET	R/W	1	✓	✓	✓	
E6h	MFR_UVP_SET	R/W	1	✓	✓	✓	
F0h	MFR_CAT_PWR_IN_FLT	R/W	2	✓		✓	
F1h	STORE_NORMAL_CODE	Send	0	✓	✓	✓	✓
F2h	RESTORE_NORMAL_CODE	Send	0	✓	✓	✓	
F8h	PWD_CHECK_CMD	W	2	✓			
FDh	CLEAR_CATFAULTS	Send	0	✓	✓	✓	
FEh	CLEAR_STOREFAULTS	Send	0	✓	✓	✓	✓
FFh	CLEAR_MTPFAULTS	Send	0	✓	✓	✓	

## PMBUS COMMANDS/REGISTERS (PAGE 2)

Command Code	Command Name	Type	Bytes	Page 2	W PRT	W/R PRT
00h	PAGE	R/W	1	✓	✓	✓
01h	MFR_HC_SLEW_RATE_SET_R1	R/W	2	✓	✓	✓
02h	MFR_ICC_MAX_R1	R/W	2	✓	✓	✓
03h	SVID_CAPABILITY_DC_LL_R1	R/W	2	✓	✓	✓
04h	SVID_SR_FAST_SR_SLOW_R1	R/W	2	✓	✓	✓
05h	MFR_ADDR_SVID_AVSBUS	R/W	2	✓	✓	✓
06h	MFR_IDROOP_CTRL1_R1	R/W	2	✓	✓	✓
07h	MFR_IDROOP_CTRL2_R1	R/W	2	✓	✓	✓
08h	IOUT_RPT_GAIN_SVID_AV_S_R1	R/W	2	✓	✓	✓
09h	MFR_IIN_CAL_IMON_OFFSET_R1	R/W	2	✓	✓	✓
0Ah	IOUT_RPT_GAIN_HC_R1	R/W	2	✓	✓	✓
0Bh	IOUT_CAL_GAIN_PMBUS_R1	R/W	2	✓	✓	✓
0Ch	MFR_IMON_DGTL_ANA_GAIN_R1	R/W	2	✓	✓	✓
0Dh	MFR_VR_MULTI_CONFIG_R1	R/W	2	✓	✓	✓
0Eh	SVID_VR_CONFIG	R/W	2	✓	✓	✓
0Fh	MFR_IIN_GAIN	R/W	2	✓	✓	✓
10h	MFR_PIN_MAX	R/W	2	✓	✓	✓
11h	MFR_SLEW_RATE_SET_R2	R/W	2	✓	✓	✓
12h	MFR_ICC_MAX_R2	R/W	2	✓	✓	✓
13h	SVID_CAPABILITY_DC_LL_R2	R/W	2	✓	✓	✓
14h	SVID_SR_FAST_SR_SLOW_R2	R/W	2	✓	✓	✓
15h	SVID_PHSHEd_VR_CONFIG	R/W	2	✓	✓	✓
16h	MFR_IDROOP_CTRL1_R2	R/W	2	✓	✓	✓
17h	MFR_IDROOP_CTRL2_R2	R/W	2	✓	✓	✓
18h	IOUT_RPT_GAIN_SVID_AV_S_R2	R/W	2	✓	✓	✓
19h	MFR_IMON_OFFSET_R2	R/W	2	✓	✓	✓
1Ah	MFR_PMBUS_ADDR_IIN_OFFSET	R/W	2	✓	✓	✓
1Bh	IOUT_CAL_GAIN_PMBUS_R2	R/W	2	✓	✓	✓
1Ch	MFR_IMON_DGTL_ANA_GAIN_R2	R/W	2	✓	✓	✓
1Dh	MFR_VR_MULTI_CONFIG_R2	R/W	2	✓	✓	✓
1Eh	VOUT_OFFSET	R/W	2	✓	✓	✓
F1h	STORE_NORMAL_CODE	Send	0	✓	✓	✓
F2h	RESTORE_NORMAL_CODE	Send	0	✓	✓	✓
F3H	STORE_MULTI_CODE	Send	0	✓	✓	✓

## REGISTER MAP (PAGE 0)

### PAGE (00h)

This command on page 0 provides the ability to configure, control, and monitor all registers (including the MTP and test mode) through only one physical address.

Command	PAGE									
Format	Unsigned binary									
Bit	7	6	5	4	3	2	1	0		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Function	X	X	Page							

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	PAGE	<p>Selection bit for the registers page.</p> <p>0x00: Page 0, all PMBus commands address operating registers on page 0      0x01: Page 1, all PMBus commands address operating registers on page 1      0x02: Page 2, all PMBus commands address operating multi-configuration registers on page 2      0x03: Page 3, all PMBus commands address the test mode registers.      0x28: Page 28, all PMBus commands address the MTP registers that are mapped to the operating registers on page 0      0x29: Page 29, all PMBus commands address the MTP registers that are mapped to the operating registers on page 1      0x2A: Page 2A, all PMBus commands address the MTP registers that are mapped to the operating multi-configuration registers on page 2      Others: Ineffective input</p> <p>Note: MTP_BYTWR_EN, bit[5] of MFR_MTP_CTRL (C5h on page 0), determines whether pages 28, 29, and 2A are accessible or not.      MTP_BYTWR_EN = 0: Page 28/29/2A is not accessible      MTP_BYTWR_EN = 1: Page 28/29/2A is accessible</p>

### OPERATION (01h)

This command on page 0 turns the rail 1 output on/off in conjunction with input from the EN pin, sets the output voltage to the upper or lower margin voltages, and selects the AVSBus mode. Rail 1 remains in the set OPERATION command state until it receives a subsequent OPERATION command, or EN alters states and changes rail 1 to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OPERATION							

Bits	Bit Name	Description
7:0	OPERATION	<p>Operation mode selection bit.</p> <p>8'b 00xx xxxx: Hi-Z off      8'b 01xx xxxx: Soft-off      8'b 1000 xxxx: Normal on      8'b 1001 xxxx: Margin low      8'b 1010 xxxx: Margin high      8'b 1011 xxxx: AVSBus mode      Others: Unused. "x" means not applicable</p>

### CLEAR\_FAULTS (03h)

This command on page 0 clears any fault bit in all status registers: STATUS\_BYTE (78h), STATUS\_WORD (79h), STATUS\_VOUT (7Ah), STATUS\_IOUT (7Bh), STATUS\_INPUT (7Ch), STATUS\_TEMPERATURE (7Dh), STATUS\_CML (7Eh), and DRMOS\_FAULT (80h).

This command is write-only. There is no data byte for this command.

### MTP\_WRITE\_PROTECT (10h)

This command on page 0 enables MTP write protection.

Command	MTP_WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MTP_WP							

Bits	Bit Name	Description
7:0	MTP_WP	Enables MTP write protection. 0x63: Disable MTP write protection Others: Enable MTP write protection

### STORE\_USER\_CODE (17h)

This command on page 0 instructs the PMBus device to copy the page 0, page 1, and page 2 contents of the operating memory to their matching locations in the MTP (except the internal trim registers). In the copying process, the device calculates two sets of CRC codes for all saved bits, and saves the corresponding CRC results in the MTP. Two sets of CRC codes include one set for user configurations on page 0 and page 1, and one set for multi-configuration on page 2. The CRC codes ensure the data being copied from the MTP is valid at the next power-up, or when the actions are restored.

This command is write-only. There is no data byte for this command.

### RESTORE\_USER\_CODE (18h)

This command on page 0 instructs the PMBus device to copy the page 0, page 1, and page 2 contents from the MTP, and overwrite the matching locations in the operating memory. Trim registers are not overwritten by the RESTORE\_USER\_CODE command. During this process, the device calculates the CRC for all restored bits. If the calculated CRC does not match the CRC values saved in the MTP, the device reports a CRC error via bit[4] of register STATUS\_CML (7Eh). The CRC error protection action is enabled by bit[0] and bit[9] of MFR\_MTP\_CTRL (C5h on page 0). After power-on reset (POR), the device triggers memory copying from the MTP.

The RESTORE\_USER\_CODE command cannot be sent while the device is outputting power, and will be ignored. This command is write-only. There is no data byte for this command.

### DEVICE\_CAPABILITY (19h)

This command on page 0 provides 1 byte to return key PMBus features that the MP297x can support.

Command	DEVICE_CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	1 1 0 1 0 1 0 0							

Bits	Bit Name	Description
7	PACKET_ERROR_CHECKING	1'b1: Packet error checking (PEC) supported
6:5	MAXIMUM_BUS_SPEED	2'b10: PMBus/I <sup>2</sup> C maximum bus speed is 1MHz
4	SMBALERT#	1'b1: The MP297x has an ALT_P# pin, and supports the SMBus alert response protocol
3	NUMERIC_FORMAT	1'b0: Numeric data format is LINEAR 11, ULNEAR 16, SLINEAR 16, and in direct format
2	AVSBUS_SUPPORT	1'b1: AVSBus supported
1:0	RESERVED	RESERVED. Always returns 2'b00.

**SMBALERT\_MASK (1Bh)**

This command on page 0 masks the faults that will not assert ALT\_P#. It is effective only when STANDBY\_ALTP\_SEL (bit[0] of register MFR\_VR\_CONFIG4 (B0h on page 1)) is 0.

Command	SMBALERT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X														X	

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	OVP	1'b0: When VOUT over-voltage protection (OVP) occurs, ALT_P# will not assert 1'b1: No mask
13	UVP	1'b0: When VOUT under-voltage protection (UVP) occurs, ALT_P# will not assert 1'b1: No mask
12	VOUT_MAX_MIN_WARNING	1'b0: When VID is set to exceed VOUT_MAX, or it is set below the VOUT_MIN threshold, ALT_P# will not assert 1'b1: No mask
11	OCP	1'b0: When OCP_TOTAL protection occurs, ALT_P# will not assert 1'b1: No mask
10	OC_UV	1'b0: When over-current (OC) and VOUT under-voltage (UV) faults occur simultaneously, the ALT_P# will not assert 1'b1: No mask
9	INVALID_CMD	1'b0: When the PMBus receives an invalid command, ALT_P# will not assert 1'b1: No mask
8	INVALID_DATA	1'b0: When the PMBus receives an invalid command, ALT_P# will not assert 1'b1: No mask
7	CRC_ERROR	1'b0: When there is a mismatch during the CRC check, ALT_P# will not assert 1'b1: No action
6	MTP_BLK_TRIG	1'b0: When the MTP operation is blocked by the fault stored to the MTP signal, ALT_P# will not assert 1'b1: No mask
5	CML_OTHER_FLT	1'b0: When other communication faults (see STATUS_CML) are triggered, ALT_P# will not assert 1'b1: No mask

4	MTP_FAULT	1'b0: When an MTP fault occurs, ALT_P# will not assert 1'b1: No mask
3	VIN_OVP	1'b0: When a VIN over-voltage (OV) fault occurs, the ALT_P# will not assert 1'b1: No mask
2	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
1	VIN_UVLO	1'b0: When VIN under-voltage lockout (UVLO) occurs, ALT_P# will not assert (warn or fault) 1'b1: No mask
0	OTP	1'b0: When an over-temperature (OT) fault occurs, ALT_P# will not assert 1'b1: No mask

### VOUT\_MODE (20h)

This command on page 0 provides 1 byte to return key VID features that the MP297x can support.

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	0	0	1	0	0	0	0	1

Bits	Bit Name	Description
7:5	DEVICE_VOUT_MODE	Always returns 3'b001. VOUT voltage is in VID mode.
4:0	VID_CODE_TYPE	Always returns 5'b00001. Indicates that the MP2975 supports VID codes for the Intel CPU.

### VOUT\_COMMAND (21h)

This command on page 0 sets the rail 1 reference voltage VID during PMBus override mode.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VOUT_COMMAND								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
8:0	VOUT_COMMAND	Sets the reference voltage VID during PMBus override mode. It is in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh, page 2). 1 VID step/LSB.

### MFR\_IDROOP\_OFFSET (22h)

This command on page 0 instructs the device to fine-tune rail 1's output voltage.

Command	MFR_IDROOP_OFFSET															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	IDROOP_OFFSET				

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	IDROOP_OFFSET	<p>Sets the droop current offset. <math>0.81\mu A/LSB</math></p> <p>This value is two's complement format. Bit[5] is the sign bit. The current list below shows the binary data and the real-world current value:</p> <p>6'b 00 0000: 0  6'b 00 0001: <math>0.81\mu A</math>  6'b 01 1111: <math>25.11\mu A</math>  6'b 10 0000: <math>-25.92\mu A</math>  6'b 10 0001: <math>-25.11\mu A</math>  6'b 11 1111: <math>-0.81\mu A</math></p>

### VOUT\_MAX (24h)

This command on page 0 sets the maximum reference voltage for rail 1 VID-DAC, to set the maximum output voltage. When an external resistive divider is applied, the maximum voltage is clamped to  $VOUT\_MAX / K_R$ .  $K_R$  is the dividing ratio of the external resistive divider.

Command	VOUT_MAX																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_MAX															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MAX	Sets the maximum reference voltage of the VID-DAC in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### VOUT\_MARGIN\_HIGH (25h)

This command on page 0 sets the reference voltage when OPERATION (01h) is set to margin high on rail 1.

Command	VOUT_MARGIN_HIGH																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_MARGIN_HIGH															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MARGIN_HIGH	Sets the margin-high reference voltage level in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step /LSB.

### VOUT\_MARGIN\_LOW (26h)

This command on page 0 sets the reference voltage when OPERATION (01h) is set to margin low on rail 1.

Command	VOUT_MARGIN_LOW																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_MARGIN_LOW															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MARGIN_LOW	Sets the margin-low reference voltage level in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### VOUT\_TRANSITION\_RATE (27h)

This command on page 0 sets rail 1's start-up slew rate for SVID, PMBus, and PVID mode. It also sets the dynamic VID transition slew rate for PMBus and PVID mode, and the AVSBus initial DVID slew rate.

Command	VOUT_TRANSITION_RATE																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_TRANS_CNT															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRANS_CNT	<p>Sets rail 1's dynamic VID transition slew rate during PMBus and PVID mode, initial DVID slew rate in AVSBus mode, and start-up VID transition slew rate for SVID, PMBus, and PVID mode. 100ns/LSB.</p> <p>The PMBus and PVID DVID slew rate can be calculated with the following equation:</p> $\text{DVID\_SR(mV/\mu s)} = \frac{\text{VID\_STEP(mV)}}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu s)}$ <p>The AVSBus initial and maximum DVID slew rate can be calculated with the following equation:</p> $\text{DVID\_SR(mV/\mu s)} = \frac{10(\text{mV})}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu s)}$ <p>If bit[8] of 68h page 0 (SS_SR_SEL) is 1'b0, the SVID start-up slew rate can be calculated with the following equation:</p> $\text{BOOT\_SR(mV/\mu s)} = \frac{\text{VID\_STEP(mV)}}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu s)}$ <p>Where VID_STEP is 5mV or 10mV, which is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2) for rail 1. VOUT_TRANS_CNT is the decimal value defined in VOUT_TRNS_RATE (27h).</p>

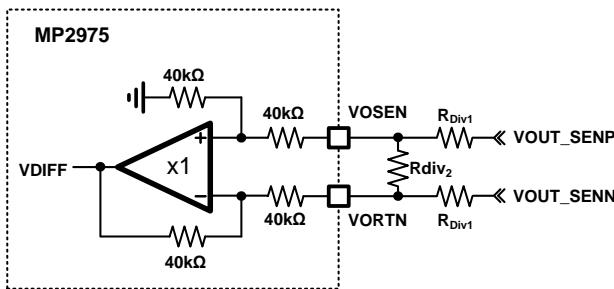
**VOUT\_SENSE\_SET (29h)**

This command on page 0 sets the VOUT sense-related options for rail 1.

Command	VOUT_SENSE_SET															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													VOUT_SCALE

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	DC_LOOP_SNS_SEL	Sets the sensing point for VOUT DC loop calibration. 1'b0: VFB signal 1'b1: VDIFF signal
11	VDIFF_GAIN_SEL	Selects the remote-sense amplifier gain. 1'b0: Unit gain. VOUT is limited to 1.6V 1'b1: Half-gain
10:9	VDIFF_VFB_ADC_GAIN	ADC buffer-sensing gain selector for VDIFF and VFB. 2'b00: Half-gain 2'b01: Unit gain 2'b10 and 2'b11: Three-quarter gain  Note: Set the ADC-sense gain to 2'b01 when the remote-sense amplifier gain is set to half-gain, or the device will not work correctly.
8:0	VOUT_SCALE	Sets the rail 1 VREF-to-VOUT dividing ratio when an external resistive divider is used. VREF ranges from 0.25V to 1.6V. Equation (12) on page 57 shows how to calculate VOUT_SCALE.

When  $V_{OUT}$  exceeds 3.2V, the output voltage must be divided by the reference voltage within 0.25V to 1.6V. The MP2975 provides two methods to sense the output voltage: remote sense and local sense. Remote sense provides better load regulation. Figure 25 shows the typical connections when  $V_{OUT}$  exceeds 3.2V and remote sense is applied.



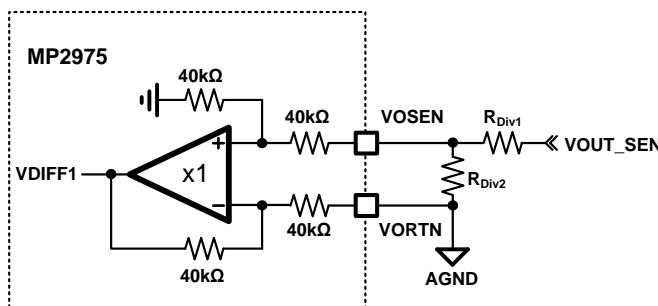
**Figure 25: Output Divider Connections with Remote Sense**

VOUT\_SENP and VOUT\_SENN are from the load and must be routed as a differential pair on quiet areas. Use Equation (11) to calculate the voltage-divider ratio in Figure 25:

$$K_{R\_RS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{\left(\frac{1}{R_{DIV1}} + \frac{2}{R_{DIV2}} + \frac{1}{40K}\right) \times R_{DIV1}} \quad (11)$$

To prevent unregulated output voltage, ensure the voltage on the VOSEN pin is always below the maximum-allowed sensing voltage (VDD33 - 0.3V).

Figure 2 shows how to connect the output divider in applications that exceed the specifications for VOSEN. VORTN is connected directly to AGND to disable remote-sense.



**Figure 26: Output Divider Connections with Local-Sense**

Use Equation (12) to estimate the voltage-divider ratio in Figure 26:

$$K_{R\_LS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{\left(\frac{1}{R_{DIV1}} + \frac{1}{R_{DIV2}} + \frac{1}{80K}\right) \times R_{DIV1}} \quad (12)$$

K<sub>R\_RS</sub> and K<sub>R\_LS</sub> must be programmed into the MP297x by PMBus command VOUT\_SENSE\_SET (29h), bit[8:0] (e.g. VOUT\_SCALE). The MP297x uses it to determine the reference voltage. Equation (13) shows how to calculate VOUT\_SCALE:

$$VOUT\_SCALE = \frac{2^5}{K_R} \quad (13)$$

Where VOUT\_SCALE is the programmed decimal value in register VOUT\_SENSE\_SET (29h), AND K<sub>R</sub> is the value of K<sub>R\_RS</sub> and K<sub>R\_LS</sub>.

Equation (14) shows how to calculate the reference voltage ( $V_{REF}$ ) in the MP2975:

$$V_{REF} = \frac{2^5}{VOUT\_SCALE} \times V_{OUT} \quad (14)$$

Table 12 shows the recommended output resistor dividers and PMBus register settings for typical POL output voltages. It also shows the resistor values in Figure 25 when remote sense is applied. Table 13 shows the resistor values in Figure 26 when local sense is applied.

**Table 12: Recommended Output Dividers with Remote Sense**

V <sub>OUT</sub> (V)	R <sub>DIV1</sub> (kΩ)	R <sub>DIV2</sub> (kΩ)	K <sub>R</sub>	VOUT_SCALE_LOOP (29h)	V <sub>REF</sub> (V)
3.3	3.01	2.05	0.25	0x0020	0.825
5	3.01	1.2	0.164	0x0015	0.82

**Table 13: Recommended Output Dividers with Local Sense**

V <sub>OUT</sub> (V)	R <sub>DIV1</sub> (kΩ)	R <sub>DIV2</sub> (kΩ)	K <sub>R</sub>	VOUT_SCALE_LOOP (29h)	V <sub>REF</sub> (V)
3.3	6.04	2.05	0.25	0x0020	0.825
5	6.04	1.2	0.164	0x0015	0.82

### VOUT\_MIN (2Bh)

This command on page 0 instructs the device to limit rail 1's minimum output voltage for PMBus, PVID, and AVSBus mode. When the output voltage is decoded from AVSBus and the PMBus interface set by the PVID registers is below the value set by VOUT\_MIN (2Bh), the output voltage is clamped to VOUT\_MIN. When an external resistive divider is applied on VOSEN, the minimum output voltage is clamped to VOUT\_MIN / K<sub>R</sub>. K<sub>R</sub> is the dividing ratio of the divider.

Command	VOUT_MIN																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_MIN															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MIN	Sets rail 1's minimum VID under PMBus and AVSBus mode. Any VID below this value is clamped to VOUT_MIN. VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2).

### VIN\_ON (35h)

This command on page 0 sets the VIN under-voltage lockout (UVLO) rising threshold.

Command	VIN_ON																							
Format	Direct																							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Function	X	X	X	X	X	X	X	X	VIN_ON															

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VIN_ON	Sets the VIN under-voltage lockout (UVLO) rising threshold. 0.125V/LSB.

### VIN\_OFF (36h)

This command on page 0 sets the VIN under-voltage lockout (UVLO) falling threshold.

Command	VIN_OFF																							
Format	Direct																							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Function	X	X	X	X	X	X	X	X	VIN_OFF															

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VIN_OFF	Sets the VIN under-voltage lockout (UVLO) falling threshold. 0.125V/LSB.

### MFR\_CONFIG\_REV\_MPS (3Ch)

The MFR\_CONFIG\_REV\_MPS command on page0 sets the internal configuration code revision. It also provides 7 bits to set minimal ADC sampling time.

Command	MFR_CONFIG_REV_MPS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CONFIG_REV_MPS				X				ADC_HOLD_MIN_TIME							

Bits	Bit Name	Description
15:12	CONFIG_REV_MPS	Program the configure file revision for MPS internal use.
11:7	RESERVED	Reserved. Fixed to 0.
6:0	ADC_HOLD_MIN_TIME	Set the minimal interval time between ADC channel switching and sample-hold. 50ns/LSB

### MFR\_OTP\_SET (4Fh)

This command on page 0 sets the over-temperature (OT) threshold and hysteresis. Over-temperature protection (OTP) is triggered by sensing the voltage on the TSEN1 pin.

Command	MFR_OTP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	OTP_HYS							OTP_LIMIT							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:8	OTP_HYS	Sets the over-temperature protection (OTP) recovery hysteresis when OTP is set to auto-retry mode. 1°C/LSB.
7:0	OTP_LIMIT	Sets the over-temperature protection (OTP) threshold. 1°C/LSB.

### MFR\_OTP\_RESPONSE (50h)

This command on page 0 sets the over-temperature protection (OTP) mode.

<b>Command</b>	MFR_OTP_RESPONSE							
<b>Format</b>	Unsigned binary							
<b>Bit</b>	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>					X	X	X	

Bits	Bit Name	Description
7:6	OTP_RESPONSE	2'b00: No action 2'b01: Not used 2'b10: The device shuts down (disables the output) and responds according to the retry setting in bits[5:3]. 2'b11: The device's output is disabled while the fault is present. Operation resumes and the output restarts when the fault condition no longer exists.
5:3	OTP_MODE	Sets the over-temperature protection (OTP) mode. 3'b000: Never restart Others: Retry
2:0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

### OT\_WARN\_LIMIT (51h)

This command on page 0 sets the over-temperature (OT) warning threshold. It is only effective for the temperature sensed on the TSEN1 pin.

<b>Command</b>	OT_WARN_LIMIT															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	OT_WARN_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	OT_WARN_LIMIT	Sets the over-temperature (OT) warning threshold. If the temperature sensed via the TSEN1 pin exceeds this threshold, bit[6] of STATUS_TEMPERATURE (7Dh) is set. 1°C/LSB.

### MFR\_IDROOP\_LIMIT\_SET (52h)

This command on page 0 sets the maximum droop voltage limitation, and sets the signal block time when the low-leakage switch is turned off during DCM.

<b>Command</b>	MFR_IDROOP_LIMIT_SET															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	SW_BLOCK_SET				IDROOP_LIMIT_SET							

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	DCM_LOW_LKG_BLOCK_SET	Sets the set signal block time after the low-leakage slope switch is turned off in DCM mode. 10ns/LSB.

7:0	VDROOP_LIMIT_SET	Sets the maximum absolute droop voltage. If the load current makes the linear droop voltage ( $V_{DROOP}$ ) exceed the set value, the actual droop voltage is clamped to VDROOP_LIMIT_SET.  This value is only valid when nonlinear AVP function is enabled by bit[11] of MFR_IDROOP_CTRL1_R1 (06h on page 2). 250mV/255mV/LSB.
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### MFR\_IMON\_CONFIG (53h)

This command on page 0 sets configurations on the internal IMON1 sense.

Command	MFR_IMON_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	X			

Bits	Bit Name	Description
15:3	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
2	IMON_ANA_FLT_DIS	Enables the internal IC's IMON1 analog filter. 1'b0: Enable IMON1 analog filter 1'b1: Disable IMON1 analog filter
1	IMON_DIGI_FIL_DIS	Enables the IMON1 2-point digital filter. 1'b0: Enable IMON1 2-point digital filter 1'b1: Disable IMON1 2-point digital filter
0	IMON_BIAS_EN	Enables a 20µA biased current on IMON1. This bit improves the IMON report accuracy when IccMAX is very low. 1'b0: No bias current on IMON1 1'b1: Add a 20µA bias current on IMON1

### IOUT\_CAL\_OFFSET (54h)

This command on page 0 sets the offset for rail 1's output current PMBus report. The offset is for IOUT over-reporting or under-reporting. The reported output current is returned via PMBus command READ\_IOUT (8Ch on page 0).

Command	IOUT_CAL_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IOUT_OFFSET_PHS								IOUT_OFFSET_TOT							

Bits	Bit Name	Description
15:14	IOUT_OFFSET_PHS_RES	Sets the bit resolution of IOUT_OFFSET_PHS. 2'b00: 0.25 ADC-step resolution 2'b01: 0.5 ADC-step resolution 2'b10: 1 ADC-step resolution 2'b11: 2 ADC-step resolution

		Sets the per-phase offset for IOUT reporting. It is effective for SVID, and the PMBus and AVSBus IOUT report. The final IOUT report is affected by IOUT_OFFSET_PHS and the active phase number. It is added to the IMON ADC sense result.  Imon_sense = ADC(Imon) + phase_num · IOUT_OFFSET_PHS · $2^{(IOUT_OFFSET_PHS\_RES - 2)}$  This bit is in two's complement data format. Bit[13] is the sign bit. The offset current resolution (IOUT_OFFSET_PHS_RES) is determined by bit[15:14] in this command. The list below shows the binary data and real-world current value.  5'b00000: 0 5'b00001: 1 x IOUT_OFFSET_PHS_RES 5'b01111: 31 x IOUT_OFFSET_PHS_RES 5'b10000: -32 x IOUT_OFFSET_PHS_RES 5'b10001: -31 x IOUT_OFFSET_PHS_RES 5'b11111: -1 x IOUT_OFFSET_PHS_RES
13:9	IOUT_OFFSET_PHS	Sets the total IOUT report offset in two's complement data format. Bit[8] is the sign bit. The total offset only affects the final IOUT PMBus report to READ_IOUT (8Ch, page0). 1A/LSB.  The list below shows the binary data and real-world current values:  9'b 0 0000 0000: 0A 9'b 0 0000 0001: 1A 9'b 0 1111 1111: 255A 9'b 1 0000 0000: -256A 9'b 1 0000 0001: -255A 9'b 1 1111 1111: -1A
8:0	IOUT_OFFSET_PMBUS	

### VIN\_OV\_FAULT\_LIMIT (55h)

This command on page 0 sets the VIN over-voltage protection (OVP) threshold. This register is in linear format. If the sensed input voltage exceeds the VIN\_OV fault limit, the VR will shut down immediately and de-asserts the VRRDY signal.

Command	VIN_OV_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	VIN_OV_FAULT_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VIN_OV_FAULT_LIMIT	Sets VIN over-voltage (OV) threshold. 0.125V/LSB.

### MFR\_APS\_DECAY\_ADV (56h)

This command on page 0 sets the advanced options of APS and decay.

Command	MFR_APS_DECAY_ADV															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									APS_COMP_CNT							
									EN							
									APS_COMP_LEVEL							

Bits	Bit Name	Description
15	VFB_WINDOW_SEL	Selects the threshold for the VFB- window and VFB+ window. 1'b0: VFB- window = VREF - 25mV, VFB+ window = VREF + 20mV 1'b1: VFB- window = VREF - 12.5mV, VFB+ window = VREF + 10mV
14	PRT_THRES_DIV_EN	Enables the protection threshold half-divider for over-voltage protection (OVP2), under-voltage protection (UVP), and reverse-voltage protection (RVP). 1'b0: Disable half-divider 1'b1: Enable half-divider. The OVP2, UVP and RVP thresholds are half of their set value
13	VFB-_DECAY_EXIT_EN	Enables decay exiting when VFB is below the VFB- window. If VFB drops below the VFB- window during the decay, the controller exits decay mode and runs with full phases if UV_DECAY_EXIT_EN = 1. 1'b0: Disable decay exiting when VFB falls below the VFB- window 1'b1: Enable decay exiting when VFB falls below the VFB- window
12:10	VFB-_DECAY_EXIT_TBLANK	Sets the blanking time to exit decay when VFB drops below the VFB- window. 50ns/LSB.
9:5	APS_COMP_CNT	The MP2975 provides positive compensation on VREF during phase-shedding to reduce undershoot. Phase-shedding might come from the SVID SetPS command or APS. VREF compensation is implemented by adding a PMBus-configurable positive voltage on the DC loop COMP. After phase-shedding starts, the voltage returns to 0 step by step with a time interval (see Figure 27). APS_COMP_CNT sets this time interval between each step. 50ns/LSB
4	DECAY_COMP_EN	Enables VREF compensation while exiting decay mode. The MP2975 provides VREF compensation while exiting decay mode. The compensation voltage level uses the same slew rate as it does during auto phase-shedding compensation (see Figure 27). 1'b0: Disable VREF compensation at decay exit 1'b1: Enable VREF compensation at decay exit
3:0	APS_COMP_LEVEL	Sets the VREF compensation level during phase-shedding to reduce undershoot. The compensation is added to VREF when phase-shedding occurs. 1.37mV/LSB.

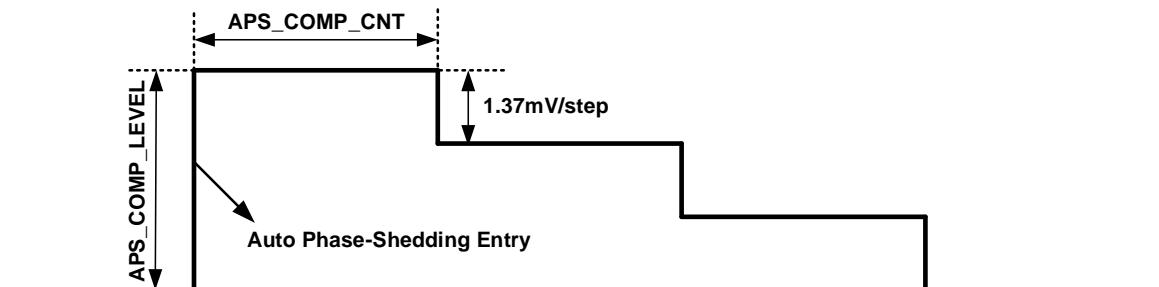


Figure 27: VREF Compensation during Auto Phase-Shedding

### MFR\_APSCtrl (57h)

This command on page 0 sets rail 1 APS-related timing and behaviors.

Command	MFR_APSCtrl															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_PHASE_WAIT_TIME										MIN_TIME_PS0				EN	EN

Bits	Bit Name	Description
15:13	DROP_DELAY_SAMPLE_TIME	Sets the phase-shedding delay time. When the reported load current is below the APS threshold for APS_DELAY_TIME_CNT consecutive times of the IOUT reporting cycle, the controller enters APS mode and automatically sheds the phase count according to the load current.
12:8	DROP_PHASE_WAIT_TIME	Sets the phase-by-phase dropping time intervals. It is only effective when bit[7] of this command is set to 1. 1μs/LSB.
7	DROP_PHASE_MODE_SEL	Sets the phase-dropping mode during phase-shedding. The phase-shedding might be from APS or from SVID SetPS command. 1'b0: Immediately drops the phase count to the target 1'b1: Sheds phases one by one with a configured delay time. The delay is set with DROP_PHASE_WAIT_TIME
6:2	MIN_FULL_PHASE_TIME	Sets the minimum full-phase runtime when the VR exits APS due to an OCP_PHASE, VFB- window, or DVID condition. 50μs/LSB.
1	APS_EXIT_UV_EN	When VFB falls below the VFB- window, enable the VR to exit APS and run with full phase. 1'b0: Disable VFB- window event to exit APS 1'b1: Enable VFB- window event to exit APS
0	APS_EXIT_OC_EN	When phase 1 triggers OCP_PHASE, enables the VR to exit APS and run with full phase. 1'b0: Disable phase1 OCP_PHASE event to exit APS 1'b1: Enable phase1 OCP_PHASE event to exit APS

### MFR\_APS\_FS\_CTRL (58h)

This command on page 0 enables the exit phase-shedding strategy by detecting the PWM frequency, which is referred to as the FS limit event. It also sets the interval between consecutive phases' PWM rising edges to exit phase-shedding.

Command	MFR_APS_FS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables exit phase-shedding according to the PWM1 off time. This threshold is set by register MFR_FS_LIMIT_12P (0Eh on page 1), bit[7:0]. The PWM minimum off time is excluded from the PWM off time (see Figure 28). 1'b0: Disable PWM1 off-time detection to exit APS 1'b1: Enable PWM1 off-time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enables exit phase-shedding according to multi-phase and the PWM interval time between consecutive phases. The threshold is set by registers 0Eh, 0Fh, 11h, 12h, 13h, and 14h on page 1. The PWM blanking time is excluded from the PWM interval (see Figure 29). 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for PWM1 off-time conditions to exit phase-shedding. Once the PWM off-time condition meets the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20μs/LSB.

2:0	FS_EXITAPS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase-shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.
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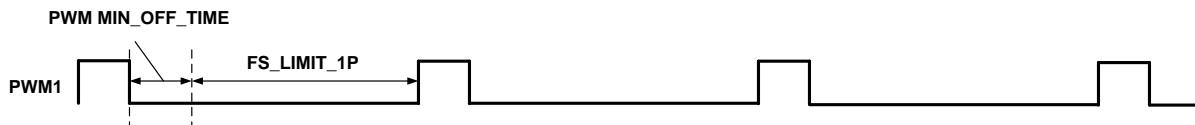


Figure 28: FS\_LIMIT\_1P Condition during 1-Phase Operation

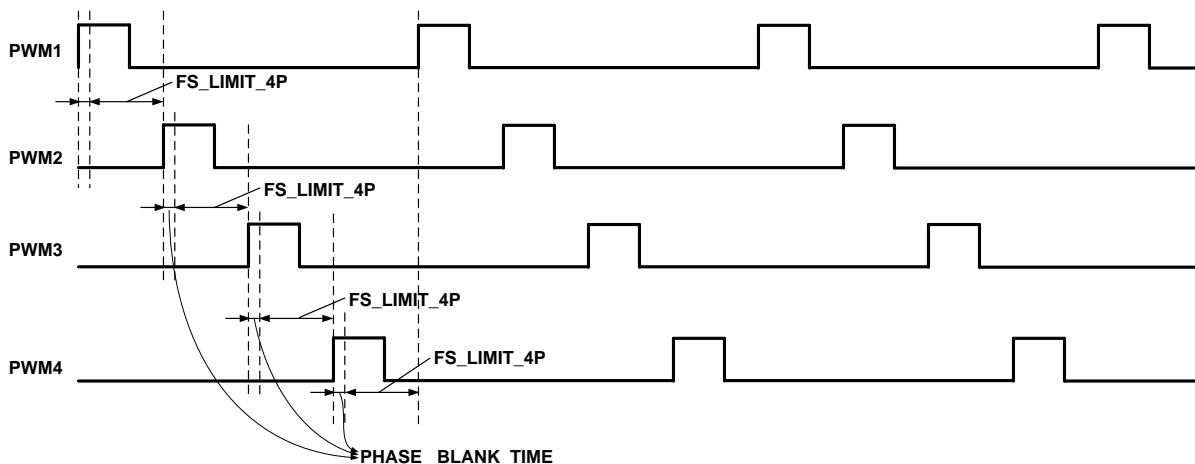


Figure 29: FS\_LIMIT\_NP Condition during N-Phase Operation (N = 4)

#### MFR\_DC\_LOOP\_CTRL (59h)

This command on page 0 sets the DC loop calibration PI parameter and related holding conditions. It also provides 2 bits to program the PWM behavior when phase-adding, and provides 1 bit to program the report format for READ\_VOUT (8Bh on page 0).

Command	MFR_DC_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	VOUT_PMBUS LSB	Sets the READ_VOUT (8Bh on page 0) report format. 1'b0: Direct format. 1mV/LSB 1'b1: VID format
14:9	DC_LOOP_KI	Sets the PI parameter for the DC calibration loop.
8	PRD_ADD_PH_MODE	Sets the phase-adding mode when the PWM period meets the condition set by bit[13:7] for this command. 1'b0: Add phases with a PWM low time inserted between Hi-Z and Hi 1'b1: Add phases with no PWM Hi-Z to Hi low time
7	VFB-_ADD_PH_MODE	Sets the phase-adding mode when VFB is below the VFB- window. 1'b0: Add phases with a PWM low time inserted between Hi-Z and Hi 1'b1: Add phases with no PWM Hi-Z to Hi low time

6	PRD_HOLD_DC_EN	Holds the DC loop when the PWM interval meets the PWM switching period conditions set via PMBus command MFR_FS (5Ch), bit[15:9]. 1'b0: Do not hold the DC loop when the PWM switching period condition meets the PWM interval 1'b1: Hold the DC loop when the PWM switching period condition meets the PWM interval
5	PS_HOLD_DC_EN	Holds the DC loop when the phase count is changed. 1'b0: Disable phase number change to hold the DC loop 1'b1: Enable phase number change to hold the DC loop
4	TRANS_HOLD_DC_EN	Holds DC loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ window or VFB- window). 1'b0: Disable the VFB+- window condition to hold the DC loop 1'b1: Enable the VFB+- window condition to hold the DC loop
3:0	DC_CAL_MIN_THOLD	Sets the DC loop minimal holding time in direct format. 200µs/LSB with +100µs offset.

#### MFR\_CB\_LOOP\_CTRL (5Ah)

This command on page 0 enables rail 1's current balance loop. It also sets the current balance loop PI parameter and its related holding conditions.

Command	MFR_CB_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	CB_LOOP_EN	Enables current balance loop. 1'b0: Disable current balance loop 1'b1: Enable current balance loop
11:8	CB_LOOP_KI	Sets the PI parameter for current balance loop.
7	TRANS_HOLD_CB_EN	Holds the current balance loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ window or VFB- window). 1'b0: No action 1'b1: Hold the current balance loop regulation when a load transient event is detected
6	PRD_HOLD_CB_EN	Holds the current balance loop when the PWM time interval meets the PWM switching period condition set with PMBus command MFR_FS (5Ch), bit[15:9]. 1'b0: Do not hold the current balance loop when the PWM switching period condition is met 1'b1: Hold the current balance loop when the PWM switching period condition is met
5	PS_HOLD_CB_EN	Holds the current balance loop when the phase count is changed. 1'b0: Do not hold the current balance loop when the phase count is changed 1'b1: Hold the current balance loop when the phase count is changed
4	DVID_HOLD_CB_EN	Holds the current balance loop when DVID occurs. 1'b0: Do not hold the current balance loop hold when DVID occurs 1'b1: Hold the current balance loop when DVID occurs

3:0	CB_LOOP_THOLD	Sets the current balance loop hold time. When any load transient event, PWM switching period change event, phase count change, or DVID event is detected, and the corresponding enable bit is set, the current balance loop stops regulating for a time set with command CB_LOOP_THOLD. 100µs/LSB.
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### MFR\_FS\_LOOP\_CTRL (5Bh)

This command on page 0 enables rail 1's frequency loop. It also sets the frequency loop PI parameters, and related holding conditions.

Command	MFR_FS_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	FS_LOOP_EN	Enables frequency loop. 1'b0: Disable frequency loop 1'b1: Enable frequency loop
13:7	FS_LOOP_KI	Sets the frequency loop regulation parameter.
6	TRANS_HOLD_FS_EN	Holds the frequency loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ window or VFB- window). 1'b0: Do not hold the frequency loop regulation when a load transient event is detected 1'b1: Hold the frequency loop regulation when a load transient event is detected
5	PS_HOLD_FS_EN	Holds the frequency loop regulation when the phase count is changed. 1'b0: Do not hold the frequency loop regulation when the phase count is changed 1'b1: Hold the frequency loop regulation when the phase count is changed
4	DVID_HOLD_FS_EN	Holds the frequency loop regulation when DVID happens. 1'b0: Do not hold the frequency loop when DVID occurs 1'b1: Hold the frequency loop regulation when DVID occurs
3:0	FS_LOOP_HOLD_TIME	Sets the minimum frequency loop hold time after any load transient event, PWM switching period change, phase count change, or DVID event is detected. The corresponding enable bit must be set. 100µs/LSB.

### MFR\_FS (5Ch)

This command on page 0 sets rail 1's switching frequency. It also sets the range of PWM periods for DC and current balance loops.

Command	MFR_FS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	HOLD_CB_DC_PRD_TIME															

Bits	Bit Name	Description
15:9	HOLD_CB_DC_PRD_TIME	<p>Sets the period changing time to hold the DC and current balance loops. If the PWM period meets the conditions below and the associated enable bits are set, the DC and current balance loops are held. All the loop hold functions related to this time setting are ineffective during DCM. (The MP2975 uses this time to hold the CB and DC loop. The FS loop cannot be held with a PWM time interval.) The real-time PWM period can be estimated with the following equation:</p> $  t_{PWM} - t_{PWM\_REF}   \leq HOLD\_CB\_DC\_PRD\_TIME \times 80\text{ns}$ <p>Where <math>t_{PWM}</math> is the real-time PWM period, and <math>t_{PWM\_REF}</math> is the nominal period set with the MFR_FS_SET command. 80ns/LSB.</p>
8:0	FS_SET	Sets the switching frequency in direct format.10kHz/LSB.

### MFR\_VR\_PROTECT\_SET (5Dh)

This command on page 0 sets certain protections for the MP2975.

Command	MFR_VR_PROTECT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function														X	X	

Bits	Bit Name	Description
15	CHIP OTP MODE	<p>Selects the chip's over-temperature protection (OTP) mode. The chip protects the MP2975 junction from an over-temperature condition. When the chip temperature exceeds 155°C, an OT fault occurs, and the chip shuts down both rails immediately if CHIP OTP EN = 1.</p> <p>1'b0: Auto-retry mode 1'b1: Latch off mode</p>
14	CHIP OTP EN	<p>Enables VR shutdown when chip over-temperature protection (OTP) occurs. It is valid for both rails.</p> <p>1'b0: Disable chip OTP 1'b1: Enable chip OTP</p>
13	VIN_OVP_MODE	<p>Selects the VIN OVP action mode.</p> <p>1'b0: Auto-retry mode 1'b1: Latch off mode</p>
12	TSEN2_DGTL_FLT_DIS	<p>Enables rail 1's TSEN2 digital-sense fault to shut down rail 1. The MP2975 senses the voltage on the TSEN2 pin with an internal ADC. Once the sensed voltage on TSEN2 is above or below the configurable level set by MFR_TSEN2_SNS_FLT_SET (55h on page1) bit[7:0], the MP2975 indicates a TSEN2 fault and shuts down rail 1 immediately. TSEN2's sensed fault direction is determined by MFR_TSEN2_SNS_FLT_SET (55h on page 1), bit[15].</p> <p>TSEN2's digital-sense fault detection does not affect the voltage monitor by the TSEN2 pin or affect TSEN2 analog fault protection.</p> <p>1'b0: Disable TSEN2 digital-sense fault protection 1'b1: Enable TSEN2 digital-sense fault protection</p>

11	TSEN2_ANA_FLT_DIS	Enables rail 1's TSEN2 analog fault to shut down rail 1. The MP2975 monitors the voltage on the TSEN2 pin. If the TSEN2 voltage is above or below a configurable threshold set by MFR_TSEN2_ANAFLT_SET (51h on page 1) bit[5:0], the MP2975 indicates a TSEN2 fault has occurred and shuts down rail 1 immediately. TSEN2's analog fault direction is determined by MFR_TSEN2_ANAFLT_SET (51h, page 1), bit[15].  TSEN2 analog fault detection does not affect the ADC sensing by the TSEN2 pin or TSEN2 digital-sense fault protection.  1'b0: Disable TSEN2 analog fault protection 1'b1: Enable TSEN2 analog fault protection
10	DRMOS_FAULT_MODE	Selects the CS fault and TSEN1 fault (TSEN1 exceeds 2.4V) action mode.  1'b0: Auto-retry mode 1'b1: Latch mode
9	PWM_FLT_DTCT_EN	Enables rail 1's Intelli-Phase™ fault type detection with a PWM pin. It is only effective when the Intelli-Phase™ supports fault type reporting with the PWM pin.  1'b0: Disable PWM pin fault type detection 1'b1: Enable PWM pin fault type detection
8	CS_FLT_EN	Enables rail 1's CS fault protection. The MP297x monitors the voltage level on the CS pin. Once CS drops below 200mV, the MP297x indicates a CS fault and shuts down immediately.  1'b0: Disable CS fault detection 1'b1: Enable CS fault detection
7	TSEN1_FLT_DIS	Enables a TSEN1 fault to shut down rail 1. The MP297x monitors the voltage level on the TSEN1 pin. Once the TSEN1 voltage exceeds 2.4V, the MP297x indicates a TSEN1 fault and shuts down rail 1 immediately.  TSEN1 fault detection does not affect over-voltage protection (OTP) or the power-stage temperature sensing on the TSEN1 pin.  1'b0: Disable TSEN1 fault protection 1'b1: Enable TSEN1 fault protection
6:4	VIN_PRT_DIS	3'b110: Disable VIN under-voltage lockout (UVLO) and over-voltage protection (OVP) Others: Enable VIN under-voltage lockout (UVLO) and over-voltage protection (OVP)
3:2	OVP1_DIS	Disables the VOUT over-voltage protection (OVP1) protection for debugging purposes. It is recommended to enable OVP1 protection during normal mode.  2'b01: Disable VOUT OVP1 protection Others: Enable VOUT OVP1 protection
1:0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

**MFR\_VR\_CONFIG2 (5Eh)**

This command on page 0 sets related options for rail 1's VBOOT and Hi-Z shutdown voltage level, and selects the PVID and PMBus override modes.

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														VID_SHUT_DOWN

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	PIN_RESET_VBOOT_EN	Enables SDIO reset function. When the SDIO pin is pulled low for 4ms, the VR resets to the boot voltage. It is effective for SVID, PMBus, and AVSBus mode, and is valid for both rails. 1'b0: Disable SDIO reset function 1'b1: Enable SDIO reset function
12	BOOT_MODE_SEL	Selects whether the rail 1 start-up voltage is set by a register or pin. 1'b0: VBOOT is set by bits [12:5] of register MFR_VR_MULTI_CONFIG (0Dh on page 2) 1'b1: PMBus VBOOT is set by a pin. The BOOT pin is assigned the ADDR/CONFIG pin. This pin is currently not recommended for use.
11	PVID_EN	Enables rail 1 PVID mode. 1'b0: Disable PVID mode 1'b1: Enable PVID mode
10	PIN_VBOOT_MODE	Selects rail 1's PIN_VBOOT mode. 1'b0: Select 4 bits to determined VBOOT. These 4 bits are defined by ADDR/CONFIG. 1'b1: Select 3MSB to determined VBOOT. The 3MSB is defined by ADDR/CONFIG.
9	PMBUS_EN	Enables rail 1 PMBus override mode. 1'b0: Disable PMBus override mode 1'b1: Enable PMBus override mode
8:0	VID_SHUT_DOWN	Sets rail 1 VID threshold at which all PWMs go into tri-state when VID slews to 0V. The Hi-Z shutdown voltage level is only effective while VID slews down to 0V. The VID slew down to 0 actions may be caused by soft-off or a command to make DVID 0V. Once the VID DAC output drops below the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged naturally by the load current (see Figure 30). It is in direct format with VID resolution. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

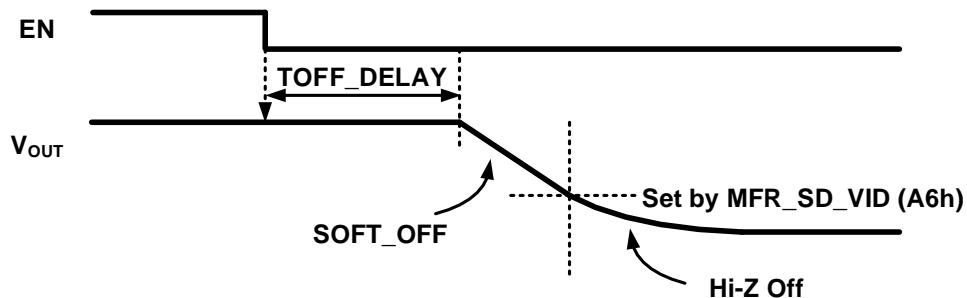


Figure 30: EN Soft-Off to Hi-Z Off Level

**MFR\_OCP\_TOTAL\_SET (5Fh)**

This command on page 0 sets the related options and values for rail 1's OCP\_Total.

Command	MFR_OCP_TOTAL_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	OCP_TOTAL_TBLANK										OCP_TOTAL_CUR				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:13	OCP_TOTAL_MODE	Sets the OCP_TOTAL action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
12:7	OCP_TOTAL_TBLANK	Sets the blanking time for OCP_TOTAL in direct format. 100µs/LSB.
6:0	OCP_TOTAL_CUR	Sets the rail 1 per-phase OCP_TOTAL entry threshold in direct format. 1A/LSB.

### TON\_DELAY (60h)

This command on page 0 sets the delay time from when system initialization ends to when rail 1's VREF starts up.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the delay time from when system initialization ends to when VREF boots up. The resolution is determined by bit[14] of PMBus command MFR_SLOPE_ANA_CTRL (76h on page 0) (e.g. ON/OFF_DLY_CLK_SEL). 20µs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50µs/LSB (ON/OFF_DLY_CLK_SEL = 1)

### MFR\_OVP\_UVP\_MODE (61h)

This command on page 0 sets the rail 1 over-voltage protection (OVP) and under-voltage protection (UVP), as well as related options and values.

Command	MFR_OVP_UVP_MODE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OVP2_BLANK_TIME								UVP_BLANK_TIME							

Bits	Bit Name	Description
15:14	OVP2_MODE	Selects the over-voltage protection (OVP2) action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 3 or 6 times (set by bit[13])
13	OVP2_RETRY_TIMES	This bit sets the retry times when bit[15:14] (OVP2_MODE) = 2'b11 1'b1: Retry 3 times 1'b0: Retry 6 times
12:8	OVP2_BLANK_TIME	Sets the OVP2 blanking time. When an OVP2 condition continues for longer than the OVP2 blanking time, an OVP2 fault occurs. 100ns/LSB.

7:6	UVP_MODE	Selects the under-voltage protection (UVP) reponse. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	UVP_BLANK_TIME	Sets the under-voltage protection (UVP) blanking time. When a UV condition continues for longer than the UVP blanking time, a UVP fault occurs. 20µs/LSB.

### MFR\_CUR\_GAIN (62h)

This command on page 0 sets rail 1's phase current-sense gain. The MP297x senses the phase current by monitoring the voltage on CS. The gain affects the real per-phase current limit. Equation (15) and Equation (16) calculate the relationship between current-sense gain/offset and the actual positive phase current limitation. Equation (17) and Equation (18) estimate the relationship between the current-sense gain/offset and the actual negative current phase limit.

OCP\_PHASE for current mode (IOUT sensing the DrMOS):

$$0.005 \times \left( \frac{\text{PHASE\_CUR\_GAIN} \text{ QCP\_PHASE}}{256} - 10 + \text{PHASE\_CUR\_OFFSET} \right)_{1:28} I_{\text{PH\_LMT}} 1000 K_{\text{CS}} 1:23 \quad (15)$$

OCP\_PHASE for voltage mode (IOUT sensing the DrMOS):

$$0.005 \times \left( \frac{\text{PHASE\_CUR\_GAIN} \text{ QCP\_PHASE}}{256} + 104 + \text{PHASE\_CUR\_OFFSET} \right)_{1:28} I_{\text{PH\_LMT}} 1000 K_{\text{CS}} 1:8 \quad (16)$$

UCP\_PHASE for current mode (IOUT sensing the DrMOS):

$$0.005 \times \left( 142 - \frac{\text{PHASE\_CUR\_GAIN} \text{ UCP\_PHASE}}{256} - \text{PHASE\_CUR\_OFFSET} \right)_{0:52} I_{\text{PH\_LMT}} 1000 K_{\text{CS}} \quad (17)$$

UCP\_PHASE for current mode (IOUT sensing the DrMOS):

$$0.005 \times \left( 256 - \frac{\text{PHASE\_CUR\_GAIN} \text{ QCP\_PHASE}}{256} - \text{PHASE\_CUR\_OFFSET} \right)_{0:52} I_{\text{PH\_LMT}} 1000 K_{\text{CS}} \quad (18)$$

Command	MFR_CUR_GAIN																									
Format	Unsigned binary																									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W										
Function	X	X	X	X	X	X	PHASE_CUR_GAIN																			
Bits	Bit Name			Description																						
15:10	RESERVED			Unused. X indicates that writes are ignored and reads are always 0.																						
9:0	PHASE_CUR_GAIN			Sets phase current-sense gain with the equation below: $\text{PHASE\_CUR\_GAIN} = \frac{256 \times K_{\text{CS}}}{5}$ Where $K_{\text{CS}}$ is the current-sense gain of Intelli-Phase™ (in $\mu\text{A/A}$ ).																						

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	PHASE_CUR_GAIN	Sets phase current-sense gain with the equation below: $\text{PHASE\_CUR\_GAIN} = \frac{256 \times K_{\text{CS}}}{5}$ Where $K_{\text{CS}}$ is the current-sense gain of Intelli-Phase™ (in $\mu\text{A/A}$ ).

### MFR\_CUR\_OFFSET (63h)

This command on page 0 sets the rail 1 phase current-sense offset.

<b>Command</b>	MFR_CUR_OFFSET															
<b>Format</b>	Two's complement															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	UCP_PHASE_OFFSET								OCP_PHASE_OFFSET							

Bits	Bit Name	Description
15:8	UCP_PHASE_CUR_OFFSET	Sets the under-current protection (UCP) phase current-limitation offset. It is in two's complement format. Bit[15] is the sign bit. The list below shows the binary data and real-world current values:  8'b 0000 0000: 0 8'b 0000 0001: (-1 x 5 / Kcs) A 8'b 0111 1111: (-127 x 5 / Kcs) A 8'b 1000 0000: (128 x 5 / Kcs) A 8'b 1000 0001: (127 x 5 / Kcs) A 8'b 1111 1111: (1 x 5 / Kcs) A  Where Kcs is current-sense gain of the Intelli-Phase™ (in $\mu$ A/A).
7:0	OCP_PHASE_CUR_OFFSET	Sets the over-current protection (OCP) phase current-limitation offset. It is in two's complement format. Bit[7] is the sign bit. The list below shows the binary data and real-world current values:  8'b 0000 0000: 0 8'b 0000 0001: (1 x 5 / Kcs) A 8'b 0111 1111: (127 x 5 / Kcs) A 8'b 1000 0000: (-128 x 5 / Kcs) A 8'b 1000 0001: (-127 x 5 / Kcs) A 8'b 1111 1111: (-1 x 5 / Kcs) A  Where Kcs is the current-sense gain of the Intelli-Phase™ (in $\mu$ A/A).

### TOFF\_DELAY (64h)

This command on page 0 sets the delay time from when EN goes low to when VREF starts to shut down on rail 1.

<b>Command</b>	TOFF_DELAY															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the delay time from EN going low to VREF shutdown. The resolution is determined by bit[14] of PMBus command MFR_SLOPE_ANA_CTRL (76h on page 0) (e.g. ON/OFF_DLY_CLK_SEL).  20 $\mu$ s/LSB (ON/OFF_DLY_CLK_SEL = 0) 50 $\mu$ s/LSB (ON/OFF_DLY_CLK_SEL = 1)

**MFR\_OCP\_UCP\_PHASE\_SET (65h)**

This command on page 0 sets rail 1's per-phase valley current limit.

<b>Command</b>	MFR_OCP_UCP_PHASE_SET															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	UCP_PHASE_LIMIT								OCP_PHASE_LIMIT							

Bits	Bit Name	Description
15:8	UCP_PHASE_LIMIT	Sets the per-phase negative valley current limit in direct format. -1A/LSB.
7:0	OCP_PHASE_LIMIT	Sets the per-phase positive valley current limit in direct format. 1A/LSB.

**MFR\_LINE\_FLOAT\_EN (66h)**

This command on page 0 provides 2 bits to enable floating line protection on rail 1 and rail 2.

<b>Command</b>	MFR_LINE_FLOAT_EN															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

Bits	Bit Name	Description
15:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	VOSEN_FLOAT_EN	Enables VOSEN floating line detection and protection. 1'b0: Disable VOSEN floating line detection and protection 1'b1: Enable VOSEN floating line detection and protection
0	VORTN_FLOAT_EN	Enables VORTN floating line detection and protection. 1'b0: Disable VORTN floating line detection and protection 1'b1: Enable VORTN floating line detection and protection

**MFR\_VR\_CONFIG1 (68h)**

This command on page 0 programs basic system configurations for rail 1.

<b>Command</b>	MFR_VR_CONFIG1															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X				X											

Bits	Bit Name	Description
15:14, 11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:12	DRMOS_KCS	Selection bit for the DRAMOS Kcs gain for rail 1. 3'b000: 5µA/A 3'b001: 8.5µA/A 3'b010: 9.7µA/A 3'b011: 10µA/A Others: Reserved

10	DROOP_COMP_LOOP_BW	This bit sets the droop compensation loop bandwidth together with bit[8] of register 06h on page 2 (AC_DROOP_BW_SEL).													
		<table border="1"> <thead> <tr> <th>DROOP_COMP_LOOP_BW</th><th>AC_DROOP_BW_SEL (Bit[8] 06h on Page 2)</th><th>BW</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>25kΩ</td></tr> <tr> <td>0</td><td>1</td><td>50kΩ</td></tr> <tr> <td>1</td><td>0</td><td>250kΩ</td></tr> <tr> <td>1</td><td>1</td><td>500kΩ</td></tr> </tbody> </table>	DROOP_COMP_LOOP_BW	AC_DROOP_BW_SEL (Bit[8] 06h on Page 2)	BW	0	0	25kΩ	0	1	50kΩ	1	0	250kΩ	1
DROOP_COMP_LOOP_BW	AC_DROOP_BW_SEL (Bit[8] 06h on Page 2)	BW													
0	0	25kΩ													
0	1	50kΩ													
1	0	250kΩ													
1	1	500kΩ													
Enable bit to disable PWM Hi-Z behavior after receiving a decay command. 1'b0: VR executes normal decay behavior, and PWMs go to Hi-Z. 1'b1: VR slews to target VID with a slow slew rate after receiving a decay command.															
Selection bit for soft-start slew rate. It is only valid for non AVSBus mode. 1'b1: The soft-start slew rate follows the SLEW_SLOW_SR command set by register 01h on page 2. 1'b0: The soft-start slew rate follows the BOOT_SR command set by register 27h on page 0.															
Enables DC loop calibration during DCM. 1'b0: Disable DC loop calibration during DCM 1'b1: Enable DC loop calibration during DCM															
6	DC_LOOP_EN	Enables DC loop calibration during both DCM and CCM operation. 1'b0: Disable DC loop calibration during both DCM and CCM operation 1'b1: Enable DC loop calibration during both DCM and CCM operation													
5	FORCE_PS_EN	Enable to force power state. It is only effective when OPERATION (01h), bit[5:4] is not set to 2'b11. 1'b0: Disable forced power state with bit[4:3] of MFR_VR_CONFIG1 (68h on page 0) 1'b1: Enable forced power state with bit[4:3] of MFR_VR_CONFIG1 (68h on page 0)													
4:3	FORCE_PS_SET	Power-state selection bits when MFR_VR_CONFIG1 (68h, page0), bit[5] = 1. 2'b00: Full-phase CCM. The phase count is determined by bit[3:0] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2) 2'b01: 1-phase CCM 2'b1X: 1-phase DCM													
2	DCM_TON_SET	Sets the PWM on time during DCM operation. 1'b0: PWM on time during DCM is the same as during CCM operation 1'b1: PWM on time during DCM is 75% of that in CCM operation													
1	OSR_EN	Enables overshoot reduction. 1'b0: Disable overshoot reduction 1'b1: Enable overshoot reduction													
0	SVID_OVERCLK_EN	Enables overclocking mode in SVID mode. In SVID overclocking mode, the VID value is determined by PMBus command VOUT_COMMAND (21h on page 0), but the VR still responds to all CPU SVID commands. 1'b0: Disable SVID overclocking mode 1'b1: Enable SVID overclocking mode													

### MFR\_BLANK\_TIME2 (69h)

This command on page 0 programs the second set of slope compensation reset times and PWM blanking times between two consecutive phases (for rail 1 only).

Three sets of SLOPE\_RESET\_TIME and PWM\_BLANK\_TIME can be set by registers 69h, 6Ah, and 72h on page 0. One of them is selected as the real-time value, according to the operation phase number. The relationship is calculated with Equation (19) and Equation (20):

$$\text{SLOPE_RESET_TIME} = \begin{cases} \text{SLOPE_RESET_TIME1}(\text{reg } 72\text{h bit}[11:6]), & \text{phase num} \geq \text{PHS_NUM_LVL1} \\ \text{SLOPE_RESET_TIME2}(\text{reg } 69\text{h bit}[11:6]), & \text{PHS_NUM_LVL2} \leq \text{phase num} < \text{PHS_NUM_LVL1} \\ \text{SLOPE_RESET_TIME3}(\text{reg } 6\text{Ah bit}[11:6]), & \text{phase num} < \text{PHS_NUM_LVL2} \end{cases} \quad (19)$$

$$\text{PWM_BLANK_TIME} = \begin{cases} \text{PWM_BLANK_TIME1}(\text{reg } 72\text{h bit}[5:0]), & \text{phase num} \geq \text{PHS_NUM_LVL1} \\ \text{PWM_BLANK_TIME2}(\text{reg } 69\text{h bit}[5:0]), & \text{PHS_NUM_LVL2} \leq \text{phase num} < \text{PHS_NUM_LVL1} \\ \text{PWM_BLANK_TIME3}(\text{reg } 6\text{Ah bit}[5:0]), & \text{phase num} < \text{PHS_NUM_LVL2} \end{cases} \quad (20)$$

Where PHS\_NUM\_LVL1 is the phase number set by register MFR\_BLANK\_TIME2 (69h on page 0) bit[15:12], and PHS\_NUM\_LVL2 is the phase number set by register MFR\_BLANK\_TIME2 (6Ah on page 0) bit[15:12].

Command	MFR_BLANK_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL1						SLOPE_RESET_TIME2						PWM_BLANK_TIME2			

Bits	Bit Name	Description
15:12	PHS_NUM_LVL1	Sets the phase number threshold to slope compensation reset time and PWM blanking time.
11:6	SLOPE_RESET_TIME2	Programs the second set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h, page0), bit[4] = 0. The slope compensation reset time should not exceed the PWM blanking time set by PWM_BLANK_TIME (e.g. bit[5:0] in register MFR_BLANK_TIME2 (69h on page 0)). 5ns/LSB.
5:0	PWM_BLANK_TIME2	Programs the second set of PWM blanking times between two consecutive phases. 5ns/LSB.

### MFR\_BLANK\_TIME3 (6Ah)

This command on page 0 programs the third set of slope compensation reset times and PWM blanking times between two consecutive phases (for rail 1 only).

Command	MFR_BLANK_TIME3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL2						SLOPE_RESET_TIME3						PWM_BLANK_TIME3			

Bits	Bit Name	Description
15:12	PHS_NUM_LVL2	Sets the phase number threshold to slope compensation reset time and PWM blanking time.

11:6	SLOPE_RESET_TIME3	Programs the third set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h, page0), bit[4] = 0. The slope compensation reset time should not exceed the PWM blanking time set by PWM_BLANK_TIME (e.g. bit[5:0] in register MFR_BLANK_TIME2 (6Ah on page 0)), 5ns/LSB.
5:0	PWM_BLANK_TIME3	Programs the third set of PWM blanking times between two consecutive phases. 5ns/LSB.

### MFR\_DROOP\_CMPN1 (6Bh)

This command on page 0 sets how the device compensates for the voltage drop caused by extra droop current when a droop resistor is applied and DVID is upward.

Command	MFR_DROOP_CMPN1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROOP_CMPN_LIMIT															

Bits	Bit Name	Description
15	DROOP_CMPN_EN	Droop compensation enable bit. 1'b0: Disable droop compensation 1'b1: Enable droop compensation
14:9	CNT_DROOP_CMPN_DEC	Sets the time interval for each VID step to reset droop compensation after DVID upward ends. 50ns/LSB.
8:6	CNT_DROOP_CMPN_INC	VID step counter to increase each step of droop compensation during upward DVID. VID_DROOP_CMPN_STEP = CNT_DROOP_CMPN_INC x VID_STEP.
5:0	DROOP_CMPN_LIMIT	Sets the maximum VID steps for droop compensation in direct format with VID step resolution. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### MFR\_DROOP\_CMPN2 (6Ch)

This command on page 0 sets how the device compensates for the voltage drop caused by extra droop current when a droop resistor is applied and DVID is upward.

Command	MFR_DROOP_CMPN2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	VID_FLTR_SEL	Selects the VID DAC output filter when DVID is downward. 2'b00: 2.14µs 2'b01: 4.28µs 2'b10: 6.42µs 2'b11: 8.56µs
13	VID_FLTR_EN	Enables the VID DAC output filter. 1'b0: Disable the VID DAC filter 1'b1: Enable the VID DAC filter

12	VID-DAC_CMPN_EN	Enables the comparator between the VID-DAC output and VID-DAC filter output, which smooths the transition between DVID downward and DVID upward. 1'b0: Disable the VID-DAC comparator 1'b1: Enable VID-DAC comparator
11:6	DLY_RST_DROOP_CMPN	Sets the delay time after VR_SETTLE to reset droop compensation when DVID is upward. 50ns/LSB.
5:0	VID_FLTR_ACT_CTRL	Sets the effective VID filter threshold in direct format when the droop compensation is reset to 0. It is only effective when bit[13], VID_FLT_EN = 1. 1 VID step/LSB.

### MFR\_PGOOD\_SET (6Dh)

This command on page 0 instructs the device when to assert VRRDY1 by setting the VRRDY1 action mode and VRRDY1 signal assertion delay time. The VRRDY assertion delay time is only effective during VRRDY non-Intel mode.

Command	MFR_PGOOD_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	PGOOD_MODE	Sets the VRRDY action mode. 1'b0: Intel mode. VRRDY asserts once VID reaches the boot-up voltage 1'b1: Non-Intel mode. VRRDY asserts when it meets the condition set by PMBus command POWER_GOOD_ON (6Eh on page 0), and the VRRDY delay time expires
7:0	PGOOD_DELAY	Sets the VRRDY assertion delay time. It is only effective when VRRDY mode is set to Non-Intel mode. 1μs/LSB.

### POWER\_GOOD\_ON (6Eh)

This command on page 0 sets the output voltage threshold at which the VRRDY1 signal asserts. It is only effective in VRRDY non-Intel mode.

Command	POWER_GOOD_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									POWER_GOOD_ON

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_ON	Sets the reference voltage threshold at which the VRRDY signal asserts. It is only effective when the VRRDY mode is selected as non-Intel mode. POWER_GOOD_ON is in direct format with the VID resolution. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### **POWER\_GOOD\_OFF (6Fh)**

This command on page 0 sets the output voltage threshold at which the VRRDY1 signal de-asserts. It is only effective when VRRDY is set to non-Intel mode.

Command	POWER_GOOD_OFF																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	POWER_GOOD_OFF															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_OFF	Sets the reference voltage threshold at which the VRRDY signal de-asserts. It is only effective when VRRDY mode is set to non-Intel mode. POWER_GOOD_OFF is in direct format with the VID resolution. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### **MFR\_BLANK\_TIME1 (72h)**

This command on page 0 programs the first set of slope compensation reset times and PWM blanking times between two consecutive phases (for rail 1 only).

Command	MFR_BLANK_TIME1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	SLOPE_RESET_TIME1										PWM_BLANK_TIME1				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:12	SLOPE_RST_SW_SEL	Selects slope reset switch for different fsw. Target the increase the slope reset speed for high frequency. With a stronger switch, turn on the low-leakage switch during DCM. Strong level = SLOPE_RST_SW_SEL + 1
11:6	SLOPE_RESET_TIME1	Programs the first set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h on page 0), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME (e.g. bit[5:0] in register MFR_BLANK_TIME2 (72h on page 0)). 5ns/LSB.
5:0	PWM_BLANK_TIME1	Programs the first set of PWM blanking times between two consecutive phases. 5ns/LSB.

### **MFR\_OSR\_SET (73h)**

This command on page 0 sets the overshoot reduction (OSR) related parameters (for rail 1 only).

Command	MFR_OSR_SET																
Format	Unsigned binary																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	X	X	OSR_DEGLITCH_TIME										OSR_BLANK_TIME			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MIN_OSR_TIME	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MIN_OSR_INTERVAL_TIME	Sets the blanking time between two effective OSR events. 10ns/LSB.

### MFR\_PWM\_MIN\_TIME1 (74h)

This command on page 0 sets the minimum pulse width when PWM is high, low, or in tri-state (for rail 1 only).

Command	MFR_PWM_MIN_TIME1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	PWM_MIN_LOW_TIME										MIN_HIGH_TIME	PWM_MIN_TRI_TIME			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	PWM_MIN_LOW_TIME	Sets the minimum PWM low time. 10ns/LSB with -5ns offset. The minimum PWM low time can be calculated with the following equation: $(\text{PWM\_MIN\_LOW\_TIME} \times 10 - 5) \text{ ns}$
8:6	PWM_MIN_HIGH_TIME	Sets the minimum PWM high time. 10ns/LSB with -5ns offset. The minimum PWM high time can be calculated with the following equation: $(\text{PWM\_MIN\_HIGH\_TIME} \times 10 - 5) \text{ ns}$
5:0	PWM_MIN_TRI_TIME	Sets the minimum PWM tri-state time. 10ns/LSB with -5ns offset. The minimum PWM tri-state time can be calculated with the following equation: $(\text{PWM\_MIN\_TRI\_TIME} \times 10 - 5) \text{ ns}$

### MFR\_PWM\_MIN\_TIME2 (75h)

This command on page 0 sets the PWM minimum off time and PWM on pulse width when under-current protection (UCP) is triggered (for rail 1 only).

Command	MFR_PWM_MIN_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	TON_LIMIT_TO_VCAL				UCP_TIME				MIN_OFF_TIME					

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	Sets the $t_{ON}$ limit below which the DC loop regulation will never be held. For the MP297x, the DC loop can be held if the PWM period meets the condition set in MFR_FS (5Ch on page 0), bit[15:9]. If the calculated PWM on time with Equation (1) is less than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	ZCD_EN	Enables rail 1 zero-current crossing detection (ZCD). 1'b0: Disable ZCD 1'b1: Enable ZCD

8:5	UCP_PWM_HIGH_TIME	Sets the PWM high time when under-current protection (UCP) is triggered. 10ns/LSB with -5ns offset. The PWM high time during UCP can be calculated with the following equation: $(UCP\_PWM\_HIGH\_TIME \times 10 - 5) \text{ ns}$
4:0	PWM_MIN_OFF_TIME	Sets the PWM minimum off time. 20ns/LSB with 15ns offset. The PWM minimum off time can be calculated with the following equation: $PWM\_MIN\_OFF\_TIME \times 20 + 15) \text{ ns}$

**MFR\_SLOPE\_ANA\_CTRL (76h)**

This command on page 0 programs the options related to slope compensation.

Command	MFR_SLOPE_ANA_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			X											X	X	
<b>Bits</b>	<b>Bit Name</b>			<b>Description</b>												
13:3:2	RESERVED			Unused. X indicates that writes are ignored and reads are always 0.												
15	PWM_TRI_MODE			Selects the tri-state mode of PWM signal. It is valid for both rails. 1'b0: Hi-Z mode 1'b1: Internally force middle voltage mode												
14	ON/OFF_DLY_CLK_SEL			Selects the clock frequency for rail 1's turn-on delay and turn-off delay counter. The counter is set with PMBus commands TON_DELAY (60h on page 0) and TOFF_DELAY (64h on page 0). See TON_DELAY (60h on page 0) on page 138 and TOFF_DELAY (64h on page 0) on page 140 for more information. 1'b0: 50kHz 1'b1: 20kHz												
12	SLOPE_LEAKAGE_EN			Turns on the slope low-leakage switch after slope counter reaches 1'b0: Disable 1'b1: Enable												
11	SLOPE_INI_EN			Enables initial slope compensation before soft start. 1'b0: Disable initial slope compensation 1'b1: Enable initial slope compensation												
10:5	SLOPE_INI_ISOURCE			Sets the current source value for initial slope compensation. The slope voltage can be calculated with the following equation: $V_{SLOPE\_INI} (\text{mV}) = 0.845 \times SLOPE\_INI\_ISOURCE \times SLOPE\_INI$ Design the initial slope voltage as (1.5 to 2) times the full-phase nominal slope voltage. See register MFR_SLOPE_SR_1P (38h on page 1) for the full-phase slope voltage calculation.												
4	SLOPE_RST_SEL			Selects the slope compensation resetting time. 1'b0: Slope compensation is reset during SLOPE_RST_TIME, defined via the PMBus commands 69h, 6Ah, and 72h [bit[11:6]]. 1'b1: Slope compensation is reset when PWM is high												
1	DVIDUP_PREBIAS_MODE			Sets the PWM behavior at DVID up. 1'b0: Pre-biased mode. All PWM signals enter Hi-Z to Hi individually 1'b1: PWM1 Hi-Z to Hi, other PWMs pull low, then pull high when the individual set signal comes												

0	DCM_EXIT_SLOPE_CTRL	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, slope compensation starts and follows the slew rate defined by the new power state. 1'b0: Maintain the slope current status when the device exits DCM 1'b1: Enable slope current when the device exits DCM to reduce undershoot
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**STATUS\_BYTE (78h)**

This command on page 0 returns 1 byte of information with a summary of the most critical status and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	MTP_BUSY	Live	Reports the live status of the MTP. 1'b0: The MTP is idle. The MTP read and write abilities with the PMBus command are available 1'b1: The MTP is busy. The MTP read and write abilities with the PMBus command are not available
6	OFF	Live	Indicates if rail 1 output is off. This bit is in live mode. It is asserted if rail 1's output is off. VOUT turns off for protections, when EN goes low, or VID = 0. 1'b0: VOUT1 is off 1'b1: VOUT1 is on
5	VOUT_OV_FAULT	Latch	Rail 1 output over-voltage (OV) fault indicator. This bit is set and latched if rail 1 over-voltage protection (OVP) occurs. The CLEARFAULTS (03h) command resets this bit. 1'b0: No VOUT OV fault 1'b1: VOUT OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 1 output over-current (OC) fault indicator. This bit is set and latched if rail 1 over-current protection (OCP) occurs. The CLEARFAULTS (03h) command resets this bit. 1'b0: No output OC fault 1'b1: Output OC fault has occurred
3	VIN_UV_FAULT	Latch	Input under-voltage (UV) fault indicator. This bit is set and latched if an input UV fault occurs. The CLEARFAULTS (03h) command resets this bit. 1'b0: No VIN UV fault 1'b1: VIN UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. This bit is set and latched if TSEN1 senses OT protection or a warning occurs. The CLEARFAULTS (03h) command resets this bit. 1'b0: No OT fault or warning 1'b1: OT fault or warning has occurred

1	CML	Latch	PMBus communication fault indicator. When a fault related to PMBus communications occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No CML fault 1'b1: CML fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_WORD (79h)**

This command on page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information on the fault conditions. The lower byte shares the information with register STATUS\_BYTE (78h).

Command	STATUS_WORD																
Format	Direct																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function							X										STATUS_BYTE(78h)

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Rail 1 VOUT fault and warning indicator. Once an output over-voltage or under-voltage protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No VOUT fault/warning 1'b1: VOUT fault/warning has occurred
14	IOUT/POUT	Live	Rail 1 IOUT/POUT fault and warning indicator. Once an output current fault or warning or output power warning occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No IOUT/POUT fault and warning 1'b1: IOUT/POUT fault or warning has occurred
13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. Once any protection or warning for input voltage, input current, or input power occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No input fault and warning 1'b1: Input fault or warning has occurred
12	PSYS FAULT	Latch	PSYS analog fault or PSYS sense fault indicator. Once a PSYS analog/sense fault occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No PSYS analog/sense fault 1'b1: PSYS analog/sense fault has occurred
11	TSEN2 FAULT	Latch	TSEN2 analog or digital sense fault indicator. Once the TSEN2 analog/sense fault occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No TSEN2 analog/sense fault 1'b1: TSEN2 analog/sense fault has occurred

10	PGOOD	Live	Rail 1 VRRDY status indicator. In VRRDY Intel mode, once VOUT reaches the boot-up voltage level, this bit is set. The bit is reset when VOUT is disabled or in a fault state.  This bit is asserted in VRRDY non-Intel mode, when VOUT exceeds POWER_GOOD_ON and the PGOOD delay time expires. It is de-asserted when VOUT falls below POWER_GOOD_OFF or a fault occurs.
9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Indicator for watchdog block timer overflow. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. The CLEAR_FAULTS command resets this bit.  1'b0: Watchdog timer has not overflowed 1'b1: Watchdog timer has overflowed

**STATUS\_VOUT (7Ah)**

This command on page 0 returns 1 byte of information with the detailed VOUT fault and warning status on rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	X	X				X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 1 VOUT over-voltage (OV) fault indicator. If an output over-voltage protection occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit.  1'b0: No VOUT OV fault 1'b1: VOUT OV fault has occurred
6:5	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
4	VOUT_UV_FAULT	Latch	Rail 1 output under-voltage (UV) fault indicator. This bit is set and latched if rail 1 UV protection occurs. The CLEAR_FAULTS (03h) command resets this bit.  1'b0: No VOUT UV fault 1'b1: VOUT UV fault has occurred
3	VOUT_MAX_MIN_WARNING	Latch	Rail 1 VOUT reaches VOUT_MAX and VOUT_MIN indicator. If the VID value exceeds the value set in VOUT_MAX (24h on page 0) and VOUT_MIN (2Bh on page 0), this bit is set and latched. The CLEAR_FAULTS command resets this bit.  1'b0: VID is between VOUT_MAX and VOUT_MIN 1'b1: VID is above VOUT_MAX or below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

1	LINE_FLOAT	Latch	Rail 1 floating line protection indicator. If a line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. It is in latch mode. The CLEAR_FAULTS (03h) command resets it.  1'b0: No floating line fault 1'b1: Floating line fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_IOUT (7Bh)**

This command on page 0 returns 1 byte of information with the detailed IOUT fault and warning status on rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 1 output over-current (OC) fault indicator. Once output OC protection occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets it.  1'b0: No output OC fault 1'b1: Output OC fault has occurred
6	OC_UV_FAULT	Latch	Rail 1 output over-current (OC) and under-voltage (UV) dual faults indicator. If output OC occurs and the UV comparator is set simultaneously, this bit is set and latched. The CLEAR_FAULTS (03h) command resets it.  1'b0: No output OC and UV faults 1'b1: Output OC has occurred and the UV comparator is set
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_INPUT (7Ch)**

This command on page 0 returns 1 byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X	X			X	X	

Bits	Bit Name	Behavior	Description
7	VIN_OV_FAULT	Latch	Input voltage over-voltage (OV) fault indicator. Once the sensed input voltage exceeds the VIN OV fault limit, this bit is set and latched. The CLEAR_FAULTS (03h) command resets it.  1'b0: No VIN OV fault 1'b1: VIN OV fault has occurred
6:5, 2:1	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

4	VIN_UVLO_LATCH	Latch	Input under-voltage lockout (UVLO) fault indicator. If the sensed input voltage falls below the VIN_OFF (36h) threshold, this bit is set and latched. The CLEAR_FAULTS (03h) command resets it. 1'b0: No VIN UVLO fault 1'b1: VIN UVLO fault has occurred.
3	VIN_UVLO_LIVE	Live	Input under-voltage lockout (UVLO) live indicator. If the sensed input voltage falls below VIN_OFF, this bit is set. Once the sensed input voltage exceeds VIN_ON, this bit is reset. 1'b0: Input voltage is below VIN_OFF (35h) 1'b1: Input voltage exceeds VIN_ON (36h)
0	PIN_WARN	Latch	Input power over-power warning indicator. Once the sensed input power is high enough to assert PSYS_CRI#/PWR_IN_ALERT#, this bit is set and latched until a CLEAR_FAULTS (03h) command resets it.

**STATUS\_TEMPERATURE (7Dh)**

This command on page 0 returns one byte of information with over-temperature (OT) faults and warning conditions.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature (OT) fault indicator. Once the sensed temperature via TSEN1 exceeds the OT fault limit set by MFR OTP_SET (5E on page 1), this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No OT fault 1'b1: OT fault has occurred.
6	TEMP_OT_WARNING	Latch	Over-temperature (OT) warning indicator. Once the sensed temperature via TSEN1 exceeds the OT warning limit set by OT_WARN_LIMIT (51h on page 0), this bit is set and latched. The CLEAR_FAULTS command resets this bit. 1'b0: No OT warning 1'b1: OT warning has occurred
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_CML (7Eh)**

This command on page 0 returns one byte of information with PMBus communication faults.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	<p>Invalid PMBus command indicator. This bit is set and latched if the MP297x receives an unsupported command code. The CLEAR_FAULTS (03h) command resets this bit.</p> <p>1'b0: No invalid PMBus command 1'b1: Invalid PMBus command has been received</p>
6	INVALID_DATA	Latch	<p>Invalid PMBus data indicator. This bit is set and latched if the MP297x receives unsupported data. The CLEAR_FAULTS (03h) command resets this bit.</p> <p>1'b0: No invalid PMBus data 1'b1: Invalid PMBus data has been received</p>
5	PEC_ERROR	Latch	<p>PMBus packet error checking (PEC) fault indicator. The PMBus interface supports the use of the PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP297x during a read transaction, or sent to the MP297x during a write transaction.</p> <p>If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed, and PEC_FAULT is set and latched. The CLEAR_FAULTS (03h) command resets this bit.</p> <p>1'b0: No PEC fault 1'b1: A PEC fault has been detected</p>
4	MTP_CRC_ERROR	Latch	<p>CRC fault indicator. While storing operating memory data into the MTP, the MP297x calculates a CRC code for each bit, and saves the final CRC code into the MTP.</p> <p>While restoring the MTP data to the operating memory, the MP297x re-calculates the CRC code with each bit. The MP297x checks the CRC results when restoration is complete. If the CRC result does not match what was stored, the VR shuts down and sets CRC_FAULT bit. This bit is in latch mode. The CLEAR_FAULTS (03h) command resets this bit.</p> <p>1'b0: No MTP CRC fault 1'b1: An MTP CRC fault has been detected</p>
3	PWD_MATCH	Live	<p>There is write protection for PMBus registers. If enabled, the PMBus registers can only be read. The register MFR_USER_PWD (04h) stores the password. Once the key is matched with MFR_USER_PWD, this bit is set. Otherwise, this bit resets.</p> <p>This bit is in live mode.</p>
2	CML_FLT_TRG	Latch	<p>This bit is set when MTP operation is blocked because the controller is recording a fault to the MTP. This bit is in latch mode. The CLEAR_FAULTS (03h) command resets this bit.</p> <p>1'b0: No MTP operation is blocked 1'b1: MTP operation has been blocked because the controller is recording a fault to the MTP</p>
1	CML_OTHER_FAULTS	Latch	<p>This bit is set if any of the following faults occur during PMBus communication:</p> <ul style="list-style-type: none"> <li>• Sending too few bits</li> <li>• Reading too few bits</li> <li>• Host sends or reads too few bytes</li> <li>• Reading too many bytes</li> </ul> <p>This bit is in latch mode. The CLEAR_FAULTS (03h) command resets this bit.</p>

0	MTP_SIGFAULTS	Latch	While data is being restored from the MTP to the memory, the device first checks the signature register in address 00h of the MTP. If the signature register is 0x1234, the restore process halts immediately and MTP_SIGFAULTS is set. This bit is in latch mode. The CLEAR_FAULTS (03h) command resets this bit.  1'b0: No MTP signature fault 1'b1: An MTP signature fault has occurred
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**DRMOS\_FAULT (80h)**

This command on page 0 provides 1 byte to return the DR莫斯 fault on both rails.

Command	DRMOS_FAULT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	CS_FAULT_TRG_R2				CS_FAULT_TRG_R1			

Bits	Bit Name	Description
7	TSEN1_FAULT_TRG	This bit indicates when the TSEN1 pin voltage exceeds the 2.4V fault indicator. 1'b0: TSEN1 has not exceeded 2.4V 1'b1: TSEN1 has exceeded 2.4V, and a fault has occurred
6:4	CS_FAULT_TRG_R2	CS fault indicators for rail 2. 3'b000: No CS fault is detected on rail 2 3'b001: A CS fault has been detected on rail 2's phase 1 3'b010: A CS fault has been detected on rail 2's phase 2 3'b011: A CS fault has been detected on rail 2's phase 3 3'b100: A CS fault has been detected on rail 2's phase 4 3'b101: A CS fault has been detected on rail 2's phase 5 3'b110: A CS fault has been detected on rail 2's phase 6 3'b111: Unused
3:0	CS_FAULT_TRG_R1	CS fault indicators for rail 1. 4'b0000: No CS fault is detected on rail 1 4'b0001: A CS fault has been detected on rail 1's phase 1 4'b0010: A CS fault has been detected on rail 1's phase 2 4'b0011: A CS fault has been detected on rail 1's phase 3 4'b0100: A CS fault has been detected on rail 1's phase 4 4'b0101: A CS fault has been detected on rail 1's phase 5 4'b0110: A CS fault has been detected on rail 1's phase 6 4'b0111: A CS fault has been detected on rail 1's phase 7 4'b1000: A CS fault has been detected on rail 1's phase 8 4'b1001: A CS fault has been detected on rail 1's phase 9 4'b1010: A CS fault has been detected on rail 1's phase 10 4'b1011: A CS fault has been detected on rail 1's phase 11 4'b1100: A CS fault has been detected on rail 1's phase 12 Others: Unused

**READ\_CS1\_2 (82h)**

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS1 and CS2 pins in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS1_2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_CS2								READ_CS1							

Bits	Bit Name	Description
15:8	READ_CS2	Returns the ADC-sensed voltage on rail 1's CS2 pin in direct format. 12.5mV/LSB.
7:0	READ_CS1	Return the ADC-sensed voltage on rail 1's CS1 pin in direct format. 12.5mV/LSB.

#### READ\_CS3\_4 (83h)

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS3 and CS4 pins in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS3_4															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_CS4								READ_CS3							

Bits	Bit Name	Description
15:8	READ_CS4	Returns the ADC-sensed voltage on rail 1's CS4 pin in direct format. 12.5mV/LSB.
7:0	READ_CS3	Returns the ADC-sensed voltage on rail 1's CS3 pin in direct format. 12.5mV/LSB.

#### READ\_CS5\_6 (84h)

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS5 and CS6 pins in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS5_6															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_CS6								READ_CS5							

Bits	Bit Name	Description
15:8	READ_CS6	Returns the ADC-sensed voltage on rail 1's CS6 pin in direct format. 12.5mV/LSB.
7:0	READ_CS5	Returns the ADC-sensed voltage on rail 1's CS5 pin in direct format. 12.5mV/LSB.

#### READ\_CS7\_8 (85h)

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS7 and CS8 pins in direct format. An internal low-pass filter is used before ADC sensing.

Command	READ_CS7_8															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_CS8								READ_CS7							

Bits	Bit Name	Description
15:8	READ_CS8	Returns the ADC-sensed voltage on rail 1's CS8 pin in direct format. 12.5mV/LSB.
7:0	READ_CS7	Returns the ADC-sensed voltage on rail 1's CS7 pin in direct format. 12.5mV/LSB.

### READ\_CS9\_10 (86h)

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS9 and CS10 in direct format. An internal low-pass filter is used before ADC sensing. The MP2975 does not offer these phases and pins.

<b>Command</b>	READ_CS9_10															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	READ_CS10								READ_CS9							

Bits	Bit Name	Description
15:8	READ_CS10	Returns the ADC-sensed voltage on rail 1's CS10 pin in direct format. 12.5mV/LSB.
7:0	READ_CS9	Returns the ADC-sensed voltage on rail 1's CS9 pin in direct format. 12.5mV/LSB.

### READ\_CS11\_12 (87h)

This command on page 0 returns the ADC-sensed average voltage on rail 1's CS11 and CS12 in direct format. An internal low-pass filter is used before ADC sensing. The MP2975 does not offer these phases and pins.

<b>Command</b>	READ_CS11_12															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	READ_CS12								READ_CS11							

Bits	Bit Name	Description
15:8	READ_CS12	Returns the ADC-sensed voltage on rail 1's CS12 pin in direct format. 12.5mV/LSB.
7:0	READ_CS11	Returns the ADC-sensed voltage on rail 1's CS11 pin in direct format. 12.5mV/LSB.

### READ\_VIN (88h)

This command on page 0 provides 2 bytes to return the sensed input voltage based on the VINSEN1 pin with LINEAR11 format.

<b>Command</b>	READ_VIN																
<b>Format</b>	LINEAR11																
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
<b>Function</b>	1	1	1	1	0	X	X	X	X	READ_VIN							

Bits	Bit Name	Description
15:11	EXP	Fixed to 11110.
10:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	READ_VIN	Returns the sensed input voltage with LINEAR11 format. 0.25V/LSB.

### READ\_IIN (89h)

This command on page 0 returns the sensed input current in LINEAR11 format.

<b>Command</b>	READ_IIN															
<b>Format</b>	LINEAR11															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	1	1	1	1	0	READ_IIN										

Bits	Bit Name	Description
15:11	EXP	Unused. Fixed to 11110.
10:0	READ_IIN	Returns the sensed input voltage in LINEAR11 format. 0.25A/LSB.

### READ\_VOUT (8Bh)

This command on page 0 returns the sensed VOSEN - VORTN voltage on rail 1.

<b>Command</b>	READ_VOUT															
<b>Format</b>	VID or direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the sensed voltage of VOSEN - VORTN. The voltage report is in VID format with VID resolution, or direct format with 1mV resolution. The resolution is determined by bit[15] (e.g. VOUT_PMBUS LSB of the PMBus command MFR_DC_CTRL (59h on page 0)). 1 VID step/LSB when VOUT_PMBUS LSB = 1 1mV/LSB when VOUT_PMBUS LSB = 0

### READ\_IOUT (8Ch)

This command on page 0 returns the sensed output current for rail 1 in direct format.

<b>Command</b>	READ_IOUT															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0	READ_IOUT										

Bits	Bit Name	Description
15:11	EXP	Fixed to 5'b00000.
10:0	READ_IOUT	Returns the sensed output current. 1A/LSB.

### READ\_TEMPERATURE (8Dh)

This command on page 0 returns the sensed temperature on the TSEN1 pin in direct format.

<b>Command</b>	READ_TEMPERATURE															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0	X	X	X								READ_TEMPERATURE

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMPERATURE	Returns the sensed temperature on the TSEN1 pin. 1°C/LSB.

### READ\_IOUT\_PK (90h)

This command on page 0 returns the sensed peak value of rail 1's output current in direct format.

<b>Command</b>	READ_IOUT_PK															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X												READ_IOUT_PK

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_IOUT_PK	Returns the sensed peak output current. Each time the READ_IOUT_PK command is received, the MP297x returns the peak output current and resets the value in the buffer to 0. This starts a new cycle of peak current recording. 0.25A/LSB.

### READ\_POUT\_PK (91h)

This command on page 0 returns rail 1's sensed peak output power in direct format.

<b>Command</b>	READ_POUT_PK															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X													READ_POUT_PK

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	READ_POUT_PK	Returns the sensed peak output power in direct format. Each time the READ_POUT_PK command is received, the MP297x returns the peak output power and resets the value in the buffer to 0. This starts a new cycle of peak-power recording. 0.25W/LSB.

### READ\_TON (94h)

This command on page 0 returns rail 1's PWM on time in real time.

<b>Command</b>	READ_TON															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X	X	READ_TON										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	READ_TON	Returns the real-time PWM on time in direct format. 0.625ns/LSB.

### READ\_TS (95h)

This command on page 0 returns the real-time switching period for rail 1.

<b>Command</b>	READ_TS															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X	X	READ_TS										

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_TS	Returns the real-time switching period in direct format. 1.25ns/LSB.

### READ\_POUT (96h)

This command on page 0 returns rail 1's sensed output power in direct format.

<b>Command</b>	READ_POUT															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0	READ_POUT										

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:0	READ_POUT	Returns the sensed output power in direct format. 1W/LSB.

### READ\_PIN (97h)

This command on page 0 returns rail 1's sensed input power in direct format.

<b>Command</b>	READ_PIN															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0	READ_PIN										

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000
10:0	READ_PIN	Returns the sensed input power in direct format. 1W/LSB.

### PMBUS\_REVISION (98h)

This command on page 0 returns the PMBus revision to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PMBUS_REVISION							

Bits	Bit Name	Description
7:0	PMBUS_REVISION	Always returns 0x33. Indicates that the VR supports PMBUS revision to 1.3. 1.25ns/LSB.

### SVID\_VENDOR\_ID (99h)

This command on page 0 sets the IC's vendor ID for users.

Command	SVID_VENDOR_ID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	VENDOR_ID							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VENDOR_ID	Sets the vendor ID for users. The default is 0x25, which indicates "MPS Corporation" in the Intel vendor list.

### SVID\_PRODUCT\_ID (9Ah)

This command on page 0 sets the IC's product ID for users.

Command	SVID_PRODUCT_ID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	PRODUCT_ID							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	PRODUCT_ID	Sets the product ID for users. The default is 0x75, which indicates "MP2975." 0x75: MP2975 0x72: MP2972 0x76: MP2976 0x78: MP2978

### PRODUCT\_REV\_USER (9Bh)

This command on page 0 provides two bytes for users to track the product revision.

<b>Command</b>	PRODUCT_REV_USER															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	PRODUCT_REV_USER															

Bits	Bit Name	Description
15:0	PRODUCT_REV_UER	Sets the product revision for users.

### CONFIG\_ID (9Dh)

This command on page 0 provides 2 bytes to set the product's 4-digit part number suffix. Contact an MPS FAE to obtain the 4-digit code.

<b>Command</b>	CONFIG_ID															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	CONFIG_ID															

Bits	Bit Name	Description
15:0	CONFIG_ID	Sets the 4-digit part number suffix.

### SVID\_LOT\_CODE\_PROTOCOL\_ID (9Eh)

This command on page 0 provides 2 bytes to record the product lot code and Intel SVID protocol versions for the PSYS rail.

<b>Command</b>	SVID_LOT_CODE_PROTOCOL_ID															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	PROTOCOL_ID_PSYS															

Bits	Bit Name	Description
15:8	PROTOCOL_ID_PSYS	Identifies which PSYS rail the controller supports based on SVID protocol. 01h = VR12.0, IMVP7 02h = VR12.5 03h = VR12.6 04h = VR13.0 10mV VID table 05h = IMVP8 06h = VR12.1 07h = VR13.0 5mV table 08h = IMVP9 09h = VR14 VR 5mV VID table 0Ah = VR14 VR 10mV VID table 0Bh = VR14 VR custom VID table 0Ch = VR14 PSYS device 0Dh = IMVP9 PSYS device
7:0	LOT_CODE	Defines the part's lot code.

**SVID\_PROTOCOL\_ID2 (9Fh)**

This command on page 0 provides 2 bytes to set the Intel SVID protocol versions for rail 1 and rail 2.

<b>Command</b>	SVID_PROTOCOL_ID2															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	PROTOCOL_ID_R2								PROTOCOL_ID_R1							

Bits	Bit Name	Description
15:8	PROTOCOL_ID_R2	Identifies which SVID protocols are supported by rail 2.
7:0	PROTOCOL_ID_R1	Identifies which SVID protocols are supported by rail 1.

**TRIM\_ZCD (B7h)**

The TRIM\_ZCD command on page0 is used to trim ZCD comparator.

<b>Command</b>	TRIM_ZCD															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X								TRIM_ZCD				TRIM_ZCD			

Bits	Bit Name	Description
15:6	RESERVED	Reserved. Fixed to 0.
5:3	TRIM_ZCD	Rail 2: DEC 7:-15mV DEC 6:-10mV DEC 5:-5mV DEC 3:+15mV DEC 2:+10mV DEC 1:+5mV DEC 0:0mV
2:0	TRIM_ZCD	Rail 1: DEC 7:-15mV DEC 6:-10mV DEC 5:-5mV DEC 3:+15mV DEC 2:+10mV DEC 1:+5mV DEC 0:0mV

**MFR\_PRODUCT\_SEL (BFh)**

The MFR\_PRODUCT\_SEL command on page0 sets the product type between MP2972, MP2975, MP2976 and MP2978. It also provides one bit to enable trim registers CRC fault protection.

<b>Command</b>	MFR_PRODUCT_SEL															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Function			PRODUCT
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Bits	Bit Name	Description
15:3	RESERVED	Reserved. Fixed to 0.
2	TRIM_CRC_ERROR_EN	Enable trim registers CRC fault protection. 1'b0: disable trim registers CRC fault to VR shutdown 1'b1: enable trim registers CRC fault to VR shutdown
1:0	PRODUCT_SEL	Select the product type: 2'b11: MP2972 2'b10: MP2975 2'b01: MP2978/MP2976 2'b00: Unused

### READ\_SVID\_AVSBUS\_ADDR (A0h)

This command on page 0 returns the SVID or AVSBus addresses.

Command	READ_SVID_AVSBUS_ADDR															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_ADDR_R2				READ_ADDR_R1			

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:4	READ_ADDR_R2	Returns the SVID or AVSBus addresses for rail 2.
3:0	READ_ADDR_R1	Returns the SVID or AVSBus addresses for rail 1.

### READ\_PIN\_ALERT\_THRESHOLD (A3h)

This command on page 0 returns the SVID-specified input power alert threshold.

Command	READ_PIN_ALERT_THRESHOLD															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	READ_PIN_ALERT_THRESHOLD									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_PIN_ALERT_THRESHOLD	Returns the SVID-specified input power alert threshold. 2W/LSB.

### READ\_VOUT\_MIN (A4h)

This command on page 0 returns rail 1's minimum VOUT based on the most recent VID setting command.

Command	READ_VOUT_MIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	READ_VOUT_MIN								

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT_MIN	Returns the minimum VOUT values based on the most recent VID setting. The returned value is reset to 0x01FF when a set VID command is received from SVID, AVSBus, or the PMBus interface. 1VID/LSB.

### READ\_VOUT\_MAX (A5h)

This command on page 0 returns the rail 1 maximum VOUT based on the most recent VID setting command.

Command	READ_VOUT_MAX																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R							
Function	X	X	X	X	X	X	X	READ_VOUT_MAX															

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT_MAX	Returns the maximum VOUT values based on the most recent VID setting. The returned value is reset to 0 when a set VID command is received from SVID, AVSBus, or PMBus interface. 1VID/LSB.

### SVID\_VOUT\_MAX (C2h)

This command on page 0 sets the initial maximum VID in SVID command that rail 1 supports. If a higher VID code is received, the VR responds to the request with a reject SVID acknowledgement.

Command	SVID_VOUT_MAX																							
Format	VID																							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Function	X	X	X	X	X	X	X	X	SVID_VOUT_MAX															

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	SVID_VOUT_MAX	Sets the maximum VID in SVID command that rail 1 supports. It is in VID format with 5mV or 10mV per step. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). It is effective only when rail 1 is in SVID mode. 1 VID step/LSB.

### SVID\_VR\_TVRRDY\_TOLERANCE1 (C3h)

This command on page 0 sets the Intel SVID specified EN2SVID\_RDY and rail 1's VR\_TOLERANCE.

Command	SVID_VR_TVRRDY_TOLERANCE1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	EN2SVID_RDY								MFR_VR_TOLERANCE							

Bits	Bit Name	Description
15:8	EN2SVID_RDY	This register holds an encoded value that represents the latency between when the VR is enabled to when it is ready for a SVID command. 1μs/LSB.
7:0	VR_TOLERANCE_R1	Data register containing the VR TOB for rail 1 based on board parts (inductor DCR and inductance tolerance, current sense errors, etc.). 1mV/LSB.

### MFR\_MTP\_PMBUS\_CTRL (C5h)

This command on page 0 sets certain configurations for the PMBus interface and MTP operation.

Command	MFR_MTP_PMBUS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	PMBUS_TIMEOUT	Sets PMBus timeout time with:  PMBUS_TIMEOUT x 1.6ms + 1.5ms  If SCL_P remains low for longer than PMBUS_TIMEOUT, the controller resets the PMBus communication and stays idle.
9	PAGE2_CRC_ERROR_EN	Enables page 2's CRC fault protection.  1'b0: Disable page 2 CRC fault to VR shutdown 1'b1: Enable page 2 CRC fault to VR shutdown
8	MTP_SELF_CHECK_EN	Enables the MTP self-check function. When it is enabled, the device starts self-checking once the MTP_SELF_CHECK_START (FAh, page 0 and page 1) command is received.  1'b0: Disable MTP self-check 1'b1: Enable MTP self-check
7	PMBUS_W_PWD_EN	Enable bit for software password protection for the PMBus's write function. The MP297x provides a password to protect registers from writing. If the input password is incorrect, the user cannot write the PMBus registers marked with "W PRT" (see the PMBus Commands/Registers section on page 44).  1'b0: Disable password protection for register writing 1'b1: Enable password protection for register writing
6	PMBUS_RW_PWD_EN	Enable bit for software password protection for the PMBus's read and write functions. The MP297x provides a password to protect registers from both reading and writing. If the input password is incorrect, the users cannot read or write the PMBus registers marked with column "R/W PRT" (see the PMBus Commands/Registers section on page 44).  1'b0: Disable password protection for register reading and writing 1'b1: Enable password protection for register reading and writing
R/W	MTP_BYTE_RW_EN	Enables MTP single-byte read or write via the PMBus when switching the page to 0x28, 0x29, or 0x2A. MTP single-byte write is for engineer use only, such as with ATE programming.  1'b1: Enable MTP single-byte read or write via the PMBus when turning the page to 0x28, 0x29, or 0x2A 1'b0: Disable MTP single-byte read or write via PMBus when turning the page to 0x28, 0x29, or 0x2A

4	STORE_ALL_EN	Enables the device to store all memory data (including the trim register) to the MTP. 1'b0: Disable 1'b1: Enable
3	MTP_ONLINE_COPY_EN	Enables the device to restore the MTP data to memory while the device is on. 1'b0: Forbids restoring the MTP data to the operation memory while the device is on 1'b1: Allows restoring the MTP data to the operation memory while the device is on
2	OPERATION_ALL_CALL_EN	Enables the OPERATION command (01h) to address both rails, regardless of the value of the PAGE (00h) command. This allows the controller to start up both rail 1 and rail 2. 1'b0: The OPERATION command (01h) only addresses a single rail 1'b1: The OPERATION command (01h) addresses both rails
1	FAULT_SAVE_MTP_EN	Enables auto-saving fault statuses to the MTP. When it is enabled, the MP297x saves any fault status in A6h, A7h, A8h, A9h, and AAh on page 1 to the MTP, and page 2A registers C0h, C1h, C2h, C3h, and C4h. When fault auto-save is enabled, the other actions for the MTP, such as store, restore, or single-byte read/write, are blocked. 1'b0: Disable fault status auto-saving to the MTP 1'b1: Enable fault status auto-saving to the MTP
0	PAGE01_CRC_ERROR_EN	Enables page 0 and page 1 CRC fault protection. 1'b0: Disable page 0 and page 1 CRC faults to VR shutdown 1'b1: Enable page 0 and page 1 CRC faults to VR shutdown  While storing memory data to the MTP, the device calculates CRC for all saved bits, and saves the CRC result in the MTP. While restoring the MTP data to the memory, the device calculates CRC for all restored bits. At the end of restoration, the device checks the CRC results saved in the MTP with the calculated CRC. If they do not match, the device reports a CRC fault and sets bit[4] of STATUS_CML (7Eh).

**PWD\_LOCK\_TOG (D0h)**

This command on page 0 locks the PMBus interface from writing or reading. This command provides a method to lock the PMBus register from writing or reading, but can unlock it again by inputting the correct password with PMBus command PWD\_CHECK\_CMD (F8h on page 0). PMBus write or read access is determined by bit[6] and bit[7] of PMBus command MFR\_MTP\_PMBUS\_CTRL (C5h on page 0).

This command is write-only. There is no data byte for this command.

**SVID\_LAST\_CMD\_DATA (E1h)**

This command on page 0 returns the last SVID command and data information for rail 1.

Command	SVID_LAST_CMD_DATA																
Format	Direct																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Function	X	X	X	SVID_LAST_CMD										SVID_LAST_DATA			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

12:8	SVID_LAST_CMD	Last SVID command.
7:0	SVID_LAST_DATA	Data associated with last SVID command.

### SVID\_SECOND\_LAST\_CMD\_DATA (E2h)

This command on page 0 returns the second-to-last SVID command and data information for rail 1.

Command	SVID_SECOND_LAST_CMD_DATA																
Format	Direct																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Function	X	X	X	SVID_SECOND_LAST_CMD										SVID_SECOND_LAST_DATA			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:8	SVID_SECOND_LAST_CMD	Second-to-last SVID command.
7:0	SVID_SECOND_LAST_DATA	Data associated with the second-to-last SVID command.

### MFR\_OVP\_TH\_SET (E5h)

This command on page 0 sets the protection threshold for rail 1 over-voltage protection (OVP1 and OVP2).

Command	MFR_OVP_TH_SET																			
Format	Unsigned binary																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Function	X	X	X	X	X	X	X	X	X	X										

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:3	OVP2_THRESHOLD_SET	Selects the VOUT OVP2 threshold. The OVP2 threshold is determined by OVP2_THRESHOLD and coefficient a and b:  3'b100: OVP2 threshold = VREF + 400mV x a x b 3'b010: OVP2 threshold = VREF + 220mV x a x b 3'b001: OVP2 threshold = VREF + 140mV x a x b Others: Invalid  Coefficient a is determined by the remote-sense amplifier gain (the value of VOUT_SCALE_SET (29h on page 0), bit[11]). a = 1 with unit gain remote-sense amplifier a = 2 with half-gain remote-sense amplifier  Coefficient b is determined by PRT_THRES_DIV_EN (MFRAPS_ADV (56h on page 0), bit[14]). b = 1 when PRT_THRES_DIV_EN = 0 b = 0.5 when PRT_THRES_DIV_EN = 1
2:0	OVP1_THRESHOLD_SET	Sets the OVP1 threshold, which is referred to VOUT_MAX. 50mV/LSB. The OVP1 threshold can be calculated with the following equation:  $VOUT\_MAX + 50mV \times (OVP1\_TH\_SET+1)$

**MFR\_UVP\_SET (E6h)**

This command on page 0 sets the protection threshold for rail 1 under-voltage protection (UVP).

Command	MFR_UVP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X				

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3	UVP_PRT_SEL	Selects the voltage point for VOUT under-voltage protection (UVP). 1'b0: Select VDIFF as the VOUT UVP point 1'b1: Select VFB as the VOUT UVP point
2:0	UVP_THRESHOLD_SET	Sets the VOUT under-voltage protection (UVP) threshold, which is referred to the VID voltage. This threshold is affected by PRT_THRES_DIV_EN (e.g. MFR_AP5_ADV (56h), bit[14]). 50mV/LSB. The UVP threshold can be calculated with the following equation: $\text{VID} - 50\text{mV} \times (\text{UVP\_TH\_SET} + 1) \times a \times b$ Coefficient <i>a</i> is determined by the remote-sense amplifier gain (the value of VOUT_SCALE_SET (29h on page 0), bit[11]). <i>a</i> = 1 with unit gain remote-sense amplifier <i>a</i> = 2 with half-gain remote-sense amplifier Coefficient <i>b</i> is decided by PRT_THRES_DIV_EN (e.g. MFR_AP5_ADV (56h on page 0), bit[14]). <i>b</i> = 1 with PRT_THRES_DIV_EN = 0 <i>b</i> = 0.5 with PRT_THRES_DIV_EN = 1

**MFR\_CAT\_PWR\_IN\_FLT (F0h)**

This command on page 0 sets the system's catastrophic input power fault limit. Once the input power exceeds the threshold, the CAT\_FLT pin asserts high or low. It can be masked by bit[12] of register MFR\_CAT\_FLT\_MASK (B3h on page 1).

Command	MFR_CAT_PWR_IN_FLT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CAT_PWR_IN_FLT_HYS										CAT_PWR_IN_FLT_LIMIT					

Bits	Bit Name	Description
15:10	CAT_PWR_IN_FLT_HYS	Sets the catastrophic input power fault recovery threshold. 8W/LSB.
9:0	CAT_PWR_IN_FLT_LIMIT	Sets the catastrophic input power fault limit. If the real input power exceeds this value, there is a trigger delay (about 3ms), then the CAT_FLT pin is asserted if the corresponding mask bit is disabled. 2W/LSB.

**STORE\_NORMAL\_CODE (F1h)**

This command on page 0 instructs the PMBus device to copy the page 0 and page 1 contents to the matching locations in the MTP, excluding the trim registers. In the copying process, the device calculates

the CRC value for all saved bits in the MTP. The CRC code checks whether the data is valid at the next start-up or system restoration.

This command is write-only. There is no data byte for this command.

#### **RESTORE\_NORMAL\_CODE (F2h)**

This command on page 0 instructs the PMBus device to copy the page 0 and page 1 contents from the MTP and overwrite the matching locations in the operating memory, excluding the trim registers. In this process, the device calculates the CRC value for all restored bits. If the calculated CRC does not match the CRC value saved in MTP, the device reports a CRC error via bit[4] of register STATUS\_CML (7Eh).

#### **PWD\_CHECK\_CMD (F8h)**

This command on page 0 provides 2 bytes for users to input the password and unlock the MTP/PMBus write and read protection. If the password input does not match the value set with PMBus command MFR\_PWD\_USER (02h on page 1), the PMBus commands and MTP will be unable to write or read.

<b>Command</b>	PWD_CHECK_CMD															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
<b>Function</b>	PWD_CHECK_INPUT															

Bits	Bit Name	Description
15:0	PWD_CHECK_INPUT	Command for users to input and check the password value.

#### **CLEAR\_CATFAULTS (FDh)**

This command on page 0 de-asserts the IMON/CAT\_FLT pin. It is effective only when register MFR\_VR\_CONFIG4 (B0h on page 1) is bit[8] = 0.

This command is write-only. There is no data byte for this command.

#### **CLEAR\_STOREFAULTS (FEh)**

This command on page 0 clears the last fault information that is stored into the MTP page2A: C0h, C1h, C2h, C3h, and C4h.

This command is write-only. There is no data byte for this command.

#### **CLEAR\_MTPFAULTS (FFh)**

This command on page 0 clears the MTP faults.

This command is write-only. There is no data byte for this command.

## REGISTER MAP (PAGE 1)

### PAGE (00h)

This command on page 1 provides the ability to configure, control, and monitor all registers, including test mode and the MTP, through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	PAGE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	PAGE	<p>2'b00: Page 0, all commands address rail 1      2'b01: Page 1, all commands address rail 2      Others: Ineffective input</p> <p>Registers page selector.</p> <p>0x00: Page 0, all PMBus commands address the operating registers on page 0      0x01: Page 1, all PMBus commands address the operating registers on page 1      0x02: Page 2, all PMBus commands address the operating multi-configuration registers on page 2      0x03: Page 3, all PMBus commands address the test mode registers      0x28: Page 28, all PMBus commands address the MTP registers that are mapped to the operating registers on page 0      0x29: Page 29, all PMBus commands address the MTP registers that are mapped to the operating registers on page 1      0x2A: Page 2A, all PMBus commands address the MTP registers that are mapped to the operating multi-configuration registers on page 2      Others: Ineffective input</p> <p>Note: MTP_WORD_WR_EN, bit[2] of MFR_MTP_CTRL (C5h), determines whether pages 28, 29, and 2A are accessible or not.</p> <p>MTP_WORD_WR_EN = 0: Pages 28, 29, and 2A are not accessible      MTP_WORD_WR_EN = 1: Pages 28, 29, and 2A are accessible</p>

### OPERATION (01h)

This command on page 1 turns the rail 2 output on/off in conjunction with input from the EN pin, sets the output voltage to the upper or lower MARGIN voltages, and selects the AVSBus mode. Rail 2 stays in the current command operating mode until a subsequent OPERATION command or a state change on the EN pin changes rail 2 to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OPERATION							

Bits	Bit Name	Description
7:0	OPERATION	<p>Operation mode.</p> <p>8'b 00xx xxxx: Hi-Z off  8'b 01xx xxxx: Soft off  8'b 1000 xxxx: Normal on  8'b 1001 xxxx: Margin low  8'b 1010 xxxx: Margin high  8'b 1011 xxxx: AVSBus mode  Others: Unused</p> <p>"x" means not applicable.</p>

### MFR\_PWD\_USER (02h)

This command on page 1 sets the password that protects the PMBus interface from reading or writing. The user can input and check the password with the PMBus command PWR\_CHK\_CMD (F8h on page 0).

Command	MFR_PWD_USER															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Function	PWD_USER															

Bits	Bit Name	Description
15:0	PWD_USER	Sets the password to protect the PMBus interface from reading or writing.

### CLEAR\_FAULTS (03h)

This command on page 1 clears any fault bits in all status registers: STATUS\_BYTE (78h), STATUS\_WORD (79h), STATUS\_VOUT (7Ah), STATUS\_IOUT (7Bh), STATUS\_INPUT (7Ch), STATUS\_TEMPERATURE (7Dh), STATUS\_CML (7Eh), and DRMOS\_FAULT (80h).

This command is write-only. There is no data byte for this command.

### MFR\_VR\_CONFIG6 (04h)

This command on page 1 sets some debugging configurations for the MP297x.

Command	MFR_VR_CONFIG6															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X									X	X		

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	VIN_2_TON_VTH_SEL	Selects the input voltage value for the one-shot on time calculation. Updates when the frequency updates, or when there is a DVID or bios update.  1'b0: Use the READ_VIN (88h) real-time value for $t_{ON}$ calculation 1'b1: The one-shot on time will only update when VIN changes by more than 1V
10	DIS_ALL_PROTECT_EN	1'b0: No action 1'b1: Disable all protections supported by the MP297x

9:8	BG_CHOP_MODE	Selects square wave frequency for bandgap. 2'b00: Keep low 2'b01: 125kHz 2'b10: 250kHz 2'b11: 500kHz
7	VIN_TO_TON_EN	Enable bit for updating $t_{ON}$ when $V_{IN}$ varies $\pm 1V$ or more away from the previous latched $V_{IN}$ . 1'b0: Disable updating $t_{ON}$ with $V_{IN}$ 1'b1: Enable updating $t_{ON}$ with $V_{IN}$  Three conditions can make the controller update $t_{ON}$ : VREF changes, PWM frequency setting changes, and/or real-time $V_{IN}$ varies at least $\pm 1V$ away from the previously latched $V_{IN}$ .
6	PWM_DLL_EN	Enable bit for DLL function. DLL can increase the PWM resolution to 0.625ns/LSB. 1'b0: Disable DLL 1'b1: Enable DLL
5	CAL_WATCH_DOG_EN	Enables watchdog monitor. 1'b0: Disable watchdog monitor 1'b1: Enable watchdog monitor  Note: The monitor value calculation state machine has a watchdog timer. If the watchdog timer overflows, this state machine is reset. Meanwhile, bit[8] of STATUS_WORD (79h on page 0 and page 1) is set.
4:3	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
2	SVID_LOG_SEL	Selects the SVID command record mode in register SVID_LAST_CMD_DATA (E1h on page 0 and page 1) and SVID_2ND_LAST_CMD_DATA (E2h on page 0 and page 1) 1'b0: Record executions and acknowledgements over the last two SVID commands 1'b1: Record any of the last two SVID commands
1	DECAY_OFS_BLOCK	Enable bit for blocking decay behavior (PWMS go to Hi-Z) when VR is slewing to the target voltage after a PMBus VOUT offset command is received. 1'b0: No blocking 1'b1: Block decay behavior after a PMBus VOUT offset command is received
0	HIZ2HI_BLANK_EN	Enable minimum tri-state time constraint when PWM goes from tri-state to high state. The minimum tri-state time is set by PWM_MIN_TIME1 (74h on page 0 and page 1), bit[5:0]. 1'b0: Enable minimum tri-state time constraint when PWM goes from tri-state to high state 1'b1: Disable minimum tri-state time constraint when PWM goes from Hi-Z to high

### MFR\_APS\_LEVEL\_1P (06h)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 1-phase.

Command	MFR_APS_LEVEL_1P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_1P								DROP_LEVEL_DCM							

Bits	Bit Name	Description
15:8	DROP_LEVEL_1P	Sets the rail 1 auto phase-shedding current threshold to 1-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_DCM	Set the rail 1 auto phase-shedding current threshold to 1-phase DCM. 1A/LSB.

#### MFRAPS\_LEVEL\_23P (07h)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 3-phase and 2-phase operation.

Command	MFRAPS_LEVEL_23P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_3P								DROP_LEVEL_2P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_3P	Sets the rail 1 auto phase-shedding current threshold to 3-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_2P	Sets the rail 1 auto phase-shedding current threshold to 2-phase CCM. 1A/LSB.

#### MFRAPS\_LEVEL\_45P (08h)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 5-phase and 4-phase.

Command	MFRAPS_LEVEL_45P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_5P								DROP_LEVEL_4P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_5P	Sets the rail 1 auto phase-shedding current threshold to 5-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_4P	Sets the rail 1 auto phase-shedding current threshold to 4-phase CCM. 1A/LSB.

#### MFRAPS\_HYS\_R1 (09h)

This command on page 1 sets the rail 1 auto phase-shedding current hysteresis.

Command	MFRAPS_HYS_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	MFRAPS_HYS		

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	MFRAPS_HYS	Sets the current hysteresis between phase-shedding and phase-adding. It prevents back and forth phase-shedding when APS is enabled. 1A/LSB.

### MFR\_AP\_S\_LEVEL\_67P (0Ah)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 7-phase or 6-phase, or it sets the rail 2 auto phase-shedding current to 5-phase or 4-phase shedding. The MP2975 does not offer 5-phase operation on rail 2.

Command	MFR_AP_S_LEVEL_67P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_7P								DROP_LEVEL_6P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_7P_R1 DROP_LEVEL_4P_R2	Sets the rail 1 auto phase-shedding current threshold to 7-phase CCM, or the rail 2 auto phase-shedding current threshold to 4-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_6P_R1 DROP_LEVEL_5P_R2	Sets the rail 1 auto phase-shedding current threshold to 6-phase CCM, or the rail 2 auto phase-shedding current threshold to 5-phase CCM. 1A/LSB.

### MFR\_AP\_S\_LEVEL\_89P (0Bh)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 9-phase or 8-phase, or the rail 2 auto phase-shedding current threshold to 3-phase or 2-phase. The MP2975 does not offer 9-phase operation on rail 1.

Command	MFR_AP_S_LEVEL_89P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_9P_R1/DROP_LEVEL_2P_R2								DROP_LEVEL_8P_R1/DROP_LEVEL_3P_R2							

Bits	Bit Name	Description
15:8	DROP_LEVEL_9P_R1 DROP_LEVEL_2P_R2	Sets the rail 1 auto phase-shedding current threshold to 9-phase CCM, or the rail 2 auto phase-shedding current threshold to 2-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_8P_R1 DROP_LEVEL_3P_R2	Sets the rail 1 auto phase-shedding current threshold to 8-phase CCM, or the rail 2 auto phase-shedding current threshold to 3-phase CCM. 1A/LSB.

### MFR\_AP\_S\_LEVEL\_1011P (0Ch)

This command on page 1 sets the rail 1 auto phase-shedding current threshold to 12-phase or 11-phase, or the rail 2 auto phase-shedding current threshold to 1-phase. The MP2975 does not offer 11-phase or 12-phase operation on rail 1.

Command	MFR_AP_S_LEVEL_89P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROP_LEVEL_11P_R1/DROP_LEVEL_DCM_R2								DROP_LEVEL_10P_R1/DROP_LEVEL_1P_R2							

Bits	Bit Name	Description
15:8	DROP_LEVEL_11P_R1 DROP_LEVEL_DCM_R2	Sets the rail 1 auto phase-shedding current threshold to 11-phase CCM, or the rail 2 auto phase-shedding current threshold to 1-phase DCM. 1A/LSB.
7:0	DROP_LEVEL_10P_R1 DROP_LEVEL_1P_R2	Sets the rail 1 auto phase-shedding current threshold to 10-phase CCM, or the rail 2 auto phase-shedding current threshold to 1-phase CCM. 1A/LSB.

### MFR\_APS\_HYS\_R2 (0Dh)

This command on page 1 sets the rail 2 auto phase-shedding current hysteresis.

<b>Command</b>	MFR_APS_HYS_R2															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MFR_APS_HYS

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	MFR_APS_HYS	Sets the current hysteresis between 1-phase shedding and phase-adding. It prevents back and forth phase-shedding when APS is enabled. 1A/LSB.

### MFR\_FS\_LIMIT\_12P (0Eh)

This command on page 1 sets the FS\_LIMIT threshold during 1-phase and 2-phase operation to detect fast load insertion and exit phase-shedding (for rail 1 only).

<b>Command</b>	MFR_FS_LIMIT_12P															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	FS_LIMIT_2P_R1								FS_LIMIT_1P_R1							

Bits	Bit Name	Description
15:8	FS_LIMIT_2P_R1	Sets the PWM interval, after which the device exits phase-shedding during 2-phase operation. If the interval between two phases is less than 2 x FS_LIMIT_2P, then counter will increase by 1. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_1P_R1	Sets the PWM1 off-time threshold to exit phase-shedding. If the PWM1 off time (after excluding MIN_OFF_TIME) is less than FS_LIMIT_1P, then counter will increase by 1. Figure 29 shows the definition of FS_LIMIT_1P. It is effective both for DCM and CCM. 10ns/LSB.

### MFR\_FS\_LIMIT\_34P (0Fh)

This command on page 1 sets FS\_LIMIT during 3-phase and 4-phase operation to detect fast load insertion and exit phase-shedding (for rail 1 only).

<b>Command</b>	MFR_FS_LIMIT_34P															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	FS_LIMIT_4P_R1								FS_LIMIT_3P_R1							

Bits	Bit Name	Description
15:8	FS_LIMIT_4P_R1	Sets the PWM interval, after which the device exits phase-shedding during 2-phase operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_3P_R1	Sets the PWM interval, after which the device exits phase-shedding if rail 1 is set for 3-phase operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

**MFR\_PROTECT\_DELAY\_TIME (10h)**

This command on page 1 sets the delay time to retry start-up after a protection occurs.

Command	MFR_PROTECT_DELAY_TIME								
Format	Unsigned binary								
Bit	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	PROTECT_DELAY_TIME							

Bits	Bit Name	Description
6:0	PROTECT_DELAY_TIME	Sets the delay time to retry start-up after a protection occurs. 100µs/LSB.

**MFR\_FS\_LIMIT\_56P (11h)**

This command on page 1 sets FS\_LIMIT during 5-phase and 6-phase operation to detect fast load insertion and exit phase-shedding (for rail 1 only).

Command	MFR_FS_LIMIT_56P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FS_LIMIT_6P_R1								FS_LIMIT_5P_R1							

Bits	Bit Name	Description
15:8	FS_LIMIT_6P_R1	Sets the PWM interval after which the device exits phase-shedding during 6-phase operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_5P_R1	Sets the PWM interval after which the device exits phase-shedding during 2-phase operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

**MFR\_FS\_LIMIT\_78P (12h)**

This command on page 1 sets FS\_LIMIT to detect fast load insertion and when to exit phase-shedding. It is active for rail 1 during 7-phase and 8-phase operation, and is active for rail 2 during 5-phase or 6-phase operation. The MP2975 does not offer 5-phase or 6-phase operation on rail 2.

Command	MFR_FS_LIMIT_78P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FS_LIMIT_8P_R1/ FS_LIMIT_5P_R2								FS_LIMIT_7P_R1/ FS_LIMIT_6P_R2							

Bits	Bit Name	Description
15:8	FS_LIMIT_8P_R1 FS_LIMIT_5P_R2	Sets the PWM interval, after which the device exits phase-shedding during 8-phase operation for rail 1, and 5-phase operation for rail 2. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_7P_R1 FS_LIMIT_6P_R2	Sets the PWM interval, after which the device exits phase-shedding during 7-phase rail 1 operation and 6-phase rail 2 operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

### MFR\_FS\_LIMIT\_910P (13h)

This command on page 1 sets the PWM interval threshold to detect fast load insertion and exit phase-shedding. It is active for 9-phase and 10-phase operation for rail 1, and 3-phase or 4-phase operation for rail 2. The MP2975 does not offer 9-phase or 10-phase operation on rail 1.

Command	MFR_FS_LIMIT_910P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FS_LIMIT_10P_R1/ FS_LIMIT_3P_R2								FS_LIMIT_9P_R1/ FS_LIMIT_4P_R2							

Bits	Bit Name	Description
15:8	FS_LIMIT_10P_R1 FS_LIMIT_3P_R2	Sets the PWM interval, after which the device exists phase-shedding during 10-phase operation for rail 1, or 3-phase operation for rail 2. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_9P_R1 FS_LIMIT_4P_R2	Sets the PWM interval, after which the device exists phase-shedding during 9-phase operation for rail 1, or 4-phase operation for rail 2. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

### MFR\_FS\_LIMIT\_1112P (14h)

This command on page 1 sets the PWM interval threshold to detect fast load insertion and exit phase-shedding. It is active for rail 1 during 11-phase or 12-phase operation, or for rail 2 during 1-phase or 2-phase operation. The MP2975 does not offer 11-phase or 12-phase operation on rail 1.

Command	MFR_FS_LIMIT_1112P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	FS_LIMIT_12P_R1/ FS_LIMIT_1P_R2								FS_LIMIT_11P_R1/ FS_LIMIT_2P_R2							

Bits	Bit Name	Description
15:8	FS_LIMIT_12P_R1 FS_LIMIT_1P_R2	Sets the PWM interval, after which the device exists phase-shedding during rail 1 12-phase operation or rail 2's PWM1 off time threshold. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. Figure 29 shows the definition of FS_LIMIT_1P. 5ns/LSB for rail 1 12-phase operation. 10ns/LSB for rail 2's PWM1 off-time threshold.
7:0	FS_LIMIT_11P_R1 FS_LIMIT_2P_R2	Sets the PWM interval, after which the device exists phase-shedding during rail 1 11-phase operation or rail 2 2-phase operation. Figure 30 shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

### STORE\_USER\_CODE (17h)

This command on page 1 instructs the PMBus device to copy the operating memory contents for page 0, page 1, and page 2 to their matching locations in the MTP (except for internal trim registers). During the copying process, the device calculates two sets of CRC codes for all saved bits and saves the corresponding CRC results in the MTP. Two sets of CRC codes include one set for user configurations on page 0 and page 1, and one set for multi-configuration on page 2. The CRC codes are used to ensure the data copied from the MTP is valid, at the next power-up or restore.

This command is write-only. There is no data byte for this command.

### RESTORE\_USER\_CODE (18h)

This command on page 1 instructs the PMBus device to copy the MTP contents for page 0, page 1 and page 2 and overwrite the matching locations in the operating memory. Trim registers are not overwritten

by RESTORE\_USER\_CODE. During this process, the device calculates CRC values for all restored bits. If the calculated CRC value does not match the CRC values saved in the MTP, the device reports a CRC error via the bit[4] of register STATUS\_CML (7Eh). CRC error protection is enabled by bit[0] and bit[9] of MFR\_MTP\_CTRL (C5h on page 0). After power-on reset (POR), the device triggers the memory copying operation from the MTP.

The RESTORE\_USER\_CODE command cannot be sent while the device is outputting power. If this is attempted, the command will be ignored.

This command is write-only. There is no data byte for this command.

#### **MFR\_SLOPE\_TRIM1 (1Ah)**

When the DC loop is disabled, the actual VOUT voltage with the MP297x can be calculated with Equation (21):

$$V_{\text{OUT}} = \frac{V_{\text{REF}} - V_{\text{SLOPE}}}{K_v} + \frac{\Delta V_{\text{OUT}}}{2} \quad (21)$$

Where  $V_{\text{REF}}$  is the reference voltage (in V),  $V_{\text{SLOPE}}$  is the slope voltage (in V),  $\Delta V_{\text{OUT}}$  is the output voltage ripple (in V), and  $K_v$  is the output voltage divider, which may be caused by the remote-sense amplifier sense gain or the external VOUT resistive divider.

The MP297x provides reference voltage trim (VTRIM) to keep the output voltage close to the design target without DC loop calibration. It is implemented by adding a negative offset over the reference voltage. In design, VTRIM is the voltage shift caused by  $V_{\text{SLOPE}}$  and the output voltage ripple. When SVID sets a PS command, or when auto phase-shedding is enabled, the reference voltage trim also makes the DC loop output constant between different phases. This improves the load transient response between different power states.

This command on page 1 trims the output voltage during 2-phase and 1-phase CCM, or during 1-phase DCM for rail 1.

Command	MFR_SLOPE_TRIM1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	VTRIM_2P_R1										VTRIM_1P_R1				VTRIM_DCM_R1

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_2P_R1	Sets the VOUT trim for rail 1's 2-phase operation. 2.35mV/LSB.
9:5	VTRIM_1P_R1	Sets the VOUT trim for rail 1's 1-phase CCM operation. 2.35mV/LSB.
4:0	VTRIM_DCM_R1	Sets the VOUT trim for rail 1's 1-phase DCM operation. 2.35mV/LSB.

#### **MFR\_PS34\_EXIT\_LAT (1Bh)**

This command on page 1 sets the latency to exit PS3 and PS4. It is valid for both rails.

Command	MFR_PS34_EXIT_LAT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PS4_EXIT_LAT										PS3_EXIT_LAT					

Bits	Bit Name	Description
15:12	PS4_EXIT_LAT_EXP	Sets the latency to exit PS4. It is valid for both rails. The PS4 latency time can be calculated with the following equation: $\text{PS4 Latency time} = \text{PS4\_EXIT\_LAT\_K} \times 2^{(\text{PS4\_EXIT\_LAT\_EXP}-4)}$
11:8	PS4_EXIT_LAT_K	
7:4	PS3_EXIT_LAT_EXP	Sets the latency to exit PS3. It is valid for both rails. The PS3 latency time can be calculated with the following equation:
3:0	PS3_EXIT_LAT_K	$\text{PS3 Latency time} = \text{PS3\_EXIT\_LAT\_K} \cdot 2^{(\text{PS3\_EXIT\_LAT\_EXP}-4)}$

### MFR\_SLOPE\_TRIM2 (1Ch)

This command on page 1 trims the output voltage during 5-phase, 4-phase, and 3-phase CCM for rail 1.

Command	MFR_SLOPE_TRIM2																
Format	Unsigned binary																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	VTRIM_5P_R1						VTRIM_4P_R1						VTRIM_3P_R1			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_5P_R1	Sets the VOUT trim for rail 1's 5-phase operation. 2.35mV/LSB.
9:5	VTRIM_4P_R1	Sets the VOUT trim for rail 1's 4-phase operation. 2.35mV/LSB.
4:0	VTRIM_3P_R1	Sets the VOUT trim for rail 1's 3-phase operation. 2.35mV/LSB.

### MFR\_SLOPE\_TRIM3 (1Dh)

This command on page 1 trims the output voltage during 7-phase or 6-phase CCM for rail 1, or during 6-phase CCM for rail 2. The MP2975 does not offer 6-phase operation on rail 2.

Command	MFR_SLOPE_TRIM3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VTRIM_7P_R1/VTRIM_6P_R2						VTRIM_6P_R1			

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:5	VTRIM_7P_R1 VTRIM_6P_R2	Sets the VOUT trim for rail 1's 7-phase operation, or rail 2's 6-phase operation. 2.35mV/LSB.
4:0	VTRIM_6P_R1	Sets the VOUT trim for rail 1's 6-phase operation. 2.35mV/LSB.

### MFR\_SLOPE\_TRIM4 (1Eh)

This command on page 1 trims the output voltage during 12-phase and 11-phase CCM for rail 1, or during 2-phase and 1-phase CCM for rail 2. The MP2975 does not offer 11-phase or 12-phase operation on rail 1.

Command	MFR_SLOPE_TRIM4																
Format	Unsigned binary																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	VTRIM_11P_R1/VTRIM_2P_R2						VTRIM_12P_R1/VTRIM_1P_R2						VTRIM_DCM_R2			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_11P_R1 VTRIM_2P_R2	Sets the VOUT trim for rail 1's 11-phase operation, or rail 2's 2-phase operation. 2.35mV/LSB.
9:5	VTRIM_12P_R1 VTRIM_1P_R2	Sets the VOUT trim for rail 1's 12-phase operation, or rail 2's 1-phase CCM operation. 2.35mV/LSB.
4:0	VTRIM_DCM_R2	Sets the VOUT trim for rail 2's 1-phase DCM operation. 2.35mV/LSB.

### MFR\_SLOPE\_TRIM5 (1Fh)

This command on page 1 trims the output voltage during 10-phase, 9-phase, and 8-phase CCM for rail 1, or during 5-phase, 4-phase, and 3-phase CCM for rail 2. The MP2975 does not offer 10-phase or 9-phase operation on rail 1, and does not offer 5-phase operation on rail 2.

Command	MFR_SLOPE_TRIM5																
Format	Unsigned binary																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	VTRIM_8P_R1/VTRIM_5P_R2				VTRIM_9P_R1/VTRIM_4P_R2				VTRIM_10P_R1/VTRIM_3P_R2							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_8P_R1 VTRIM_5P_R2	Sets the VOUT trim for rail 1's 8-phase operation, or rail 2's 5-phase operation. 2.35mV/LSB.
9:5	VTRIM_9P_R1 VTRIM_4P_R2	Sets the VOUT trim for rail 1's 9-phase operation, or rail 2's 4-phase operation. 2.35mV/LSB.
4:0	VTRIM_10P_R1 VTRIM_3P_R2	Sets the VOUT trim for rail 1's 10-phase operation, or rail 2's 3-phase operation. 2.35mV/LSB.

### VOUT\_COMMAND (21h)

This command on page 1 sets the rail 2 reference voltage VID at PMBus override mode.

Command	VOUT_COMMAND																
Format	VID																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	X	X	X	X	X	X	VOUT_COMMAND									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_COMMAND	Sets the reference voltage VID during PMBUS override mode. It is in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

**MFR\_IDROOP\_OFFSET (22h)**

This command on page 1 instructs the device to fine-tune the rail 2 output voltage.

<b>Command</b>	MFR_IDROOP_OFFSET															
<b>Format</b>	Direct, two's complement															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	IDROOP_OFFSET

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	IDROOP_OFFSET	Sets the droop current offset. 0.81µA/LSB.  This value is in two's complement format. Bit[5] is the sign bit. The list below shows the binary data and real-world current value:  6'b 00 0000: 0 6'b 00 0001: 0.81µA 6'b 01 1111: 25.11µA 6'b 10 0000: -25.92µA 6'b 10 0001: -25.11µA 6'b 11 1111: -0.81µA

**VOUT\_MAX (24h)**

This command on page 1 sets the maximum reference voltage of the rail 2 VID-DAC, which is used to set the maximum output voltage. When an external resistive divider is applied, the maximum voltage is clamped to VOUT\_MAX / K<sub>R</sub>. K<sub>R</sub> is the dividing ratio of the external resistive divider.

<b>Command</b>	VOUT_MAX															
<b>Format</b>	VID															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VOUT_MAX

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MAX	Sets the maximum reference voltage of the VID-DAC in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

**VOUT\_MARGIN\_HIGH (25h)**

This command on page 1 sets the reference voltage when OPERATION (01h) is set to margin high on rail 2.

<b>Command</b>	VOUT_MARGIN_HIGH															
<b>Format</b>	VID															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VOUT_MARGIN_HIGH

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MARGIN_HIGH	Sets the margin high reference voltage level in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step /LSB.

**VOUT\_MARGIN\_LOW (26h)**

This command on page 1 sets the reference voltage when OPERATION (01h) is set to margin low on rail 2.

Command	VOUT_MARGIN_LOW																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_MARGIN_LOW															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MARGIN_LOW	Sets the margin low reference voltage level in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

**VOUT\_TRANSITION\_RATE (27h)**

This command on page 1 sets the rail 2 boot-up slew rate during SVID, PMBus, and PVID mode, and the dynamic VID transition slew rate in PMBus and PVID mode. It also sets the AVSBus initial DVID slew rate.

Command	VOUT_TRANSITION_RATE																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	VOUT_TRANS_CNT															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRANS_CNT	<p>Sets the rail 2 dynamic VID transition slew rate in PMBus and PVID mode, the initial DVID slew rate in AVSBus mode, and the start-up VID transition slew rate during SVID, PMBus, and PVID mode. 100ns/LSB.</p> <p>The PMBus and PVID DVID slew rate can be calculated with the following equation:</p> $\text{DVID\_SR(mV/\mu s)} = \frac{\text{VID\_STEP(mV)}}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu s)}$ <p>The AVSBus initial DVID slew rate can be calculated with the following equation:</p> $\text{DVID\_SR(mV/\mu s)} = \frac{10(\text{mV})}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu s)}$ <p>If bit[8] of 68h on page 1(SS_SR_SEL) is set to 1'b0, the non-AVSBus start-up slew rate can be calculated with the following equation:</p>

		$\text{BOOT\_SR}(\text{mV}/\mu\text{s}) = \frac{\text{VID\_STEP}(\text{mV})}{\text{VOUT\_TRANS\_CNT} \times 0.1(\mu\text{s})}$
Where VID_STEP is 5mV or 10mV, which is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2) for rail 2, and VOUT_TRANS_CNT is the decimal value defined in VOUT_TRNS_RATE (27h).		

### VOUT\_SENSE\_SET (29h)

This command on page 1 sets the rail 2 VOUT sense-related options.

Command	VOUT_SENSE_SET															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													VOUT_SCALE

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	DC_LOOP_SNS_SEL	Sets the sensing point for VOUT DC loop calibration. 1'b0: VFB signal 1'b1: VDIFF signal
11	VDIFF_GAIN_SEL	Selects the gain of the remote-sense amplifier. 1'b0: Unit gain. VOUT is limited to 1.6V 1'b1: Half-gain
10:9	VDIFF_VFB_ADC_GAIN	ADC buffer sensing gain selector for VDIFF and VFB. 2'b00: Half-gain 2'b01: Unit gain 2'b10 and 2'b11: Three-quarter gain  Note: Set the ADC-sense gain to 2'b01 when the remote-sense amplifier gain is set to half-gain, or the device will not work correctly.
8:0	VOUT_SCALE	Sets the rail 1 VREF to VOUT dividing ratio when an external resistive divider is used. VREF ranges from 0.25 (if bit[8] of 68h page 1 (SS_SR_SEL) is 1'b0) to 1.6V. Equation (12) shows how to calculate VOUT_SCALE.

### VOUT\_MIN (2Bh)

This command on page 1 instructs the device to limit the rail 2 minimum output voltage during PMBus, PVID, and AVSBus mode. If the output voltage decoded from the AVSBus and PMBus interface or set by the PVID registers falls below what is set by VOUT\_MIN (2Bh), the output voltage is clamped to VOUT\_MIN. If an external resistive divider is applied on VOSEN, the minimum output voltage is clamped to VOUT\_MIN / K<sub>R</sub>. K<sub>R</sub> is the dividing ratio of the divider.

Command	VOUT_MIN															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									VOUT_MIN

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

8:0	VOUT_MIN	Sets the minimum VID in rail 2's PMBus and AVSBus modes. Any VID below this value is clamped to VOUT_MIN. It is in VID format with 5mV or 10mV per step. The rail 2 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2).
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### MFR\_VR\_CONFIG3 (35h)

This command on page 1 sets some configurations for the MP297x.

Command	MFR_VR_CONFIG3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X						

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5	PS4_VRRDY_SEL	Selects PS4 VRRDY signal behavior. 1'b0: The VRRDY behavior follows SVID Multi VR register (34h) bit[0] 1'b1: The VRRDY remains asserted when the device enters PS4
4	LOW_PWR_MODE_EN	Enables low-power mode. 1'b0: Regular-power mode. In regular-power mode, the MTP and PMBus are live when both EN1 and EN2 are low. EN enables the output power. 1'b1: Enable low-power mode. In low-power mode, the MTP is off and the device consumes about 120µA to minimize power dissipation when both EN1 and EN2 are low.
3	PSYS_DAC_SEL	Selects the 8-bit digital input of PSYS DAC. 1'b0: The digital input of PSYS DAC is from the SVID command (SVID PSYS critical threshold register, 4Ah, PSYS_CR_LVL_H) 1'b1: The digital input of PSYS DAC is set by bit[7:0] of register MFR_PSYS_LEVEL (B4h on page 1).
2	PWR_IN_ALT_MODE	Selects the PSYS_CRIT#/PWR_IN_ALERT# assertion mode 1'b0: Selects the PWR_IN_ALERT# signal to assert PSYS_CRIT#/PWR_IN_ALERT# 1'b1: Selects the PSYS_CRIT# signal to assert PSYS_CRIT#/PWR_IN_ALERT#
1	INTEL_SPEC	Selects the Intel spec that the VR executes. 1'b0: VR13.HC (or earlier versions) 1'b1: VR14
0	INTEL_RPT_MODE	Selects the bit for SVID high-precision and normal precision telemetry mode. 1'b0: Normal precision telemetry mode (8-bit width telemetry data) 1'b1: High-precision telemetry mode (16-bit width telemetry data)

### MFR\_VIN\_SCALE\_OFFSET (36h)

This command on page 1 sets the resistive divider ratio for input voltage sensing. It also sets the input voltage-sensing offset.

Command	MFR_VIN_SCALE_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VIN_SCALE_LOOP								VIN_SENSE_OFFSET							

Bits	Bit Name	Description
15:8	VIN_SCALE_LOOP	Sets the input voltage sensing scale, calculated with the following equation: $\text{VIN\_SENSE\_SCALE} = \frac{2557.5 \times V_{\text{INSEN}}}{V_{\text{IN}}} = \frac{2557.5 \times R_{\text{BOTTOM}}}{R_{\text{TOP}} + R_{\text{BOTTOM}}}$ Where $R_{\text{TOP}}$ and $R_{\text{BOTTOM}}$ are the resistor dividers on the VINSEN pin.
7:0	VIN_SENSE_OFFSET	Sets the input voltage sensing offset. It is in two's complement format. Bit[7] is the sign bit. $V_{\text{IN\_OFFSET}} = \frac{1.6 \times \text{VIN\_SENSE\_OFFSET} \times (R_{\text{TOP}} + R_{\text{BOTTOM}})}{1023 \times R_{\text{BOTTOM}}}$ Where $V_{\text{IN\_OFFSET}}$ is the actual input voltage sensing offset on the input voltage, and $R_{\text{TOP}}$ and $R_{\text{BOTTOM}}$ are the resistor dividers on the VINSEN pin.

### MFR\_SLOPE\_SR\_1P (38h)

Slope compensation provides enough noise immunity for PWM generation to make the PWM switches stable on the MP297x. Slope compensation is generated by a PMBus-configurable current source and a PMBus-configurable capacitor. The MP297x provides a slope voltage programming command for any phase count operation. The MFR\_SLOPE\_SR\_4P command on page 0 provides 2 bytes to program the slope compensation for 4-phase operation. It is for rail 1 only.

This command on page 1 provides 2 bytes to program the slope compensation for 1-phase operation. It is for rail 1 only.

Command	MFR_SLOPE_SR_1P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X							CURRENT_SOURCE

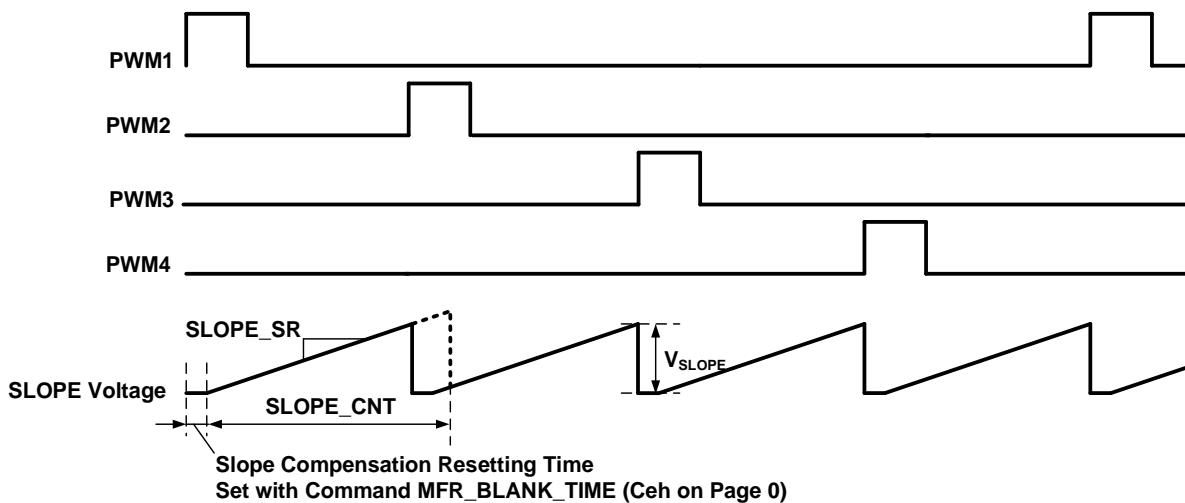
Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25µA/LSB.

CCM operation can use Equation (22) to calculate the slope slew rate. The values for CURRENT\_SOURCE and CAP are configured through different registers.

$$\text{SLOPE\_SR}_{\text{NP}} = 16892 \times \frac{\text{CURRENT\_SOURCE}}{(16 - \text{CAP})} \quad (22)$$

Where SLOPE\_SR<sub>NP</sub> is the slope voltage slew rate in N-phase CCM (in V/s), and N is the phase count, which ranges from 1 to 12.

Figure 31 shows a slope voltage curve in 4-phase CCM.



**Figure 31: Slope Voltage in 4-Phase CCM**

The slope voltage amplitude ( $V_{SLOPE}$ ) can be calculated with Equation (23):

$$V_{SLOPE\_NP} = SLOPE\_SR_{@NP} \times \left( \frac{1}{N \times f_{SW}} - t_{RST} \right) \quad (23)$$

Where,  $V_{SLOPE\_NP}$  is the slope voltage of N-phase CCM (in V), N is the phase count (which ranges from 1 to 12),  $SLOPE\_SR_{@NP}$  is the slope voltage slew rate calculated with Equation (23),  $f_{SW}$  is the single-phase switching frequency set with command MFR\_FS (5Ch on page 0 and page 1) (in Hz), and  $t_{RST}$  is the slope compensation resetting time as set with command MFR\_BLANK\_TIME (69h, 6Ah, and 72h on page 0 and page 1) (in s).

In general design, a slope voltage amplitude ( $V_{SLOPE}$ ) of 20mV to 40mV is used to cover all potential  $t_{ON}$ , L, and  $C_{OUT}$  variation. Lower slope voltages lead to faster load transient response, while higher slope voltages lead to better noise immunity (less PWM jittering).

#### MFR\_SLOPE\_CNT\_1P (39h)

This command on page 1 sets the rail 1 slope voltage clamp time during 1-phase operation. The clamp time limits the slope voltage when the switching off-time is too long (e.g. DCM operation or output load release transient). It should cover the regular PWM switching off-time (see Figure 29). The slope voltage is clamped once the clamp timer expires, which does not stop slope compensation.

For adequate time margins for slope compensation, it is recommended to design the slope clamp timer to be the 130% of the switching off-time, estimated with Equation (24):

$$t_{\text{SLOPE\_CLAMP}} = 1.3 \times \left( \frac{1}{N \times f_{\text{SW}}} - t_{\text{RST}} \right) \quad (24)$$

Where  $t_{\text{SLOPE\_CLAMP}}$  is the slope clamping timer (in s),  $f_{\text{SW}}$  is the single-phase switching frequency set with command MFR\_FS (5Ch on page 0 and page 1) (in Hz), and  $t_{\text{RST}}$  is the slope compensation resetting time as set with command MFR\_BLANK\_TIME (69h, 6Ah, and 72h on page 0 and page 1) (in s).

Command	MFR_SLOPE_CNT_1P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time. 5ns/LSB.

### MFR\_SLOPE\_SR\_2P (3Ah)

This command on page 1 provides 2 bytes to program the slope compensation for 2-phase operation for rail 1.

Command	MFR_SLOPE_SR_2P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets current-source value for slope compensation. 0.25μA/LSB.

### MFR\_SLOPE\_CNT\_2P (3Bh)

This command on page 1 sets the slope voltage clamp time during 2-phase operation for rail 1.

Command	MFR_SLOPE_CNT_2P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time. 5ns/LSB.

**MFR\_SLOPE\_SR\_3P (3Ch)**

This command on page 1 provides 2 bytes to program the slope compensation for 3-phase operation for rail 1.

Command	MFR_SLOPE_SR_3P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									
																CURRENT_SOURCE

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets current-source value for slope compensation. 0.25μA/LSB.

**MFR\_SLOPE\_CNT\_3P (3Dh)**

This command on page 1 sets the slope voltage clamp time during 3-phase operation for rail 1.

Command	MFR_SLOPE_CNT_3P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time. 5ns/LSB.

**MFR\_SLOPE\_SR\_4P (3Eh)**

This command on page 1 provides 2 bytes to program the slope compensation for 4-phase operation for rail 1.

Command	MFR_SLOPE_SR_4P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

**MFR\_SLOPE\_CNT\_4P (3Fh)**

This command on page 1 sets the slope voltage clamp time during 4-phase operation for rail 1.

Command	MFR_SLOPE_CNT_4P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time during 4-phase operation. 5ns/LSB.

**MFR\_SLOPE\_SR\_5P (40h)**

This command on page 1 provides 2 bytes to program the slope compensation during 5-phase operation for rail 1.

Command	MFR_SLOPE_SR_5P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation during 5-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets current-source value for slope compensation during 5-phase operation. 0.25μA/LSB.

**MFR\_SLOPE\_CNT\_5P (41h)**

This command on page 1 sets the slope voltage clamp time during 5-phase operation for rail 1.

Command	MFR_SLOPE_CNT_5P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time during 5-phase operation. 5ns/LSB.

### MFR\_SLOPE\_SR\_6P (42h)

This command on page 1 provides 2 bytes to program the slope compensation for 6-phase operation for rail 1.

Command	MFR_SLOPE_SR_6P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									
	CURRENT_SOURCE															

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation during 6-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation during 6-phase operation. 0.25µA/LSB.

### MFR\_SLOPE\_CNT\_6P (43h)

This command on page 1 sets the slope voltage clamp time during 6-phase operation for rail 1.

Command	MFR_SLOPE_CNT_6P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time during 6-phase operation. 5ns/LSB.

### MFR\_SLOPE\_SR\_7P (44h)

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 7-phase operation, or rail 2's 6-phase operation. The MP2975 does not offer 6-phase operation on rail 2.

Command	MFR_SLOPE_SR_7P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									
	CURRENT_SOURCE															

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 7-phase operation, or rail 2's 6-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation for rail 1's 7-phase operation, or rail 2's 6-phase operation. 0.25µA/LSB.

**MFR\_SLOPE\_CNT\_7P (45h)**

This command on page 1 sets the slope voltage clamp time for rail 1's 7-phase operation, or rail 2's 6-phase operation. The MP2975 does not offer 6-phase operation on rail 2.

Command	MFR_SLOPE_CNT_7P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 7-phase operation, or rail 2's 6-phase operation. 5ns/LSB.

**MFR\_SLOPE\_SR\_8P (46h)**

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 8-phase operation, or rail 2's 5-phase operation. The MP2975 does not offer 5-phase operation on rail 2.

Command	MFR_SLOPE_SR_8P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 8-phase operation, or rail 2's 5-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation for rail 1's 8-phase operation, or rail 2's 5-phase operation. 0.25µA/LSB.

**MFR\_SLOPE\_CNT\_8P (47h)**

This command on page 1 sets the slope voltage clamp time for rail 1's 8-phase operation, or rail 2's 5-phase operation. The MP2975 does not offer 5-phase operation on rail 2.

Command	MFR_SLOPE_CNT_8P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 8-phase operation, or rail 2's 5-phase operation. 5ns/LSB.

**MFR\_SLOPE\_SR\_9P (48h)**

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 9-phase operation, or rail 2's 4-phase operation. The MP2975 does not offer 9-phase operation on rail 1.

Command	MFR_SLOPE_SR_9P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									
																CURRENT_SOURCE

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 9-phase operation, or rail 2's 4-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation for rail 1's 9-phase operation, or rail 2's 4-phase operation. 0.25µA/LSB.

**MFR\_SLOPE\_CNT\_9P (49h)**

This command on page 1 sets the slope voltage clamp time for rail 1's 9-phase operation, or rail 2's 4-phase operation. The MP2975 does not offer 9-phase operation on rail 1.

Command	MFR_SLOPE_CNT_9P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 9-phase operation, or rail 2's 4-phase operation. 5ns/LSB.

**MFR\_SLOPE\_SR\_10P (4Ah)**

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 10-phase operation, or rail 2's 3-phase operation. The MP2975 does not offer 10-phase operation on rail 1.

Command	MFR_SLOPE_SR_10P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 10-phase operation, or rail 2's 3-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation for rail 1's 10-phase operation, or rail 2's 3-phase operation. 0.25µA/LSB.

### MFR\_SLOPE\_CNT\_10P (4Bh)

This command on page 1 sets the slope voltage clamp time for rail 1's 10-phase operation, or rail 2's 3-phase operation. The MP2975 does not offer 10-phase operation on rail 1.

Command	MFR_SLOPE_CNT_10P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 10-phase operation, or rail 2's 3-phase operation. 5ns/LSB.

### MFR\_SLOPE\_SR\_11P (4Ch)

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 11-phase operation, or rail 2's 2-phase operation. The MP2975 does not offer 11-phase operation on rail 1.

Command	MFR_SLOPE_SR_11P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 11-phase operation, or rail 2's 2-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation for rail 1's 11-phase operation, or rail 2's 2-phase operation. 0.25µA/LSB.

### MFR\_SLOPE\_CNT\_11P (4Dh)

This command on page 1 sets the slope voltage clamp time for rail 1's 11-phase operation, or rail 2's 2-phase operation. The MP2975 does not offer 11-phase operation on rail 1.

Command	MFR_SLOPE_CNT_11P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 11-phase operation, or rail 2's 2-phase operation. 5ns/LSB.

### MFR\_SLOPE\_SR\_12P (4Eh)

This command on page 1 provides 2 bytes to program the slope compensation for rail 1's 12-phase operation, or rail 2's 1-phase CCM operation. The MP2975 does not offer 12-phase operation on rail 1.

Command	MFR_SLOPE_SR_12P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CAP									
																CURRENT_SOURCE

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation for rail 1's 12-phase operation, or rail 2's 1-phase operation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation for rail 1's 12-phase operation, or rail 2's 1-phase operation. 0.25µA/LSB.

### MFR\_SLOPE\_CNT\_12P (4Fh)

This command on page 1 sets the slope voltage clamp time for rail 1's 12-phase operation, or rail 2's 1-phase CCM operation. The MP2975 does not offer 12-phase operation on rail 1.

Command	MFR_SLOPE_CNT_12P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for rail 1's 12-phase operation, or rail 2's 1-phase operation. 5ns/LSB.

### MFR\_TEMP\_CAL (50h)

This command on page 1 sets the temperature-sense gain and offset.

Command	MFR_TEMP_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TEMP_OFFSET										TEMP_GAIN					

Bits	Bit Name	Description
15:8	TEMP_OFFSET	Sets the temperature-sense offset to convert the voltage on the TSEN1 pin to direct temperature in degrees. It is in two's complement format. Bit[7] is the sign bit. The list below shows the binary data and real-world temperature value:  8'b 0000 0000: 0 8'b 0000 0001: 1°C 8'b 0111 1111: 127°C 8'b 1000 0000: -128°C 8'b 1000 0001: -127°C 8'b 1111 1111: -1°C

7:0	TEMP_GAIN	Sets the temperature-sense gain to transfer the voltage on TSEN1 to direct temperature in degrees.
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The Intelli-Phase™ reports the junction temperature to the VTEMP or TOUT pin. Connect any Intelli-Phase™ devices to the TSEN1 pin so that the MP297x senses the power stage's temperature by sensing the voltage of TSEN1. TEMP\_GAIN and TEMP\_OFFSET programs the junction temperature gain and offset of TSEN1 pin into the MP297x. The Intelli-Phase™ junction temperature  $T_J$  can be calculated with Equation (25):

$$T_J(^{\circ}\text{C}) = a \times V_{\text{TSEN}1} + b \quad (25)$$

Where  $V_{\text{TSEN}1}$  is the voltage on the MP297x TSEN1 pin (in V),  $a$  is the temperature sense gain of the Intelli-Phase™ (in  $^{\circ}\text{C}/\text{V}$ ),  $b$  is the temperature sense offset in ( $^{\circ}\text{C}$ ),  $a$  is 80% of TEMP\_GAIN, and  $b$  is equal to TEMP\_OFFSET.

### MFR\_TSEN2\_ANA\_FAULT (51h)

This command on page 1 sets some configurations of the TSEN2 analog fault. It is valid for both rails.

Command	MFR_TSEN2_ANA_FAULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function									X	X						

Bits	Bit Name	Description
15	TSEN2_ANA_FAULT_DIR	Selects the TSEN2 analog fault direction. 1'b0: TSEN2 analog fault is triggered when the TSEN2 voltage exceeds the threshold set by bit[5:0] in this command 1'b1: TSEN2 analog fault is triggered when the TSEN2 voltage drops below the threshold set by bit[5:0] in this command
14	TSEN2_ANA_FAULT_MODE	Selects the TSEN2 analog fault action mode. 1'b0: Auto-retry 1'b1: Latch-off
13	TSEN2_ANA_FAULT_SD_MODE	Sets the shutdown mode when TSEN2 analog fault is triggered. 1'b0: Soft shutdown with a half DVID fast slew rate 1'b1: Hi-Z shutdown
12:8	TSEN2_DELAY_TIME	Sets the trigger delay for the TSEN2 analog fault. 100ns/LSB.
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	TSEN2_ANA_VTH	Sets the threshold for the TSEN2 analog fault. 50mV/LSB, maximum 2.4V.

### MFR\_IDROOP\_LIMIT\_SET (52h)

This command on page 1 sets the rail 2 maximum droop voltage limitation, and the sets the signal block time during DCM when the low-leakage switch is turned off.

Command	MFR_IDROOP_LIMIT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												IDROOP_LIMIT_SET

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	DCM_LOW_LKG_BLOCK_SET	Sets the set signal block time after the low-leakage slope switch is turned off in DCM mode. 10ns/LSB.
7:0	VDROOP_LIMIT_SET	Sets the maximum absolute droop voltage. If the load current makes the linear droop voltage ( $V_{DROOP}$ ) exceed the set value, the actual droop voltage is clamped to VDROOP_LIMIT_SET. This value is only valid when nonlinear AVP function is enabled by bit[11] of MFR_IDROOP_CTRL1_R2 (16h on page 2). 250/255mV/LSB.

### MFR\_IMON\_CONFIG (53h)

This command on page 1 sets some configurations on the internal IMON2 sense.

Command	MFR_IMON_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	X			

Bits	Bit Name	Description
15:3	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
2	IMON_ANA_FLT_DIS	Enables the IMON2 analog filter internal IC. 1'b0: Enable the IMON2 analog filter 1'b1: Disable the IMON2 analog filter
1	IMON_DIGI_FIL_DIS	Enables the IMON2 2-point digital filter. 1'b0: Enable the IMON2 2-point digital filter 1'b1: Disable the IMON2 2-point digital filter
0	IMON_BIAS_EN	Enables a 20µA bias current on IMON2. This improves the IMON2 report accuracy when $I_{CCMAX}$ is very low. 1'b0: No bias current on IMON2 1'b1: Add 20µA bias current on IMON2

### IOUT\_CAL\_OFFSET (54h)

This command on page 1 sets the offset for rail 2 output current PMBus report. The offset is for IOUT over-reporting or under-reporting. The reported output current is returned via PMBus command READ\_IOUT (8Ch on page 1).

Command	IOUT_CAL_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																IOUT_OFFSET_TOT

Bits	Bit Name	Description
15:14	IOUT_OFFSET_PHS_RES	Sets the bit resolution of IOUT_OFFSET_PHS. 2'b00: 0.25 ADC step resolution 2'b01: 0.5 ADC step resolution 2'b10: 1 ADC step resolution 2'b11: 2 ADC step resolution

13:9	IOUT_OFFSET_PHS	Sets the per-phase offset for IOUT reporting. It is effective for SVID, PMBus and AVSBus IOUT report. The final IOUT report is affected by IOUT_OFFSET_PHS and the active phase number. It is added to the IMON ADC-sense result, estimated with the following equation:  $\text{Imon\_sense} = \text{ADC(Imon)} + \text{phase\_num} \cdot \text{IOUT\_OFFSET\_PHS} \cdot 2^{(\text{IOUT\_OFFSET\_PHS\_RES} - 2)}$ <p>It is in two's complement data format. Bit[13] is the sign bit. The offset current resolution (IOUT_OFFSET_PHS_RES) is determined by bit[15:14] in this command. The table below shows the binary data and real-world current value.</p> <p>5'b00000: 0      5'b00001: 1 x IOUT_OFFSET_PHS_RES (A)      5'b01111: 31 x IOUT_OFFSET_PHS_RES (A)      5'b10000: -32 x IOUT_OFFSET_PHS_RES (A)      5'b10001: -31 x IOUT_OFFSET_PHS_RES (A)      5'b11111: -1 x IOUT_OFFSET_PHS_RES (A)</p>
8:0	IOUT_OFFSET_PMBUS	Sets the total IOUT report offset in two's complement data format. Bit[8] is the sign bit. The total offset only affects the final IOUT PMBus report to READ_IOUT (8Ch on page 1). 1A/LSB.  <p>The list below shows the binary data and real-world current value.</p> <p>9'b 0 0000 0000: 0A      9'b 0 0000 0001: 1A      9'b 0 1111 1111: 255A      9'b 1 0000 0000: -256A      9'b 1 0000 0001: -255A      9'b 1 1111 1111: -1A</p>

**MFR\_TSEN2\_DGTL\_FAULT (55h)**

This command on page 1 sets some configurations of the TSEN2 digital fault. It is valid for both rails.

Command	MFR_TSEN2_DGTL_FAULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TSEN2_DGTL_FLT_HYS								TSEN2_DGTL_FLT_TH							

Bits	Bit Name	Description
15	TSEN2_DGTL_FAULT_DIR	Selects the TSEN2 digital fault direction.  1'b0: TSEN2 digital fault is triggered when the TSEN2 voltage exceeds the threshold set by bit[7:0] in this command 1'b1: TSEN2 digital fault is triggered when the TSEN2 voltage drops belows the threshold set by bit[7:0] in this command
14	TSEN2_DGTL_FAULT_MODE	Selects the TSEN2 digital fault action mode.  1'b0: Auto-retry 1'b1: Latch-off
13:8	TSEN2_DGTL_FLT_HYS	Sets the TSEN2 digital fault hysteresis when this fault is set to auto-retry mode. 8 ADC-step/LSB
7:0	TSEN2_DGTL_FLT_TH	Sets the TSEN2 digital fault threshold. 8 ADC-step/LSB, maximum 3.19V

**MFR\_AP5\_DECAY\_ADV (56h)**

This command on page 1 sets rail 2's advanced options for APS and decay.

Command	MFR_AP5_DECAY_ADV															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							APS_COMP_CNT									
EN	APS_COMP_LEVEL															

Bits	Bit Name	Description
15	VFB_WINDOW_SEL	Selects the threshold of the VFB- window and VFB+ window. 1'b0: VFB- window = VREF - 25mV, VFB+ window = VREF + 20mV 1'b1: VFB- window = VREF - 12.5mV, VFB+ window = VREF + 10mV
14	PRT_THRES_DIV_EN	Enables the half divider for the protection thresholds for over-voltage protection (OVP2), under-voltage protection (UVP), and reverse-voltage protection (RVP). 1'b0: Disable half divider 1'b1: Enable half divider. The real OVP2, UVP, and RVP thresholds are half of their set value
13	VFB-_DECAY_EXIT_EN	Enables decay exiting when VFB drops below the VFB- window. During the decay process, when VFB is detected to be below the VFB- window, the controller exits decay and runs with full phase if UV_DECAY_EXIT_EN = 1. 1'b0: Disable decay exiting when VFB is below the VFB- window 1'b1: Enable decay exiting when VFB is below the VFB- window
12:10	VFB-_DECAY_EXIT_TBLANK	Sets the blanking time to exit decay when VFB drops below the VFB- window. 50ns/LSB.
9:5	APS_COMP_CNT	The MP297x provides positive compensation on VREF during phase-shedding to reduce undershoot. Phase-shedding may be initiated by an SVID SetPS command or APS. The VREF compensation is implemented by adding a PMBus-configurable positive voltage on COMP of the DC loop.  After phase-shedding starts, the voltage returns to 0V step by step with a time interval (see Figure Xa). APS_COMP_CNT sets the time interval between each step. 50ns/LSB.
4	DECAY_COMP_EN	Enables VREF compensation while the device exits decay. The MP297x provides VREF compensation while exiting decay. The compensation voltage level and slew rate is the same as with auto phase-shedding compensation (see Figure Xa). 1'b0: Disable VREF compensation while exiting decay 1'b1: Enable VREF compensation while exiting decay
3:0	APS_COMP_LEVEL	Sets the VREF compensation level during phase-shedding to reduce undershoot. The compensation is added to VREF when phase-shedding begins. 1.37mV/LSB

**MFR\_AP5\_CTRL (57h)**

This command on page 1 sets rail 2's APS timing and behaviors.

Command	MFR_AP5_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		DROP_PHASE_WAIT_TIME										MIN_TIME_PS0				
EN	EN															

Bits	Bit Name	Description
15:13	DROP_DELAY_SAMPLE_TIME	Sets the phase-shedding delay time. When the reported load current is below the APS threshold for APS_DELAY_TIME_CNT consecutive times of the IOUT reporting cycle, the controller enters APS mode and automatically sheds the phase count according to the load current.
12:8	DROP_PHASE_WAIT_TIME	Sets the phase-by-phase dropping time intervals. It is only effective when bit[7] of this command is set to 1. 1μs/LSB.
7	DROP_PHASE_MODE_SEL	Sets the phase dropping mode during phase-shedding. Phase-shedding may be due to APS or a SVID SetPS command. 1'b0: Drop phase count to the target phase count immediately 1'b1: Shed phases one by one with a configured delay time. The delay time is set with DROP_PHASE_WAIT_TIME of this command
6:2	MIN_FULL_PHASE_TIME	Sets the minimal full-phase runtime when the VR exits APS due to OCP_PHASE, VFB- window, or DVID events. 50μs/LSB.
1	APS_EXIT_UV_EN	When VFB falls below the VFB- window, this bit enables the VR to exit APS and run with full phase. 1'b0: Disable VFB- window event to exit APS 1'b1: Enable VFB- window event to exit APS
0	APS_EXIT_OC_EN	When phase 1 triggers OCP_PHASE, enables the VR to exit APS and run with full phase. 1'b0: Disable phase-1 OCP_PHASE event to exit APS 1'b1: Enable phase-1 OCP_PHASE event to exit APS

### MFR\_APS\_FS\_CTRL (58h)

This command on page 1 enables the exit phase-shedding strategy by detecting the PWM frequency, which is referred to as the FS limit event. It also sets the interval between consecutive phases' PWM rising edges to exit phase-shedding. It is for rail 2 only.

Command	MFR_APS_FS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the device to exit phase-shedding according to the PWM1_L2 off time. The time threshold is set by register MFR_FS_LIMIT_1112P (14h on page 1), bit[7:0]. The PWM minimum off time is excluded from PWM off time (see Figure 29). 1'b0: Disable PWM1_L2 off-time detection to exit APS 1'b1: Enable PWM1_L2 off-time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enables exit-phase-shedding according to the multi-phase PWMs interval time between consecutive phases. The time threshold is set by registers 12h, 13h, and 14h on page 1. The PWM blanking time is excluded from the PWM interval time (see Figure 30). 1'b0: Disable multi-phase PWM interval time detection to exit APS 1'b1: Enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count for PWM1_L2 off-time conditions to exit phase-shedding. Once the PWM off time reaches the counting threshold, the controller exits APS immediately.

6:3	RETURNAPS_DELAY	Sets the minimum full-phase runtime after exiting APS due to an FS limit event. 20µs/LSB.
2:0	FS_EXITAPS_CNT_NP	Sets the continuous count for the multi-phase PWM interval time to exit phase-shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.

**MFR\_DC\_LOOP\_CTRL (59h)**

This command on page 1 sets the DC loop calibration PI parameter and related holding conditions. It also provides 2 bits to program the PWM behavior during phase-adding, and provides 1 bit to program the READ\_VOUT (8Bh on page1) report format. It is for rail 2 only.

Command	MFR_DC_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	VOUT_PMBUS_LSB	Sets the READ_VOUT(8Bh on page 1) report format. 1'b0: Direct format, 1mV/LSB 1'b1: VID format
14:9	DC_LOOP_KI	Sets the PI parameter of the DC calibration loop.
8	PRD_ADD_PH_MODE	Sets the phase-adding mode when the PWM period meets the condition set with bit[13:7] in this command. 1'b0: Add phases with a PWM low time inserted between Hi-Z and Hi 1'b1: Add phases with no PWM Hi-Z to Hi lowt ime
7	VFB-_ADD_PH_MODE	Sets the phase-adding mode when VFB falls below the VFB- window. 1'b0: Add phases with a PWM low time inserted between Hi-Z and Hi 1'b1: Add phases with PWM Hi-Z to Hi low time
6	PRD_HOLD_DC_EN	Holds the DC loop when the PWM interval reaches the PWM switching period condition set via PMBus command MFR_FS (5Ch on page 1), bit[15:9]. 1'b0: Do not hold the DC loop when PWM switching period condition meets 1'b1: Hold the DC loop when the PWM switching period condition is met
5	PS_HOLD_DC_EN	Holds the DC loop when the phase count changes. 1'b0: Disable phase number changing to hold DC loop 1'b1: Enable phase number changing to hold the DC loop
4	TRANS_HOLD_DC_EN	Holds the DC loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ window or is below the VFB- window). 1'b0: Disable VFB+- window condition to hold DC loop 1'b1: Enable VFB+- window condition to hold DC loop
3:0	DC_CAL_MIN_THOLD	Sets the minimum DC loop hold time in direct format. 200µs/LSB with a +100µs offset.

### MFR\_CB\_LOOP\_CTRL (5Ah)

This command on page 1 enables a current-balance loop for rail 2. It also sets rail 2's current-balance loop PI parameter and related holding conditions.

Command	MFR_CB_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	CB_LOOP_EN	Enable the current-balance (CB) loop. 1'b0: Disable the CB loop 1'b1: Enable the CB loop
11:8	CB_LOOP_KI	Sets the PI parameter of current-balance loop.
7	TRANS_HOLD_CB_EN	Holds the current-balance (CB) loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ window or falls below the VFB- window). 1'b0: No CB loop hold for load transient event 1'b1: Hold the CB loop regulation when a load transient event is detected
6	PRD_HOLD_CB_EN	Holds the current-balance (CB) loop when the PWM time interval meets PWM switching period condition set via PMBus command MFR_FS (5Ch on page 1), bit[15:9]. 1'b0: No CB loop hold when the PWM interval meets the switching period conditions 1'b1: Hold the CB loop when the PWM switching period condition meets the PWM interval
5	PS_HOLD_CB_EN	Holds the current-balance (CB) loop when the phase count changes. 1'b0: No CB loop when phase count is changed 1'b1: Hold the CB loop when phase count is changed
4	DVID_HOLD_CB_EN	Holds the current-balance (CB) loop when DVID occurs. 1'b0: No CB loop hold when DVID occurs 1'b1: Hold the CB loop when DVID occurs
3:0	CB_LOOP_THOLD	Sets the current-balance loop hold time. If the corresponding enable bit is set and the device experiences a load transient, PWM switching period change, phase count change, or DVID event, the current balance loop stops regulating for a time set by command CB_LOOP_THOLD. 100µs/LSB.

### MFR\_FS\_LOOP\_CTRL (5Bh)

This command on page 1 enables the frequency loop for rail 2. It also sets the rail 2 frequency loop PI parameter and related holding conditions.

Command	MFR_FS_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	FS_LOOP_EN	Enables the frequency loop. 1'b0: Disable frequency loop 1'b1: Enable frequency loop
13:7	FS_LOOP_KI	Sets the frequency loop regulation parameter.
6	TRANS_HOLD_FS_EN	Holds the frequency-loop regulation when a load transient event is detected (e.g. VFB exceeds the VFB+ or VFB- window). 1'b0: No frequency loop hold when a load transient event is detected 1'b1: Hold the frequency-loop regulation when a load transient event is detected
5	PS_HOLD_FS_EN	Holds the frequency loop regulation when the phase count is changed. 1'b0: No frequency loop hold when the phase count is changed 1'b1: Hold the frequency-loop regulation when the phase count is changed
4	DVID_HOLD_FS_EN	Holds the frequency-loop regulation when DVID occurs. 1'b0: No frequency loop hold when DVID happens 1'b1: Hold the frequency-loop regulation when DVID happens
3:0	FS_LOOP_HOLD_TIME	Sets the minimum frequency loop hold time when the corresponding bit is enabled or there is a load transient, PWM switching period change, phase count change, or DVID event. 100µs/LSB.

### MFR\_FS (5Ch)

This command on page 1 sets the rail 2 switching frequency. It also sets the range of PWM periods for DC and current-balance loops for rail 2.

Command	MFR_FS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	HOLD_CB_DC_PRD_TIME															
	MFR_FS_SET															

Bits	Bit Name	Description
15:9	HOLD_CB_DC_PRD_TIME	Sets the period change time to hold the DC loop and current balance (CB) loop. If the PWM period meets the condition below and the associated enable bits are set, the DC loop and CB loop will be held. All the loop hold functions related to this time setting are ineffective during DCM. (The MP297x uses this time to hold the CB and DC loop. The FS loop cannot be held during this PWM time interval.) $  t_{PWM} - t_{PWM\_REF}   \leqslant HOLD\_CB\_DC\_PRD\_TIME \times 80ns$ Where $t_{PWM}$ is the real-time PWM period, and $t_{PWM\_REF}$ is the nominal period set with MFR_FS_SET in this command. 80ns/LSB.
8:0	MFR_FS_SET	Sets the switching frequency in direct format. 10kHz/LSB.

### MFR\_VR\_PROTECT\_SET (5Dh)

This command on page 1 sets some protection-related options for the MP297x.

Command	MFR_VR_PROTECT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										X

Bits	Bit Name	Description
15:10, 0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	TSEN2_DGTL_FLT_DIS	Enables rail 1's TSEN2 digital-sense fault to shut down rail 2. 1'b0: Disable TSEN2 digital-sense fault protection 1'b1: Enable TSEN2 digital-sense fault protection
8	TSEN2_ANA_FLT_DIS	Enables rail 1's TSEN2 analog fault to shut down rail 2. 1'b0: Disable TSEN2 analog fault protection 1'b1: Enable TSEN2 analog fault protection
7	DRMOS_FAULT_MODE	Selects the CS fault and TSEN1 fault (TSEN1 exceeds 2.4V) response on rail 2. 1'b0: Auto-retry 1'b1: Latch
6	PWM_FLT_DTCT_EN	Enables rail's 2 Intelli-Phase™ fault type detection with a PWM pin. It is only effective when the Intelli-Phase™ supports fault type reporting with the PWM pin. 1'b0: Disable PWM pin fault type detection 1'b1: Enable PWM pin fault type detection
5	CS_FLT_EN	Enables rail 2's CS fault protection. The MP297x monitors the voltage level on CS. Once CS is below 200mV, a CS fault occurs and the MP297x shuts down immediately. 1'b0: Disable CS fault detection 1'b1: Enable CS fault detection
4	TSEN1_FLT_DIS	Enables TSEN1 fault to shut down rail 2. The MP297x monitors the voltage on the TSEN1 pin. Once the TSEN1 voltage exceeds 2.2V, a TSEN1 fault occurs and the MP297x shuts down rail 1 immediately. TSEN1 fault detection does not affect power stage temperature sensing by the TSEN1 pin. It also does not affect over-temperature protection (OTP). 1'b0: Disable TSEN1 fault protection 1'b1: Enable TSEN1 fault protection
3:1	OVP1_DIS	Disables VOUT over-voltage protection (OVP1) protection for debugging. It is recommended to enable OVP1 protection during normal mode. 2'b011: Disable VOUT OVP1 protection Others: Enable VOUT OVP1 protection

**MFR\_VR\_CONFIG2 (5Eh)**

This command on page 1 sets the rail 2 VBOOT-related options, selects the PVID and PMBus override modes, and sets the Hi-Z shutdown voltage level.

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													VID_SHUT_DOWN

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	BOOT_MODE_SEL	Selects whether the start-up voltage is set by a register or pin. 1'b0: VBOOT is set by bits[11:4] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2) 1'b1: PMBus VBOOT is set by pin. The BOOT pin is assigned to the ADDR/CONFIG pin. This setting is not recommended.
11	PVID_EN	Enables rail 2 PVID mode. 1'b0: Disable PVID mode 1'b1: Enable PVID mode
10	PIN_VBOOT_MODE	Selects rail 1's PIN_VBOOT mode. 1'b0: Select 4 bits to determined VBOOT. These 4 bits are defined by ADDR/CONFIG 1'b1: Select 3MSB to determined VBOOT. The 3MSB is defined by ADDR/CONFIG
9	PMBUS_EN	Enables rail 2's PMBus override mode. 1'b0: Disable PMBus override mode for rail 2 1'b1: Enable PMBus override mode for rail 2
8:0	VID_SHUT_DOWN	Set rail 2's VID threshold, at which all PWMs go into tri-state when VID slews to 0V. The Hi-Z shutdown voltage level is only effective when VID slews down to 0V. The VID slews downs may be caused by soft-off or DVID going to 0V. Once the VID-DAC output is below the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged by the load current naturally (see Figure 3). It is in direct format with VID resolution. The rail 1 VID resolution is determined by bit[4] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

**MFR\_OCP\_TOTAL\_SET (5Fh)**

This command on page 1 sets the rail 2 OCP\_TOTAL related options and values.

Command	MFR_OCP_TOTAL_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	OCP_TOTAL_TBLANK										OCP_TOTAL_CUR				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:13	OCP_TOTAL_MODE	Set the OCP_TOTAL action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
12:7	OCP_TOTAL_TBLANK	Sets the blanking time for OCP_TOTAL in direct format. 100µs/LSB.
6:0	OCP_TOTAL_CUR	Sets the rail 2 per-phase OCP_TOTAL entry threshold in direct format. 1A/LSB.

### **TON\_DELAY (60h)**

This command on page 1 sets the delay time from when system initialization ends to when rail 2's VREF starts up.

<b>Command</b>	TON_DELAY															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the delay time from when system initialization ends to VREF boot-up. The resolution is determined by bit[14] of PMBus command MFR_SLOPE_ANA_CTRL (76h, page1), i.e. ON/OFF_DLY_CLK_SEL. 20µs/LSB (ON/OFF_DLY_CLK_SEL=0) 50µs/LSB (ON/OFF_DLY_CLK_SEL=1)

### **MFR\_OVP\_UVP\_MODE (61h)**

This command on page 1 sets the rail 2 over-voltage protection (OVP) and under-voltage protection (UVP) related options and values.

<b>Command</b>	MFR_OVP_UVP_MODE															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	OVP2_BLANK_TIME								UVP_BLANK_TIME							

Bits	Bit Name	Description
15:14	OVP2_MODE	Selects the over-voltage protection (OVP2) action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 3 or 6 times, determined by bit[13] below
13	OVP2_RETRY_TIMES	This bit sets the retry times when bit[15:14] = 2'b11 1'b1: Retry 3 times 1'b0: Retry 6 times
12:8	OVP2_BLANK_TIME	Sets the over-voltage protection (OVP2) blanking time. When an OVP2 condition remains for longer than the OVP2 blanking time, an OVP2 fault occurs. 100ns/LSB.
7:6	UVP_MODE	Selects the under-voltage protection (UVP) action mode. 2'b00: No action 2'b01: Latch-off 2'b10: Hiccup 2'b11: Retry 6 times
5:0	UVP_BLANK_TIME	Sets the under-voltage protection (UVP) blanking time. When a UV condition remains longer than the UVP blanking time, a UVP fault occurs. 20µs/LSB.

**MFR\_CUR\_GAIN (62h)**

This command on page 1 sets the rail 2 phase current sense gain. The MP297x senses the phase current by monitoring the voltage on CS. The gain will affect the real per-phase current limit. Equation (15) and Equation (16) on page 71 show the relationship of the current-sense gain and offset, and actual positive phase current limitation. Equation (17) and Equation (18) on page 71 show the relationship between the current-sense gain and offset, and the actual negative current phase limitation.

Command	MFR_CUR_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	PHASE_CUR_GAIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	PHASE_CUR_GAIN	Sets the phase current sense gain using the following equation: $\text{PHASE\_CUR\_GAIN} = \frac{256 \times K_{CS}}{5}$ Where $K_{CS}$ is the current sense gain of the Intelli-Phase™ (in $\mu\text{A/A}$ ).

**MFR\_CUR\_OFFSET (63h)**

This command on page 1 sets the rail 2 phase current sense offset.

Command	MFR_CUR_OFFSET															
Format	Two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	UCP_PHASE_OFFSET								OCP_PHASE_OFFSET							

Bits	Bit Name	Description
15:8	UCP_PHASE_CUR_OFFSET	Sets the under-current protection (UCP) phase current limitation offset. It is in two's complement format. Bit[15] is the sign bit. The list below shows the binary data and real-world current values: 8'b 0000 0000: 0 8'b 0000 0001: (-1 x 5 / $K_{CS}$ ) A 8'b 0111 1111: (-127 x 5 / $K_{CS}$ ) A 8'b 1000 0000: (128 x 5 / $K_{CS}$ ) A 8'b 1000 0001: (127 x 5 / $K_{CS}$ ) A 8'b 1111 1111: (1 x 5 / $K_{CS}$ ) A Where $K_{CS}$ is the Intelli-Phase™ (in $\mu\text{A/A}$ ).
7:0	OCP_PHASE_CUR_OFFSET	Sets over-current protection (OCP) phase current limitation offset. It is in two's complement format. Bit[7] is the sign bit. The list below shows the binary data and real-world current values: 8'b 0000 0000: 0 8'b 0000 0001: (1 x 5 / $K_{CS}$ ) A 8'b 0111 1111: (127 x 5 / $K_{CS}$ ) A 8'b 1000 0000: (-128 x 5 / $K_{CS}$ ) A 8'b 1000 0001: (-127 x 5 / $K_{CS}$ ) A 8'b 1111 1111: (-1 x 5 / $K_{CS}$ ) A Where $K_{CS}$ is the Intelli-Phase™ (in $\mu\text{A/A}$ ).

### TOFF\_DELAY (64h)

This command on page 1 sets the rail 2 delay time from when EN goes low to when VREF starts shutdown.

<b>Command</b>	TOFF_DELAY															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the delay time from EN low to VREF shutdown. The resolution is determined by bit[14] of PMBus command MFR_SLOPE_ANA_CTRL (76h on page 1) (e.g. ON/OFF_DLY_CLK_SEL). 20µs/LSB (ON/OFF_DLY_CLK_SEL = 0). 50µs/LSB (ON/OFF_DLY_CLK_SEL = 1).

### MFR\_OCP\_UCP\_PHASE\_SET (65h)

This command on page 1 sets the rail 2 per-phase valley current limit.

<b>Command</b>	MFR_OCP_UCP_PHASE_SET															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	UCP_PHASE_LIMIT															

Bits	Bit Name	Description
15:8	UCP_PHASE_LIMIT	Sets the per-phase negative valley current limit in direct format. -1A/LSB.
7:0	OCP_PHASE_LIMIT	Sets the per-phase positive valley current limit in direct format. 1A/LSB.

### MFR\_PSYS\_ANAFAULT (66h)

This command on page 1 sets some configurations for PSYS analog fault. It also provides 2 bits to enable PSYS digital fault. It is valid for both rails.

<b>Command</b>	MFR_PSYS_ANAFAULT															
<b>Format</b>	Unsigned binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	PSYS_DGTLFLT_EN_R2	Enables the PSYS digital fault for rail 2. 1'b0: Disable the PSYS digital fault for rail 2 1'b1: Enable the PSYS digital fault for rail 2
10	PSYS_DGTLFLT_EN_R1	Enables the PSYS digital fault for rail 1. 1'b0: Disable the PSYS digital fault for rail 1 1'b1: Enable the PSYS digital fault for rail 1

9	PSYS_ANA_FLT_EN_R2	Enables the PSYS analog fault for rail 2. 1'b0: Disable the PSYS analog fault for rail 2 1'b1: Enable the PSYS analog fault for rail 2
8	PSYS_ANA_FLT_EN_R1	Enables the PSYS analog fault for rail 1. 1'b0: Disable the PSYS analog fault for rail 1 1'b1: Enable the PSYS analog fault for rail 1
7	PSYS_ANA_FAULT_DIR	Selects the PSYS analog fault direction. 1'b0: PSYS analog fault is triggered when the PSYS voltage exceeds the threshold set by bit[7:0] on register MFR_PSYS_LEVEL (B4h on page 1) 1'b1: PSYS analog fault is triggered when the PSYS voltage drops below the threshold set by bit[7:0] on register MFR_PSYS_LEVEL (B4h on page 1)
6	PSYS_ANA_FAULT_MODE	Selects the PSYS analog fault action mode. 1'b0: Auto-retry 1'b1: Latch-off
5	PSYS_ANA_FAULT_OFF_MODE	Selects the shutdown mode of the PSYS analog fault. 1'b0: Soft shutdown with half of DVID fast slew rate 1'b1: Hi-Z shutdown
4:0	PSYS_ANA_DELAY_TIME	Sets the trigger delay of PSYS analog fault. 100ns/LSB.

### MFR\_PSYS\_DGTLFAULT (67h)

This command on page 1 sets some configurations for a PSYS digital fault. It is valid for both rails.

Command	MFR_PSYS_DGTLFAULT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PSYS_DGTLFLT_HYS										PSYS_SNS_DGTL_LEVEL					

Bits	Bit Name	Description
15	PSYS_DGTL_FAULT_DIR	Selects the PSYS digital fault direction. 1'b0: PSYS digital fault is triggered when the PSYS voltage exceeds the threshold set by bit[5:0] in this command 1'b1: PSYS digital fault is triggered when the PSYS voltage falls below the threshold set by bit[5:0] in this command
14	PSYS_DGTL_FAULT_MODE	Selects the PSYS digital fault action mode. 1'b0: Auto-retry 1'b1: Latch-off
13:8	PSYS_DGTLFLT_HYS	Sets the PSYS digital fault recovery threshold when this fault is set to hiccup mode. 4 ADC step/LSB.
7:0	PSYS_DGTLFLT_TH	Sets the PSYS digital fault threshold. 4 ADC-step/LSB, maximum 1.6V.

### MFR\_VR\_CONFIG1 (68h)

This command on page 1 programs some basic system configurations for rail 2.

Command	MFR_VR_CONFIG1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X			X											

Bits	Bit Name	Description															
15:14, 11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.															
13:12	DRMOS_KCS	Selects the DRMOS' Kcs gain on rail 1. 3'b000: 5µA/A 3'b001: 8.5µA/A 3'b010: 9.7µA/A 3'b011: 10µA/A Others: Reserved															
10	DROOP_COMP_LOOP_BW	This bit sets the droop compensation loop bandwidth combined with bit[8] of register 16h on page 2 (AC_DROOP_BW_SEL): <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DROOP_COMP_LOOP_BW</th> <th>AC_DROOP_BW_SEL Bit[8], 16h on Page 2)</th> <th>BW (Hz)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>25k</td> </tr> <tr> <td>0</td> <td>1</td> <td>50k</td> </tr> <tr> <td>1</td> <td>0</td> <td>250k</td> </tr> <tr> <td>1</td> <td>1</td> <td>500k</td> </tr> </tbody> </table>	DROOP_COMP_LOOP_BW	AC_DROOP_BW_SEL Bit[8], 16h on Page 2)	BW (Hz)	0	0	25k	0	1	50k	1	0	250k	1	1	500k
DROOP_COMP_LOOP_BW	AC_DROOP_BW_SEL Bit[8], 16h on Page 2)	BW (Hz)															
0	0	25k															
0	1	50k															
1	0	250k															
1	1	500k															
9	DIS_DECAY_EN	Enable bit to disable PWM Hi-Z after receiving a decay command. 1'b0: VR executes normal decay behavior and PWM goes to Hi-Z 1'b1: VR slews to target VID with slow slew rate after receiving a decay command															
8	SS_SR_SEL	Selects the soft-start slew rate mode. It is not compatible with AVSBus mode. 1'b1: The soft-start slew rate follows the SLEW_SLOW_SR set by register 11h on page 2 1'b0: The soft-start slew rate follows the BOOT_SR set by register 27h on page 1															
7	DC_LOOP_EN_DCM	Enables DC loop calibration at DCM. 1'b0: Disable DC loop calibration at DCM 1'b1: Enable DC loop calibration at DCM															
6	DC_LOOP_EN	Enables DC loop calibration both at DCM and CCM operation. 1'b0: Disable DC loop calibration 1'b1: Enable DC loop calibration															
5	FORCE_PS_EN	Enables forced power state. It is only effective when OPERATION (01h), bit[5:4] is not set to 2'b11. 1'b0: Disable forced power state with bit[4:3] of MFR_VR_CONFIG1 (68h on page 0) 1'b1: Enable forced power state with bit[4:3] of MFR_VR_CONFIG (68h on page 0)															
4:3	FORCE_PS_SET	Power state selection bits when MFR_VR_CONFIG1 (68h, page0), bit[5] = 1. 2'b00: Full-phase CCM. The phase count is determined by bit[3:0] of MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 2'b01: 1-phase CCM 2'b1X: 1-phase DCM															
2	DCM_TON_SET	Sets the PWM on time during DCM operation. 1'b0: PWM on time during DCM is same as in CCM operation 1'b1: PWM on time at DCM is 75% of that inCCM operation															
1	OSR_EN	Enables overshoot reduction. 1'b0: Disable overshoot reduction 1'b1: Enable overshoot reduction															

0	SVID_OVERCLK_EN	Enables overclocking in SVID mode. During SVID overclocking, VID is determined by PMBus command VOUT_COMMAND (21h on page 1), but the MP297x still responds to all CPU SVID commands. 1'b0: Disable SVID overclocking 1'b1: Enable SVID overclocking
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**MFR\_BLANK\_TIME2 (69h)**

This command on page 1 programs the second set of slope compensation reset times and PWM blanking times between two consecutive phases on rail 2.

Three sets of SLOPE\_RESET\_TIME and PWM\_BLANK\_TIME can be set by registers 69h, 6Ah and 72h on page 1. One is selected as the real-time value according to the operation phase number. The relationships can be estimated with Equation (25) and Equation (26), respectively:

$$\text{SLOPE_RESET_TIME} = \begin{cases} \text{SLOPE_RESET_TIME1(reg 72h bit[11:6]),} & \text{phase num} \geq \text{PHS_NUM_LVL1} \\ \text{SLOPE_RESET_TIME2(reg 69h bit[11:6]),} & \text{PHS_NUM_LVL2} \leq \text{phase num} < \text{PHS_NUM_LVL1} \\ \text{SLOPE_RESET_TIME3(reg 6Ah bit[11:6]),} & \text{phase num} < \text{PHS_NUM_LVL2} \end{cases} \quad (26)$$

$$\text{PWM_BLANK_TIME} = \begin{cases} \text{PWM_BLANK_TIME1(reg 72h bit[5:0]),} & \text{phase num} \geq \text{PHS_NUM_LVL1} \\ \text{PWM_BLANK_TIME2(reg 69h bit[5:0]),} & \text{PHS_NUM_LVL2} \leq \text{phase num} < \text{PHS_NUM_LVL1} \\ \text{PWM_BLANK_TIME3(reg 6Ah bit[5:0]),} & \text{phase num} < \text{PHS_NUM_LVL2} \end{cases} \quad (26)$$

Where PHS\_NUM\_LVL1 is the phase number set by register MFR\_BLANK\_TIME2 (69h on page 1) bit[15:12], and PHS\_NUM\_LVL2 is the phase number set by register MFR\_BLANK\_TIME2 (6Ah on page 1) bit[15:12].

Command	MFR_BLANK_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL1				SLOPE_RESET_TIME2				PWM_BLANK_TIME2							

Bits	Bit Name	Description
15:12	PHS_NUM_LVL1	Sets the phase number threshold for slope compensation reset time and PWM blanking time.
11:6	SLOPE_RESET_TIME2	Programs the second set for slope compensation reset time. It is effective when register MFR_SLOPE_ANA_CTRL (76h on page 1), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME, bit[5:0], in register MFR_BLANK_TIME2 (69h on page 1). 5ns/LSB.
5:0	PWM_BLANK_TIME2	Programs the second set of PWM blanking times between two consecutive phases. 5ns/LSB.

**MFR\_BLANK\_TIME3 (6Ah)**

This command on page 1 programs the third set of slope compensation reset times and PWM blanking times between two consecutive phases on rail 2.

Command	MFR_BLANK_TIME3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PHS_NUM_LVL2				SLOPE_RESET_TIME3				PWM_BLANK_TIME3							

Bits	Bit Name	Description
15:12	PHS_NUM_LVL2	Sets the phase number threshold for the slope compensation reset time and PWM blanking time.
11:6	SLOPE_RESET_TIME3	Programs the third set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h on page1), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME, bit[5:0], in register MFR_BLANK_TIME3 (6Ah on page 1). 5ns/LSB.
5:0	PWM_BLANK_TIME3	Programs the third set of PWM blanking times between two consecutive phases. 5ns/LSB.

### MFR\_DROOP\_CMPN1 (6Bh)

This command on page 1 sets the options to compensate the voltage drop caused by extra droop current when a droop resistor is applied during upward DVID on rail 2.

Command	MFR_DROOP_CMPN1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	DROOP_CMPN_LIMIT															

Bits	Bit Name	Description
15	DROOP_CMPN_EN	Droop compensation enable bit. 1'b0: Disable droop compensation 1'b1: Enable droop compensation
14:9	CNT_DROOP_CMPN_DEC	Sets the time interval for each VID step to reset droop compensation after DVID upward ends. 50ns/LSB.
8:6	CNT_DROOP_CMPN_INC	VID step counter to increase each step of droop compensation during upward DVID. $VID\_DROOP\_CMPN\_STEP = CNT\_DROOP\_CMPN\_INC \times VID\_STEP$
5:0	DROOP_CMPN_LIMIT	Sets the maximum VID steps for droop compensation in direct format with VID step resolution. The rail 1 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### MFR\_DROOP\_CMPN2 (6Ch)

This command on page 1 sets the options to compensate for the voltage drop caused by extra droop current when a droop resistor is applied during upward DVID on rail 2.

Command	MFR_DROOP_CMPN2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	VID_FLTR_SEL	Selects the VID-DAC output filter when DVID is downward. 2'b00: 2.14μs 2'b01: 4.28μs 2'b10: 6.42μs 2'b11: 8.56μs

13	VID_FLTR_EN	Enables the VID-DAC output filter. 1'b0: Disable VID DAC filter 1'b1: Enable VID DAC filter
12	VID-DAC_CMPN_EN	A comparator is designed between the VID-DAC output and VID-DAC filter output. It smooths the transition between downward and upward DVID. 1'b0: Disable the VID-DAC comparator 1'b1: Enable VID-DAC comparator
11:6	DLY_RST_DROOP_CMPN	Sets the delay time after VR_SETTLE to reset the droop compensation when DVID is upward. 50ns/LSB.
5:0	VID_FLTR_ACT_CTRL	Sets the VID filter effective threshold in direct format when the droop compensation is reset to 0. It is only effective when bit[13], VID_FLT_EN = 1. 1VID step/LSB.

### MFR\_PGOOD\_SET (6Dh)

This command on page 1 instructs the device when to assert VRRDY2 by setting the VRRDY2 action mode and the VRRDY2 signal assertion delay time. The VRRDY assertion delay time is only effective when VRRDY is set to non-Intel mode.

Command	MFR_PGOOD_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	PGOOD_MODE	Sets the VRRDY action mode. 1'b0: Intel mode. VRRDY asserts once VID reaches the start-up voltage 1'b1: Non-Intel mode. VRRDY asserts when the condition set by PMBus command POWER_GOOD_ON (6Eh on page 1) occurs and the VRRDY delay time expires
7:0	PGOOD_DELAY	Sets the VRRDY assertion delay time. It is only effective when VRRDY is set to non-Intel mode. 1μs/LSB.

### POWER\_GOOD\_ON (6Eh)

This command on page 1 sets the output voltage threshold at which the VRRDY2 signal asserts. It is only effective when VRRDY is set to non-Intel mode.

Command	POWER_GOOD_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									POWER_GOOD_ON

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_ON	Sets the reference voltage threshold at which the VRRDY signal asserts. It is only effective when VRRDY mode is set to as non-Intel mode. POWER_GOOD_ON is in direct format with VID resolution. The rail 1 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### **POWER\_GOOD\_OFF (6Fh)**

This command on page 1 sets the output voltage threshold at which the VRRDY2 signal de-asserts. It is only effective when VRRDY is set to non-Intel mode.

Command	POWER_GOOD_OFF																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	POWER_GOOD_OFF															

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_OFF	Sets the reference voltage threshold at which the VRRDY signal de-asserts. It is only effective when VRRDY is set to non-Intel mode. POWER_GOOD_OFF is in direct format with VID resolution. The rail 1 VID resolution is determined by bit[3] of MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### **MFR\_BLANK\_TIME1 (72h)**

This command on page 1 programs the first set of slope compensation reset times and PWM blanking times between two consecutive phases for rail 2.

Command	MFR_BLANK_TIME1																
Format	Unsigned binary																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	SLOPE_RESET_TIME1															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:12	SLOPE_RST_SW_SEL	Selects the slope reset switch for different switching frequencies. Increase the slope reset speed for high frequencies. For stronger switches, turn on the low-leakage switch during DCM. Strong level = SLOPE_RST_SW_SEL + 1
11:6	SLOPE_RESET_TIME1	Programs the first set of slope compensation reset times. It is effective when register MFR_SLOPE_ANA_CTRL (76h on page 1), bit[4] = 0. The slope compensation reset time should not be longer than the PWM blanking time set by PWM_BLANK_TIME, bit[5:0], in register MFR_BLANK_TIME2 (72h on page 1). 5ns/LSB.
5:0	PWM_BLANK_TIME1	Programs the first set of PWM blanking times between two consecutive phases. 5ns/LSB.

### **MFR\_OSR\_SET (73h)**

This command on page 1 sets the overshoot reduction (OSR) related parameters for rail 2.

Command	MFR_OSR_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	OSR_DEGLITCH_TIME								OSR_BLANK_TIME				

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	MIN_OSR_TIME	Sets the minimum OSR duration time. 5ns/LSB.
6:0	MIN_OSR_INTERVAL_TIME	Sets the blanking time between two effective OSR events. 10ns/LSB.

### MFR\_PWM\_MIN\_TIME1 (74h)

This command on page 1 sets the minimum pulse width when PWM is high, low, or in tri-state. This is for rail 2 only.

Command	MFR_PWM_MIN_TIME1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	PWM_MIN_LOW_TIME										MIN_HIGH_TIME	PWM_MIN_TRI_TIME			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	PWM_MIN_LOW_TIME	Sets the minimum PWM low time. 10ns/LSB with -5ns offset. The minimum PWM low time can be calculated with the following equation: $(\text{PWM\_MIN\_LOW\_TIME} \times 10 - 5) \text{ ns}$
8:6	PWM_MIN_HIGH_TIME	Sets the minimum PWM high time. 10ns/LSB with -5ns offset. The minimum PWM high time can be calculated with the following equation: $(\text{PWM\_MIN\_HIGH\_TIME} \times 10 - 5) \text{ ns}$
5:0	PWM_MIN_TRI_TIME	Sets the minimum PWM tri-state time. 10ns/LSB with -5ns offset. The minimum PWM tri-state time can be calculated with: $(\text{PWM\_MIN\_TRI\_TIME} \times 10 - 5) \text{ ns}$

### MFR\_PWM\_MIN\_TIME2 (75h)

This command on page 1 sets the PWM minimum off time and PWM on pulse width when under-current protection (UCP) is triggered on rail 2.

Command	MFR_PWM_MIN_TIME2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	TON_LIMIT_TO_VCAL				UCP_TIME				MIN_OFF_TIME					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	TON_LIMIT_TO_VCAL	Sets the $t_{on}$ limit below which the DC loop regulation will never be held. On the MP297x, the DC loop can be held if the PWM period meets the condition set in MFR_FS (5Ch, page1), bit[15:9]. But if the PWM on time calculated with Equation (1) is shorter than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
9	ZCD_EN	Enable bit for rail 2 zero-current crossing detection (ZCD). 1'b0: Disable ZCD 1'b1: Enable ZCD

8:5	UCP_PWM_HIGH_TIME	Sets the PWM high time when under-current protection (UCP) is triggered. 10ns/LSB with -5ns offset. The PWM high time at UCP can be calculated with the following equation:  (UCP_PWM_HIGH_TIME x 10 – 5) ns
4:0	PWM_MIN_OFF_TIME	Sets the PWM minimum off-time. 20ns/LSB with 15ns offset. The PWM minimum off-time can be calculated with the following equation:  (PWM_MIN_OFF_TIME x 20 + 15) ns

**MFR\_SLOPE\_ANA\_CTRL (76h)**

This command on page 1 programs the slope compensation options for rail 2.

Command	MFR_SLOPE_ANA_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X		X										X	X		
Bits	Bit Name			Description												
15, 13	RESERVED			Unused. X indicates that writes are ignored and reads are always 0.												
14	ON/OFF_DLY_CLK_SEL			Selects the clock frequency for the rail 1 turn-on delay and turn-off delay counter. The counter is set with PMBus command TON_DELAY (60h on page 1) and TOFF_DELAY (64h, page 1). See the TON_DELAY (60h on page 1) and TOFF_DELAY (64h on page 1) sections on page 140 for more information.  1'b0: 50kHz 1'b1: 20kHz												
12	SLOPE_LEAKAGE_EN			Enables slope low-leakage switching after the slope counter reaches the set value for each phase.  1'b0: Disable 1'b1: Enable												
11	SLOPE_INI_EN			Enables initial slope compensation before soft start.  1'b0: Disable initial slope compensation 1'b1: Enable initial slope compensation												
10:5	SLOPE_INI_ISOURCE			Sets the current-source value for initial slope compensation. The slope voltage can be calculated with the following equation:  $V_{SLOPE\_INI} (\text{mV}) = 0.845 \times SLOPE\_INI\_ISOURCE \times SLOPE\_INI$ Design the initial slope voltage so that it is 150% to 200% of the full-phase nominal slope voltage. See register MFR_SLOPE_SR_1P (38h on page 1) on page 118 for full-phase slope voltage calculations.												
4	SLOPE_RST_SEL			Selects the slope compensation resetting time.  1'b0: Slope compensation is reset during SLOPE_RST_TIME, which is defined with PMBus commands 69h, 6Ah, and 72h on page 1, bit[11:6] 1'b1: Slope compensation is reset when PWM is high												
3:2	RESERVED			Unused. X indicates that writes are ignored and reads are always 0.												
1	DVIDUP_PREBIAS_MODE			Sets the PWM behavior during upward DVID.  1'b0: Pre-biased mode. All PWM signals enter Hi-Z to high individually 1'b1: PWM1 goes Hi-Z to high. Other PWMs pull low first, then pull high when an individual set signal is received												

0	DCM_EXIT_SLOPE_CTRL	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, the slope compensation starts, then follows the slew rate defined by the new power state. 1'b0: Maintain the slope current status when exiting DCM 1'b1: Enable the slope current while exiting DCM to reduce undershoot
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**STATUS\_BYTE (78h)**

This command on page 1 returns 1 byte of information with a summary of the most critical status and fault updates.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								X

Bits	Bit Name	Behavior	Description
7	MTP_BUSY	Live	Reports the live status of the MTP. 1'b0: The MTP is idle. The MTP can read and write with a PMBus command 1'b1: The MTP is busy. The MTP cannot read or write with a PMBus command
6	OFF	Live	Rail 2 output is off. This bit is in live mode. It is asserted if the rail 1 output is off. VOUT can turn off for protections, when EN is low, or VID = 0. 1'b0: VOUT1 is off 1'b1: VOUT1 is on
5	VOUT_OV_FAULT	Latch	Rail 2 output over-voltage (OV) fault indicator. This bit is set and latched if rail 1 OVP occurs. Send the CLEARFAULTS (03h) command to reset this bit. 1'b0: No VOUT OV fault 1'b1: VOUT OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 2 output current over-current (OC) fault indicator. This bit is set and latched if rail 1 OCP occurs. Send the CLEARFAULTS (03h) command to reset this bit. 1'b0: No output OC fault 1'b1: Output OC fault has occurred
3	VIN_UV_FAULT	Latch	Input voltage under-voltage (UV) fault indicator. This bit is set and latched if an input voltage UV fault happens. Send the CLEARFAULTS (03h) command to reset this bit. 1'b0: No VIN UV fault 1'b1: VIN UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature (OT) fault and warning indicator. This bit is set and latched if TSEN1 senses and OT warning or OT protection. Send the CLEARFAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning 1'b1: OT fault or warning has occurred

1	CML	Latch	PMBus communication fault indicator. If a PMBus communication fault occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault 1'b1: A CML fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_WORD (79h)**

This command on page 1 returns 2 bytes of information with a summary of the device's fault and warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte shares information with register STATUS\_BYTE (78h).

Command	STATUS_WORD															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function						X										STATUS_BYTE (78H)

Bits	Bit Name	Behavior	Description
15	VOUT	Live	Rail 2 VOUT fault and warning indicator. If an output over-voltage or under-voltage protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No VOUT fault/warning 1'b1: VOUT fault/warning has occurred
14	IOUT/POUT	Live	Rail 2 IOUT/POUT fault and warning indicator. If an output current or power fault/warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No IOUT/POUT fault and warning 1'b1: IOUT/POUT fault or warning has occurred
13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. If any protection or warning of the input voltage, current, or power occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No input fault and warning 1'b1: Input fault or warning has occurred
12	PSYS FAULT	Latch	PSYS analog fault or PSYS sense fault indicator. If a PSYS analog/sense fault occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No PSYS analog/sense fault 1'b1: PSYS analog/sense fault has occurred
11	TSEN2 FAULT	Latch	Rail 2 TSEN2 analog fault or TSEN2 digital sense fault indicator. If a TSEN2 analog/sense fault occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No TSEN2 analog/sense fault 1'b1: TSEN2 analog/sense fault has occurred

10	PGOOD	Live	Rail 2 VRRDY status indicator. When VRRDY is set to Intel mode and VOUT reaches its start-up voltage, this bit is set. The bit resets when VOUT is disabled or in a fault state.  When VRRDY is set to non-intel mode, VOUT exceeds the POWER_GOOD_ON level, and the PGOOD delay time expires, this bit is asserted. It is de-asserted when a fault occurs or VOUT falls below POWER_GOOD_OFF.
9	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	Indicator for watchdog block timer overflow. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation, state machine, and timer are reset, and this bit is set. The CLEAR_FAULTS (03h) command resets this bit.  1'b0: Watchdog timer does not overflow 1'b1: Watchdog timer has overflowed

**STATUS\_VOUT (7Ah)**

This command on page 1 returns one byte of information with the detailed VOUT fault and warning statuses on rail 2.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	X	X				X		X

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 2 VOUT over-voltage (OV) fault indicator. Once output OVP occurs, this bit is set and latched. The CLEAR_FAULTS command resets this bit.  1'b0: No VOUT OV fault 1'b1: VOUT OV fault has occurred
6:5	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.
4	VOUT_OV_FAULT	Latch	Rail 2 output voltage over-voltage (OV) fault indicator. This bit is set and latched if rail 1 OVP occurs. The CLEAR_FAULTS (03h) command resets this bit.  1'b0: No VOUT OV fault 1'b1: VOUT OV fault has occurred
3	VOUT_MAX_MIN_WARNING	Latch	Rail 2 VOUT hit VOUT_MAX and VOUT_MIN indicator.  Once the VID value exceeds the value set in VOUT_MAX (24h, page 0) and VOUT_MIN (2Bh, page 0), this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit.  1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID has exceeded VOUT_MAX or is below VOUT_MIN
2	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

1	LINE_FLOAT	Latch	Rail 2 line float protection indicator. Once a line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. It is in latch mode. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No line float fault 1'b1: Line float fault has occurred
0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**STATUS\_IOUT (7Bh)**

This command on page 1 returns 1 byte of information with the detailed IOUT fault and warning statuses on rail 2.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	X

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 2 output over-current (OC) fault indicator. If output OCP occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No output OC fault 1'b1: Output OC fault has occurred
6	OC_UV_FAULT	Latch	Rail 2 output OC and under-voltage (UV) dual fault indicator. If an output OC occurs and the UV comparator is simultaneously set, this bit is set and latched. The CLEAR_FAULTS (03h) command resets this bit. 1'b0: No output over-current and under-voltage faults 1'b1: Output OC has occurred and the UV comparator sets
5:0	RESERVED	N/A	Unused. X indicates that writes are ignored and reads are always 0.

**READ\_CS1\_2\_L2 (85h)**

This command on page 1 returns the ADC-sensed average voltage on rail 2's CS1 and CS2 in direct format. An internal low-pass filter is used before the ADC.

Command	READ_CS1_2_L2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_CS2_L2								READ_CS1_L2							

Bits	Bit Name	Description
15:8	READ_CS2_L2	Returns the ADC-sensed voltage on rail 2 CS2 in direct format. 12.5mV/LSB.
7:0	READ_CS1_L2	Returns the ADC-sensed voltage on rail 2 CS1 in direct format. 12.5mV/LSB.

### READ\_CS3\_4\_L2 (86h)

This command on page 1 returns the ADC-sensed average voltage on rail 2's CS3 and CS4 in direct format. An internal low-pass filter is used before the ADC.

<b>Command</b>	READ_CS3_4_L2															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	READ_CS4_L2								READ_CS3_L2							

Bits	Bit Name	Description
15:8	READ_CS4_L2	Returns the ADC-sensed voltage on rail 2's CS4 in direct format. 12.5mV/LSB.
7:0	READ_CS3_L2	Returns the ADC-sensed voltage on rail 2's CS3 in direct format. 12.5mV/LSB.

### READ\_CS5\_6\_L2 (87h)

This command on page 1 returns the ADC-sensed average voltage on rail 2's CS5 and CS6 in direct format. An internal low-pass filter is used before the ADC. The MP2975 does not offer these options.

<b>Command</b>	READ_CS5_6_L2															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	READ_CS6_L2								READ_CS5_L2							

Bits	Bit Name	Description
15:8	READ_CS6_L2	Returns the ADC-sensed voltage on rail 2's CS6 in direct format. 12.5mV/LSB.
7:0	READ_CS5_L2	Returns the ADC-sensed voltage on rail 2's CS5 in direct format. 12.5mV/LSB.

### READ\_VOUT (8Bh)

This command on page 1 returns the sensed rail 2 VOSEN-VORTN voltage.

<b>Command</b>	READ_VOUT															
<b>Format</b>	VID or direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	x	x	x	x	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the sensed voltage of VOSEN-VORTN. The voltage report is in VID format with VID resolution, or direct format with 1mV resolution. The resolution is determined by bit[15] (e.g. VOUT_PMBUS_LSB of PMBus command MFR_DC_CTRL (59h on page 1)).  1 VID step/LSB when VOUT_PMBUS_LSB = 1 1mV/LSB VOUT_PMBUS_LSB = 0

### READ\_IOUT (8Ch)

This command on page 1 returns rail 2's sensed output current direct format.

<b>Command</b>	READ_IOUT															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0											READ_IOUT

Bits	Bit Name	Description
15:11	EXP	Fixed to 5'b00000.
10:0	READ_IOUT	Returns the sensed output current. 1A/LSB.

### READ\_IOUT\_PK (90h)

This command on page 1 returns the sensed peak value of rail 2's output current in direct format.

<b>Command</b>	READ_IOUT_PK															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X												READ_IOUT_PK

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_IOUT_PK	Returns the sensed peak output current. Each time the MP297x receives the command READ_IOUT_PK, it returns the peak output current and resets the value in the buffer to 0. This starts a new cycle of peak current recording. 0.25A/LSB.

### READ\_POUT\_PK (91h)

This command on page 1 returns rail 2's sensed peak output power in direct format.

<b>Command</b>	READ_POUT_PK															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X													READ_POUT_PK

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:0	READ_POUT_PK	Returns the sensed peak output power in direct format. Each time the MP297x receives the command READ_POUT_PK, it returns the peak output power and resets the value in the buffer to 0. This starts a new cycle of peak power recording. 0.25W/LSB.

### READ\_TON (94h)

This command on page 1 returns rail 2's real-time PWM on time.

<b>Command</b>	READ_TON															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X	X	READ_TON										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	READ_TON	Returns the real-time PWM on time in direct format. 0.625ns/LSB.

### READ\_TS (95h)

This command on page 1 returns rail 2's real-time switching period time.

<b>Command</b>	READ_TS															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	X	X	X	X	X	READ_TS										

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_TS	Returns the real-time switching period time in direct format. 1.25ns/LSB.

### READ\_POUT (96h)

This command on page 1 returns rail 2's sensed output power in direct format.

<b>Command</b>	READ_POUT															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
<b>Function</b>	0	0	0	0	0	READ_POUT										

Bits	Bit Name	Description
15:11	EXP	Fixed to 00000.
10:0	READ_POUT	Returns the sensed output power in direct format. 1W/LSB.

### MFR\_CS\_OFFSET1 (99h)

This command on page 1 sets the CS ADC-sensing offset for thermal balance adjusting.

<b>Command</b>	MFR_CS_OFFSET1															
<b>Format</b>	Two's complement															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	CS4_OFFSET				CS3_OFFSET				CS2_OFFSET						

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

		Sets the offset on the ADC-sensed value of the CS4 pin voltage. It is in two's complement format. Bit[14] is the signed bit. The real-world current affected by CS4_OFFSET can be calculated with the following equation:
14:10	CS4_OFFSET	$I_{OFFSET} = 8 \times \frac{1.6}{1023} \times \frac{CSx\_OFFSET}{K_{cs} \times R_{cs}}$ Where $I_{OFFSET}$ is the real-world offset current, $CSx\_OFFSET$ is the real-world decimal value, $K_{cs}$ is the current-sense gain (in A/A), and $R_{cs}$ is the CS pin resistor (in $\Omega$ ).
9:5	CS3_OFFSET	Sets the offset on the ADC-sensed value of the CS3 pin voltage. It is in two's complement format. Bit[9] is the signed bit.
4:0	CS2_OFFSET	Sets the offset on the ADC-sensed value of the CS2 pin voltage. It is in two's complement format. Bit[4] is the signed bit.

### MFR\_CS\_OFFSET2 (9Ah)

This command on page 1 sets the CS ADC-sensing offset for thermal balance adjusting.

Command	MFR_CS_OFFSET2																
Format	Two's complement																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	CS7_OFFSET						CS6_OFFSET						CS5_OFFSET			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	CS7_OFFSET CS6_L2_OFFSET	Sets the offset on the ADC-sensed value of the CS7 pin voltage when it is assigned to rail 1, or CS6_L2 when it is assigned to rail 2. It is in two's complement format. Bit[14] is the sign bit.
9:5	CS6_OFFSET	Sets the offset on the ADC-sensed value of the CS6 pin voltage. It is in two's complement format. Bit[9] is the sign bit.
4:0	CS5_OFFSET	Sets the offset on the ADC-sensed value of the CS5 pin voltage. It is in two's complement format. Bit[4] is the sign bit.

### MFR\_CS\_OFFSET3 (9Bh)

This command on page 1 sets the CS ADC-sensing offset for thermal balance adjusting.

Command	MFR_CS_OFFSET3																
Format	Two's complement																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	X	CS10_OFFSET						CS9_OFFSET						CS8_OFFSET			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	CS10_OFFSET CS3_L2_OFFSET	Sets the offset on the ADC-sensed value of the CS10 pin voltage when it is assigned to rail 1, or CS3_L2 when it is assigned to rail 2. It is in two's complement format. Bit[14] is the sign bit.
9:5	CS9_OFFSET CS4_L2_OFFSET	Sets the offset on the ADC-sensed value of the CS9 pin voltage when it is assigned to rail 1, or CS4_L2 when it is assigned to rail 2. It is in two's complement format. Bit[9] is the sign bit.

4:0	CS8_OFFSET CS5_L2_OFFSET	Sets the offset on the ADC-sensed value of the CS8 pin voltage when it is assigned to rail 1, or CS5_L2 when it is assigned to rail 2. It is in two's complement format. Bit[4] is the sign bit.
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### MFR\_CS\_OFFSET4 (9Dh)

This command on page 1 sets the CS ADC-sensing value offset for thermal balance adjusting.

Command	MFR_CS_OFFSET4															
Format	Two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	CS12_OFFSET				CS11_OFFSET					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:5	CS12_OFFSET	Sets the offset on the ADC-sensed value of the CS12 pin voltage when it is assigned to rail 1. It is in two's complement format. Bit[9] is the sign bit.
4:0	CS11_OFFSET CS2_L2_OFFSET	Sets the offset on the ADC-sensed value of the CS11 pin voltage when it is assigned to rail 1, or CS2_L2 when it is assigned to rail 2. It is in two's complement format. Bit[4] is the sign bit.

### MFR\_AVSBUS\_CONFIG (9Eh)

This command on page 1 programs the options and parameters related to AVSBus override mode.

Command	MFR_AVSBUS_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	SETTLE_PREFIX_MODE	Selects the behavior when issuing a status response frame during AVSBus VID.  1'b0: Only the slave issues a status response frame when it receives a status from a corresponding rail 1'b1: The slave issues a status response frame and a Get Response command if the VDONE flag of the status response frame is set to 1
8	DIS_PREFIX_MODE	Selects the behavior mode of the status response frame during AVSBus mode, but VID is controlled by the PMBus interface.  1'b0: The status response frame is issued from the VR to CPU when any of the AVSBus status bits flags are changed: over-current warning (OCW), under-voltage warning (UVW), over-temperature warning (OTW), and over-power warning (OPW) 1'b1: The status response frames are not issued from the VR to CPU when any of the AVSBus status bits (OCW, UVW, OTW, and OPW) flags are changed.
7	AVSBUS_PREFIX_MODE	Selects when the MP297X issues a status response frame to the CPU at dynamic VID transition. It is only effective during AVSBus override mode.  1'b0: The MP297X issues status response frame when either rails' VR is settled 1'b1: The MP297X issues status response frame when both rails' VRs are settled

6	VDONE_WARN_EN	Masks the VDONE warning flag to force the slave to issue a status response frame to the CPU. 1'b0: Mask VDONE warning 1'b1: Do not mask VDONE warning
5	OCW_WARN_EN	Masks the over-current warning (OCW) flag to force the slave to issue the status response frame to the CPU. 1'b0: Mask OCW warning 1'b1: Do not mask OCW warning
4	UVW_WARN_EN	Masks the under-voltage warning (UVW) flag to force the slave to issue the status response frame to the CPU. 1'b0: Mask UVW warning 1'b1: Do not mask UVW warning
3	OPW_WARN_EN	Masks the over-power warning (OPW) flag to force the slave to issue the status response frame to the CPU. 1'b0: Mask OPW warning 1'b1: Do not mask OPW warning
2	OTW_WARN_EN	Masks the over-temperature warning (OTW) flag to force the slave to issue a status response frame to the CPU. 1'b0: Mask OTW warning 1'b1: Do not mask OTW warning
1:0	COMM_PORTS_CFG	Selects which pins are multiplexed as AVSBus communication lines during AVSBus override mode. 2'b11: Not used 2'b10: Multiplex VR_HOT (pin 14) to AVS_MISO, multiplex SDIO (pin 18) to AVS_MOSI, and multiplex SCLK (pin 17) to AVS_CLK 2'b01: Multiplex ALERT# (pin 19) to AVS_MISO, multiplex SDIO (pin 18) to AVS_MOSI, and multiplex SCLK (Pin 17) to AVS_CLK 2'b00: No pins are multiplexed for AVSBus

### MFR\_CUR\_OFFSET\_SVID (9Fh)

This command on page 1 sets the IOUT offset for SVID telemetry.

Command	MFR_CUR_OFFSET_SVID															
Format	Two's complementary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W															
Function	CUR_OFFSET_SVID_R2								CUR_OFFSET_SVID_R1							

Bits	Bit Name	Description
15:8	CUR_OFFSET_SVID_R2	Default value of SVID register I_OFFSET (28h). Sets the IOUT offset added on rail 2's SVID telemetry (15h). (ICCMAX_R2/255)A/LSB.
7:0	CUR_OFFSET_SVID_R1	Default value of SVID register I_OFFSET (28h). Sets the IOUT offset added on rail 1's SVID telemetry (15h). (ICCMAX_R1/255)A/LSB.

### READ\_VOUT\_MIN (A4h)

This command on page 1 returns the rail 2 minimum VOUT based on the most recent VID setting command.

Command	READ_VOUT_MIN																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R							
Function	X	X	X	X	X	X	X	READ_VOUT_MIN															

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT_MIN	Returns the minimum VOUT values based on the most recent VID setting. The returned value is reset to 0x01FF when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1VID/LSB.

### READ\_VOUT\_MAX (A5h)

This command on page 1 returns the rail 2 maximum VOUT based on the most recent VID setting command.

Command	READ_VOUT_MAX																						
Format	Direct																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R							
Function	X	X	X	X	X	X	X	READ_VOUT_MAX															

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT_MAX	Returns the maximum VOUT values based on the last VID setting. The returned value is reset to 0 when a set VID command is received from the SVID, AVSBus, or PMBus interface. 1VID/LSB.

### MFR\_FAULTS1 (A6h)

This command on page 1 returns the protection information for the MP297x. The MP2975 does not offer 9-phase, 10-phase, 11-phase, or 12-phase operation for rail 1, and it does not offer 5-phase or 6-phase operation for rail 2.

Command	MFR_FAULTS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X					X						

Bits	Bit Name	Description
15:11, 7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	DRMOS_FLT_R2	Rail 2 DRMOS fault indicator. A DRMOS fault means TSEN1 has exceeded 2.2V, or CS has dropped below the 200mV fault level. 1'b0: No DRMOS fault on rail 2 1'b1: A DRMOS fault has occurred on rail 2

9	DRMOS_FLT_R1	Rail 1 DRMOS fault indicator. A DRMOS fault means TSEN1 has exceeded 2.2V, or CS has dropped below the 200mV fault level. 1'b0: No DRMOS fault on rail 1 1'b1: A DRMOS fault has occurred on rail 1
8	TSEN1_FLT_FLAG	This bit indicates if the TSEN1 pin voltage exceeds the 2.2V fault value. 1'b0: No TSEN1 fault 1'b1: TSEN1 has exceeded 2.2V, and a fault has occurred
6:4	CS_FLT_FLAG_R2	CS fault indicators for rail 2. 3'b000: No CS fault is detected on rail 2 3'b001: A CS fault has been detected on phase 1 of rail 2 3'b010: A CS fault has been detected on phase 2 of rail 2 3'b011: A CS fault has been detected on phase 3 of rail 2 3'b100: A CS fault has been detected on phase 4 of rail 2 3'b101: A CS fault has been detected on phase 5 of rail 2 3'b110: A CS fault has been detected on phase 6 of rail 2 3'b111: Unused
3:0	CS_FLT_FLAG_R1	CS fault indicator for rail 1. 4'b0000: No CS fault is detected on rail 1 4'b0001: A CS fault has been detected on phase 1 of rail 1 4'b0010: A CS fault has been detected on phase 2 of rail 1 4'b0011: A CS fault has been detected on phase 3 of rail 1 4'b0100: A CS fault has been detected on phase 4 of rail 1 4'b0101: A CS fault has been detected on phase 5 of rail 1 4'b0110: A CS fault has been detected on phase 6 of rail 1 4'b0111: A CS fault has been detected on phase 7 of rail 1 4'b1000: A CS fault has been detected on phase 8 of rail 1 4'b1001: A CS fault has been detected on phase 9 of rail 1 4'b1010: A CS fault has been detected on phase 10 of rail 1 4'b1011: A CS fault has been detected on phase 11 of rail 1 4'b1100: A CS fault has been detected on phase 12 of rail 1 Others: Unused

**MFR\_FAULTS2 (A7h)**

This command on page 1 returns the protection information of the MP297x.

Command	MFR_FAULTS2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15	VIN_OVP_FLAG_R1	Rail 1 VIN over-voltage protection (OVP) indicator. 1'b0: No VIN OVP on rail 1 1'b1: VIN OVP has occurred on rail 1
14	VIN_OVP_FLAG_R2	Rail 2 VIN over-voltage protection (OVP) indicator. 1'b0: No VIN OVP on rail 2 1'b1: VIN OVP has occurred on rail 2
13	VIN_UVLO_FLAG_R1	Rail 1 VIN under-voltage lockout (UVLO) indicator. 1'b0: No VIN UVLO on rail 1 1'b1: VIN UVLO has occurred on rail 1

12	VIN_UVLO_FLAG_R2	Rail 2 VIN under-voltage lockout (UVLO) indicator. 1'b0: No VIN UVLO on rail 2 1'b1: VIN UVLO has occurred on rail 2
11	OTP_FLAG	TSEN1 over-temperature protection (OTP) indicator. 1'b0: No TSEN1 OTP 1'b1: TSEN1 OTP has occurred
10	CHIP OTP_FLAG	Chip over-temperature protection (OTP) indicator. 1'b0: No chip OTP 1'b1: Chip OTP has occurred
9	TSEN2_ANA_FAULT_FLAG	TSEN2 analog fault indicator. 1'b0: No TSEN2 analog fault 1'b1: A TSEN2 analog fault has occurred
8	TSEN2_DGTL_FAULT_FLAG	TSEN2 digital fault indicator. 1'b0: No TSEN2 digital fault 1'b1: A TSEN2 digital fault has occurred
7	PSYS_ANA_FAULT_FLAG	PSYS analog fault indicator. 1'b0: No PSYS analog fault 1'b1: A PSYS analog fault has occurred
6	PSYS_DGTL_FAULT_FLAG	PSYS digital fault indicator. 1'b0: No PSYS digital fault 1'b1: A PSYS digital fault has occurred
5	OVP_FLAG_R1	Rail 1 VOUT over-voltage (OV) fault indicator. 1'b0: No VOUT OV fault 1'b1: A VOUT OV fault has occurred
4	UVP_FLAG_R1	Rail 1 VOUT under-voltage (UV) fault indicator. 1'b0: No VOUT UV fault 1'b1: A VOUT UV fault has occurred
3	OCP_FLAG_R1	Rail 1 VOUT over-current (OC) fault indicator. 1'b0: No VOUT OC fault 1'b1: A VOUT OC fault has occurred
2	OVP_FLAG_R2	Rail 2 VOUT over-voltage (OV) fault indicator. 1'b0: No VOUT OV fault 1'b1: A VOUT OV fault has occurred
1	UVP_FLAG_R2	Rail 2 VOUT under-voltage (UV) fault indicator. 1'b0: No VOUT UV fault 1'b1: A VOUT UV fault has occurred
0	OCP_FLAG_R2	Rail 2 VOUT over-current (OC) fault indicator. 1'b0: No VOUT OC fault 1'b1: A VOUT OC fault has occurred

**MFR\_FAULTS3 (A8h)**

This command on page 1 returns the Intelli-Phase™ fault type information.

Command	MFR_FAULTS3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM1_FAULTS				PWM2_FAULTS				PWM3_FAULTS				PWM4_FAULTS			

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Intelli-Phase™ fault type indication for phase 1. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection
11:8	PWM2_FAULTS	Intelli-Phase™ fault type indication for phase 2. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection
7:4	PWM3_FAULTS	Intelli-Phase™ fault type indication for phase 3. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection
3:0	PWM4_FAULTS	Intelli-Phase™ fault type indication for phase 4. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection

**MFR\_FAULTS4 (A9h)**

This command on page 1 returns the Intelli-Phase™ fault type information. The MP2975 does not offer 5-phase or 6-phase operation for rail 2.

Command	MFR_FAULTS4															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM5_FAULTS				PWM6_FAULTS				PWM7_FAULTS				PWM8_FAULTS			

Bits	Bit Name	Description
15:12	PWM5_FAULTS	Intelli-Phase™ fault type indication for phase 5. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection

11:8	PWM6_FAULTS	Intelli-Phase™ fault type indication for phase 6. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection
7:4	PWM7_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 7, or rail 2's phase 6. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection
3:0	PWM8_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 8, or rail 2's phase 5. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current limit protection 4'b0100: Over-temperature protection (OTP) 4'b1000: SW-PGND short protection

**MFR\_FAULTS5 (AAh)**

This command on page 1 returns the Intelli-Phase™ fault type information. The MP2975 does not offer 9-phase, 10-phase, 11-phase, or 12-phase operation for rail 1.

Command	MFR_FAULTS5															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	PWM9_FAULTS				PWM10_FAULTS				PWM11_FAULTS				PWM12_FAULTS			

Bits	Bit Name	Description
15:12	PWM9_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 9, or rail 2's phase 4. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM10_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 10, or rail 2's phase 3. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM11_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 11, or rail 2's phase 2. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection

3:0	PWM12_FAULTS	Intelli-Phase™ fault type indication for rail 1's phase 12, or rail 2's phase1. 4'b0000: No fault 4'b0001: VIN-SW short 4'b0010: Current-limit protection 4'b0100: Over-temperature protection 4'b1000: SW-PGND short protection
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### MFR\_CRC\_NORMAL\_CODE (ABh)

This command on page 1 returns the CRC calculation result based on the last store process of page 0 and page 1 non-trim registers.

Command	MFR_CRC_NORMAL_CODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	CRC_NORMAL_CODE															

Bits	Bit Name	Description
15:0	CRC_NORMAL_CODE	Returns the CRC calculation result based on the last store processes of page 0 and page 1 non-trim registers.

### MFR\_CRC\_MULTI\_CONFIG (ADh)

This command on page 1 returns the CRC calculation result based on the last storing process for page 2's multi-configuration registers.

Command	MFR_CRC_MULTI_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	CRC_MULTI_CONFIG															

Bits	Bit Name	Description
15:0	CRC_MULTI_CONFIG	Returns the CRC calculation result based on the last store process for page 2's multi-configuration registers.

### MFR\_VR\_CONFIG4 (B0h)

This command on page 1 sets some basic configurations for the MP297x.

Command	MFR_VR_CONFIG4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X									X				

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

12:11	EN_SIG_SEL	Selects the enable signal for rail 1 and rail 2. 2'b00: Select external EN1 (pin 13) as rail 1's enable pin, and select external EN2 (pin 33) as rail 2's enable pin 2'b01: Select rail 2's VRRDY2 as rail 1's enable pin, and select external EN1 (pin 33) as rail 2's enable pin 2'b10: Select external EN1 (pin 13) as rail 1's enable pin, and select rail 1's VRRDY1 signal as rail 2's enable 2'b11: Select external EN1 (pin 13) as both rail 1's and rail 2's enable pin
10	DRMOS_CS_TYPE_SEL	Selects the IOUT current-sense type of the DrMOS. 1'b0: Current source mode 1'b1: Voltage source mode
9	RESET_EN_2978	Enables VR shutdown behavior when the RESET# pin asserts. It is valid for both rail 1 and rail 2. This bit is only for the MP2978 . 1'b0: The VR does not shut down when the RESET# pin asserts 1'b1: The VR shuts down when the RESET# pin asserts
8	IMON_CATFLT_SEL	Enables the IMON signal output for observation. (IMON is multiplexed with another pin.) 1'b0: Disable, and IMON becomes CATFLT_SEL 1'b1: Enable, and VIMON can be observed
7	CATFLT_CLR_RESET_EN_2978	Enables CATFLT pin de-assertion when RESET# de-asserts. It is effective only when both bit[8] and bit[9] in this command are 0. This bit is only for the MP2978. 1'b0: RESET# de-assertion does not trigger CATFLT de-assertion 1'b1: RESET# de-assertion triggers CATFLT de-assertion
6	CATFLT_CLR_ONOFF_EN	Enables CATFLT de-assertion when the VR is power recycling in regular-power mode, EN is high, or the OPERATION command is on. It is only effective when bit[8] in this command = 0. 1'b0: CATFLT does not de-assert during power cycling 1'b1: CATFLT de-asserts during power cycling
5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4	CATFLT_OUT_SEL	Selects the CATFLT output status when it asserts. It is effective only when bit[8] in this command = 0. 1'b0: Assertion status is low 1'b1: Assertion status is Hi-Z
3	STANDBY_OUT_SEL	Selects the STANDBY output status when it asserts. It is only effective when bit[0] in this command = 1. 1'b0: STANDBY outputs low when it asserts 1'b1: STANDBY outputs Hi-Z when it asserts
2	STANDBY_PS4_EN	Enables STANDBY assertion when both rails are in PS4. It is only effective when bit[0] in this command = 1. 1'b0: Disable STANDBY assertion when the VR is in PS4 1'b1: Enable STANDBY assertion when the VR is in PS4
1	STANDBY_VR_OFF_EN	Enables STANDBY assertion when both rails are off, which can be caused by regular-power mode, EN off, or OPERATION command off. It is only effective when bit[0] in this command = 1. 1'b0: Disable STANDBY assertion when the VR is off 1'b1: Enable STANDBY assertion when the VR is off
0	STANDBY_ALTP_SEL	ALT#_P/STANDBY MUX configuration. 1'b0: ALT#_P 1'b1: STANDBY

### MFR\_PIN\_OFFSET (B1h)

This command on page 1 sets the PIN report offset.

Command	MFR_PIN_OFFSET															
Format	Two's complement binary format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	PIN_OFFSET							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	PIN_OFFSET	Sets the PIN report offset. It is in two's complement format. Bit[7] is the sign bit. 1W/LSB.

### RESERVED (B2h)

This command on page 1 is reserved. It's for ATE only.

### MFR\_CAT\_FLT\_MASK (B3h)

This command on page 1 masks the faults that assert CAT\_FLT. It is only effective when bit[8] of register MFR\_VR\_CONFIG4 (B0h on page 1) is 0.

Command	MFR_CAT_FLT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	LINE_FLOAT_MASK	1'b0: CAT_FLT does not assert when floating line protection occurs 1'b1: CAT_FLT assert when floating line protection occurs
12	CAT_PWR_IN_ALT_MASK	1'b0: CAT_FLT does not assert when input over-power occurs 1'b1: CAT_FLT asserts when input over-power occurs
11	VIN_OVP_MASK	1'b0: CAT_FLT does not assert when VIN over-voltage (OV) occurs 1'b1: CAT_FLT asserts when VIN OV occurs
10	VIN_UVLO_MASK	1'b0: CAT_FLT does not assert when VIN under-voltage lockout (UVLO) occurs 1'b1: CAT_FLT asserts when VIN UVLO occurs
9	TEN1 OTP MASK	1'b0: CAT_FLT does not assert when TSEN1 over-temperature protection (OTP) occurs 1'b1: CAT_FLT asserts when TSEN1 OTP occurs
8	CHIP OTP MASK	1'b0: CAT_FLT does not assert when chip over-temperature (OT) occurs 1'b1: CAT_FLT asserts when chip OT occurs
7	TSEN2_ANA_FLT_MASK	1'b0: CAT_FLT does not assert when a TSEN2 analog fault occurs 1'b1: CAT_FLT asserts when a TSEN2 analog fault occurs
6	TSEN2_DGLT_FLT_MASK	1'b0: CAT_FLT does not assert when a TSEN2 digital fault occurs 1'b1: CAT_FLT asserts when a TSEN2 digital fault occurs
5	PSYS_ANA_FLT_MASK	1'b0: CAT_FLT does not assert when a PSYS analog fault occurs 1'b1: CAT_FLT asserts when a PSYS analog fault occurs

4	PSYS_DGLTFLT_MASK	1'b0: CAT_FLT does not assert when a PSYS digital fault occurs 1'b1: CAT_FLT asserts when a PSYS digital fault occurs
3	OVP_MASK	1'b0: CAT_FLT does not assert when VOUT over-voltage protection (OVP) occurs 1'b1: CAT_FLT asserts when VOUT OVP occurs
2	UVP_MASK	1'b0: CAT_FLT does not assert when VOUT under-voltage protection (UVP) occurs 1'b1: CAT_FLT asserts when VOUT UVP occurs
1	OCP_MASK	1'b0: CAT_FLT does not assert when over-current protection (OCP) occurs 1'b1: CAT_FLT asserts when OCP occurs
0	DRMOS_FLT_MASK	1'b0: CAT_FLT does not assert when a DrMOS fault occurs 1'b1: CAT_FLT asserts when a DrMOS fault occurs

### MFR\_PSYS\_LEVEL (B4h)

This command on page 1 sets the reference voltage of the PSYS analog fault comparator. It is only effective when bit[3] of register MFR\_VR\_CONFIG3 (35h on page 1) is 1.

Command	MFR_PSYS_LEVEL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PIN_OFFSET_TUNE1										PSYS_LEVEL					

Bits	Bit Name	Description
15:10	PIN_OFFSET_TUNE1	Sets the PIN report offset when the calculated PIN exceeds 1024W. This value is added to PIN to form the final PIN report. It is in two's complement format. Bit[15] is the sign bit. 2W/LSB.
9:8	TON_PRD_FIL_SEL	Time constant for the digital low-pass filter to sense PWM on-time and frequency, which are used to calculate efficiency.  2'b00: (500k / fs) x 6ms 2'b01: (500k / fs) x 12ms 2'b10: (500k / fs) x 24ms 2'b11: (500k / fs) x 48ms  fs is the configured PWM frequency with register MFR_FS (5Ch on page 0 and page 1).
7:0	PSYS_LEVEL	Sets the PSYS analog fault threshold. 6.25mV/LSB.

### MFR\_PIN\_OFFSET\_TUNE2 (B5h)

This command on page 1 tunes the input power report.

Command	MFR_PIN_OFFSET_TUNE2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PIN_OFFSET_TUNE2						PIN_OFFSET_TUNE5						PIN_OFFSET_TUNE6			

Bits	Bit Name	Description
15:10	PIN_OFFSET_TUNE2	Sets the PIN report offset when the calculated PIN is between 512W and 1024W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[15] is the sign bit. 2W/LSB.

9:5	PIN_OFFSET_TUNE5	Sets the PIN report offset when the calculated PIN is between 64W and 128W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[9] is the sign bit. 1W/LSB.
4:0	PIN_OFFSET_TUNE6	Sets the PIN report offset when the calculated PIN is between 32W and 64W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[4] is the sign bit. 0.5W/LSB.

### MFR\_PIN\_OFFSET\_TUNE3 (B6h)

This command on page 1 tunes the input power report.

Command	MFR_PIN_OFFSET_TUNE3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PIN_OFFSET_TUNE3						PIN_OFFSET_TUNE7						PIN_OFFSET_TUNE8			

Bits	Bit Name	Description
15:10	PIN_OFFSET_TUNE3	Sets the PIN report offset when the calculated PIN is between 256W and 512W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[15] is the sign bit. 1W/LSB.
9:5	PIN_OFFSET_TUNE7	Sets the PIN report offset when the calculated PIN is between 16W and 32W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[9] is the sign bit. 0.5W/LSB.
4:0	PIN_OFFSET_TUNE8	Sets the PIN report offset when the calculated PIN is between 8W and 16W. This value will be added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[4] is the sign bit. 0.25W/LSB.

### MFR\_PIN\_OFFSET\_TUNE4 (B7h)

This command on page 1 tunes the input power report.

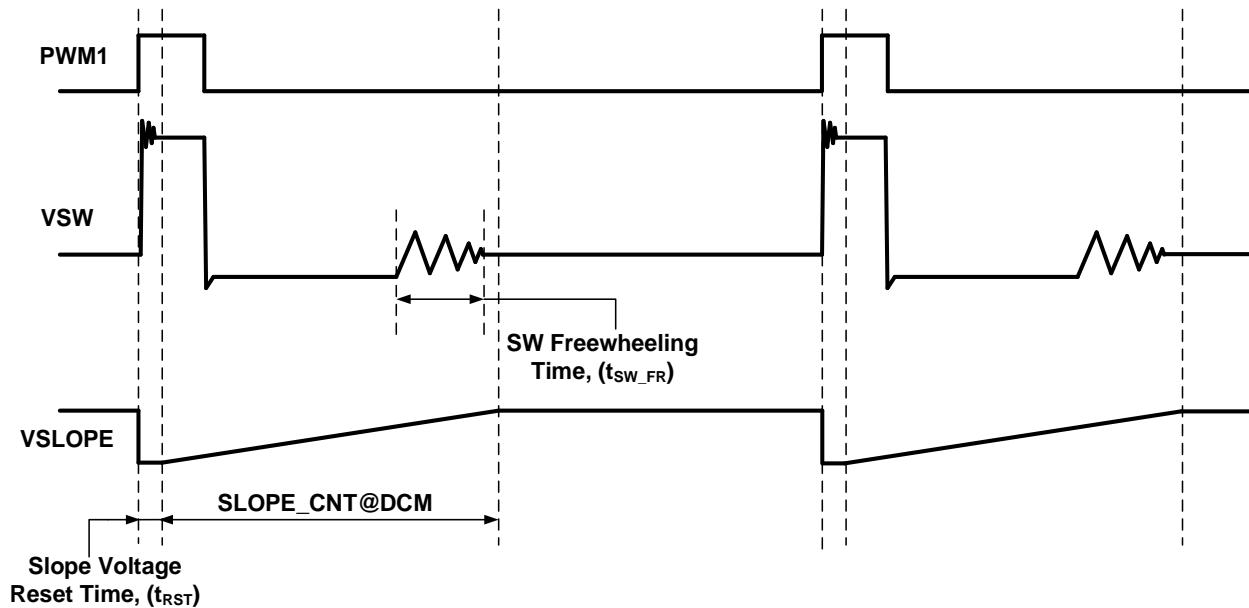
Command	MFR_PIN_OFFSET_TUNE4															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PIN_OFFSET_TUNE4						PIN_OFFSET_TUNE9						PIN_OFFSET_TUNE10			

Bits	Bit Name	Description
15:10	PIN_OFFSET_TUNE4	Sets the PIN report offset when the calculated PIN is between 128W and 256W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[14] is the sign bit. 1W/LSB.
9:5	PIN_OFFSET_TUNE9	Sets the PIN report offset when the calculated PIN is between 4W and 8W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[9] is the sign bit. 0.25W/LSB.
4:0	PIN_OFFSET_TUNE10	Sets the PIN report offset when the calculated PIN is less than 4W. This value is added to the calculated PIN to form a final PIN report. It is in two's complement format. Bit[4] is the sign bit. 0.25W/LSB.

### MFR\_SLOPE\_SR\_CNT\_DCM\_R1 (B8h)

This command on page 1 sets the slope compensation slew rate for rail 1 during 1-phase DCM. Calculate the slope slew rate using Equation (20) with CAP = 0. It also sets the slope clamp time during 1-phase DCM.

During 1-phase DCM, the off time increases to reduce the switching frequency as the load current decreases. The slope voltage clamp time should be long enough to avoid the SW node freewheeling period when the zero-current detection (ZCD) turns off the low-side MOSFET to transit the SW node to Hi-Z (see Figure 32).



**Figure 32: Slope Voltage Compensation during DCM**

Use Equation (27) to calculate the slope clamp time for DCM operation:

$$t_{\text{SLOPE\_CLAMP @ DCM}} = 1.1 \times \left( \frac{1}{f_{\text{sw}}} - t_{\text{RST}} + t_{\text{SW\_FR}} \right) \quad (27)$$

Where  $t_{\text{SLOPE\_CLAMP @ DCM}}$  is the slope clamp time in 1-phase DCM (in s),  $t_{\text{sw}}$  is the single-phase switching period set with command MFR\_FS (5Ch on page 0 and page 1) (in s),  $t_{\text{BLANK}}$  is the PWM blanking time set with command MFR\_BLANK\_TIME (69h, 6Ah, and 72h, on page 0 and page 1) (in s), and  $t_{\text{SW\_FR}}$  is the SW node freewheeling time (in s).

Command	MFR_SLOPE_SR_CNT_DCM_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	SLOPE_CNT															

Bits	Bit Name	Description
15:6	SLOPE_CNT	Sets the slope voltage clamp time for 1-phase DCM operation. 5ns/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25μA/LSB.

#### MFR\_SLOPE\_SR\_CNT\_DCM\_R2 (B9h)

This command on page 1 sets the slope compensation slew rate for rail 2 during 1-phase DCM. Calculate the slope slew rate with Equation (23) when CAP = 0. It also sets the slope clamp time during 1-phase DCM.

Command	MFR_SLOPE_SR_CNT_DCM_R2														
Format	Unsigned binary														

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Function	SLOPE_CNT												CURRENT_SOURCE				

Bits	Bit Name	Description
15:6	SLOPE_CNT	Sets the slope voltage clamp time for 1-phase DCM operation. 5ns/LSB.
5:0	CURRENT_SOURCE	Sets the current-source value for slope compensation. 0.25µA/LSB.

### PVID\_VID12\_R1 (BAh)

This command on page 1 programs the rail 1 PVID voltage during PVID override.

Command	PVID_VID12_R1															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID2_R1															

Bits	Bit Name	Description
15:8	PVID_VID2_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b001. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID1_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b000. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### PVID\_VID34\_R1 (BBh)

This command on page 1 programs the rail 1 PVID voltage during PVID override.

Command	PVID_VID34_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID4_R1															

Bits	Bit Name	Description
15:8	PVID_VID4_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b011. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID3_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b010. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### PVID\_VID56\_R1 (BCh)

This command on page 1 programs the rail 1 PVID voltage during PVID override.

Command	PVID_VID56_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID6_R1															

Bits	Bit Name	Description
15:8	PVID_VID6_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b101. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID5_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b100. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### PVID\_VID78\_R1 (BDh)

This command on page 1 programs the rail 1 PVID voltage during PVID override.

Command	PVID_VID78_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID8_R1															PVID_VID7_R1

Bits	Bit Name	Description
15:8	PVID_VID8_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b111. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID7_R1	Sets the rail 1 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b110. It is in VID format. The VID resolution is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2). 1 VID step/LSB.

### PVID\_VID12\_R2 (BEh)

This command on page 1 programs the rail 2 PVID voltage during PVID override.

Command	PVID_VID12_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID2_R2															PVID_VID1_R2

Bits	Bit Name	Description
15:8	PVID_VID2_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b001. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID1_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b000. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### PVID\_VID34\_R2 (BFh)

This command on page 1 programs the rail 2 PVID voltage during PVID override.

Command	PVID_VID34_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID4_R2															PVID_VID3_R2

Bits	Bit Name	Description
15:8	PVID_VID4_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b011. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID3_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3=3'b010. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### PVID\_VID56\_R2 (C0h)

This command on page 1 programs the rail 2 PVID voltage during PVID override.

Command	PVID_VID56_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID6_R2															

### PVID\_VID6\_R2 (C0h)

This command on page 1 programs the rail 2 PVID voltage during PVID override.

Bits	Bit Name	Description
15:8	PVID_VID6_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b101. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID5_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b100. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### PVID\_VID78\_R2 (C1h)

This command on page 1 programs the rail 2 PVID voltage during PVID override.

Command	PVID_VID78_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PVID_VID8_R2															

### PVID\_VID8\_R2 (C1h)

This command on page 1 sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b111. It is in VID format. The VID resolution is determined by bit[3] of register MFR\_VR\_MULTI\_CONFIG\_R2 (1Dh on page 2). 1 VID step/LSB.

Bits	Bit Name	Description
15:8	PVID_VID8_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b111. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.
7:0	PVID_VID7_R2	Sets the rail 2 PVID voltage when pins PVID1, PVID2, and PVID3 = 3'b110. It is in VID format. The VID resolution is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2). 1 VID step/LSB.

### SVID\_VOUT\_MAX (C2h)

This command on page 1 sets the maximum VID in SVID command that rail 2 supports. If a higher VID code is received, the VR responds to the request with an SVID reject acknowledgement.

Command	SVID_VOUT_MAX																						
Format	VID																						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Function	X	X	X	X	X	X	X	X	SVID_VOUT_MAX														

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	SVID_VOUT_MAX	Sets the maximum VID in SVID command that rail 2 supports. It is only effective when rail 2 is in SVID mode. 1 VID step/LSB.

### SVID\_VR\_TOLERENCE\_PS4\_DLY (C3h)

This command on page 1 sets the Intel VR13-specified rail 2 VR TOLERANCE. It also has bits to set the delay time to exit PS4.

Command	SVID_VR_TOLERENCE_PS4_DLY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	PS4_DELAY_TIME										TEMP_OFFSET_SVID	

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	PS4_DELAY_TIME	Sets the delay time to exit PS4. This value is valid for both rails. Each rail has an independent resolution that is determined by bit[14] of PMBus command MFR_VR_CONFIG2 (76h on page 0 and page 1), ON/OFF_DLY_CLK_SEL. Ensure the resolution is same both on page 0 and page 1, or the rails will not have the same delay time. 20µs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50µs/LSB (ON/OFF_DLY_CLK_SEL = 1)
7:0	VR_TOLERANCE_R2	Data register containing the VR TOB for rail 2 based on board parts (e.g. inductor DCR, inductance tolerance, and current-sense errors). 1mV/LSB.

### SVID\_TEMP\_OFFSET (C4h)

This command on page 1 sets the temperature offset for SVID telemetry.

Command	SVID_TEMP_OFFSET															
Format	Two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	SVID_TEMP_OFFSET							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	SVID_TEMP_OFFSET	Default value for SVID register T_OFFSET (29h). Sets the temperature offset added to SVID telemetry (17h). 1°C/LSB.

### MFR\_VR\_CONFIG5 (C6h)

This command on page 1 sets some debugging configurations for the MP297x.

Command	MFR_VR_CONFIG5															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function											X					

Bits	Bit Name	Description
15	REG_22_SEL	1'b1: Register 22h of page 0 and page 1 is used for VOUT_TRIM 1'b0: Register 22h of page 0 and page 1 is used for MFR_IDROOP_OFFSET
14	OC_PHASE_SS_EN	Enables OCP_PHASE limitation during soft start. It is valid for both rails. 1'b0: Disable OCP_PHASE limitation during soft start 1'b1: Enable OCP_PHASE limitation during soft start
13:12	OC_PHASE_PWM_BLANK_TIME	Sets the PWM set signal blanking time when the OCP_Phase limit is tripped. If the phase current exceeds OCP_PHASE after the set PWM blanking time, the present phase is skipped, and the next phase turns on. The set time is active for both rails. 20ns/LSB with 15ns offset.  BLANK_TIME = 20ns / LSB x OCP_PHASE_SET + 15ns
11	ADDR_PL_SEL	Selects whether the PMBus address 4LSB is set by the ADDR_PL pin or by the register. 1'b1: PMBus address 4LSB is set by the ADDR_PL pin 1'b0: PMBus address 4LSB is set by bit[11:8] of register MFR_ADDR_IIN_OFFSET (1Ah on page 2)
10	MUL_CONFIG_EN	Disable multi-configuration during the MTP copying process. 1'b1: Disable multi-configuration. The device copies the first sets of configuration from the MTP to operation registers, regardless of the voltage on CONFIG 1'b0: Enable multi-configuration function. The device copies the CONFIG pin defined sets of configuration from the MTP to the operation registers
9	PHSHED_TON_MODE	Sets the PWM pulse behavior during phase-shedding. 1'b0: During the last switching cycle before phase-shedding, PWM produces a normal-width pulse and then goes to tri-state 1'b1: During the last switching cycle before phase-shedding, PWM produces a pulse half the normal-width pulse, and then goes to tri-state
8	OVP_DISCH_MODE	Sets the PWM behavior after over-voltage protection (OVP) occurs. 1'b0: If OVP occurs, all PWMs are pulled low until Vo drops below the reverse-voltage protection (RVP) threshold. Then all PWMs remain in tri-state, regardless of whether Vo exceeds the RVP threshold again 1'b1: If OVP occurs, all PWMs are pulled low for as long as Vo exceeds the RVP threshold.
7	UCP_EN	Enables under-current protection (UCP). It is valid for both rails. 1'b0: Disable UCP 1'b1: Enable UCP
6	VID_>2LSB_ALT_MODE	Selects the SVID ALT# behavior when the DVID step exceeds 2 steps. It is only effective when the VID resolution is 5mV/step. 1'b0: ALT# asserts after VR_SETTLE 1'b1: ALT# asserts 2 VID steps before VR_SETTLE
5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4	DIS_PHSHED_EN	Follows the PS behavior. It is only valid when phase-shedding is set to follow the set PS (bit[14:13] for rail 2, and bit[8:7] for rail 1, is 2'b10). 1'b1: Disable phase-shedding. The VR operates in full-phase mode except during PS4 and decay conditions, and acknowledgement. All PS commands are set at the same time 1'b0: VR follows the PS command
3:2	DECAY_LENGTH_R2	Sets the maximum time for each VID step during decay mode for rail 1. It sets the minimum decay slew rate. VID is forced to ramp down 1 VID step when the present VID lasts for longer than the time set by DECAY_LENGTH. 100ns/LSB.

1:0	DECAY_LENGTH_R1	Sets the maximum time for each VID step during decay mode for rail 2. It sets the minimum decay slew rate. VID is forced to ramp down 1 VID step when the present VID step lasts for longer than the time set by DECAY_LENGTH. 100ns/LSB.
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**PWD\_LOCK\_TOG (D0h)**

This command on page 1 locks the PMBus interface from reading or writing. This user can unlock the PMBus interface by inputting the correct password using PMBus command PWD\_CHECK\_CMD (F8h on page 0). PMBus read or write access is determined by bit[6] and bit[7] of the PMBus command MFR\_MTP\_PMBUS\_CTRL (C5h on page 0).

This command is write-only. There is no data byte for this command.

**SVID\_LAST\_CMD\_DATA (E1h)**

This command on page 1 returns the last SVID command and the data for rail 2.

Command	SVID_LAST_CMD_DATA																
Format	Direct																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Function	X	X	X	SVID_LAST_CMD										SVID_LAST_DATA			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:8	SVID_LAST_CMD	Last SVID command.
7:0	SVID_LAST_DATA	Data associated with the last SVID command.

**SVID\_SECOND\_LAST\_CMD\_DATA (E2h)**

This command on page 1 returns the second-to-last SVID command, and the data for rail 2.

Command	SVID_SECOND_LAST_CMD_DATA																
Format	Direct																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Function	X	X	X	SVID_SECOND_LAST_CMD										SVID_SECOND_LAST_DATA			

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:8	SVID_SECOND_LAST_CMD	Second to last SVID command.
7:0	SVID_SECOND_LAST_DATA	Data associated with the second to last SVID command.

**MFR\_OVP\_TH\_SET (E5h)**

This command on page 1 sets the protection threshold for rail 1 and rail 2 over-voltage protection (OVP1 and OVP2, respectively).

Command	MFR_OVP_TH_SET																			
Format	Unsigned binary																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Function	X	X	X	X	X	X	X	X	X	X										

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:3	OVP2_THRESHOLD_SET	<p>Selects VOUT over-voltage protection (OVP2) threshold.  The OVP2 threshold is decided by OVP2_THRESHOLD, and coefficient a and b:</p> <p>3'b100: OVP2 threshold = VREF + 400mV x a x b  3'b010: OVP2 threshold = VREF + 220mV x a x b  3'b001: OVP2 threshold = VREF + 140mV x a x b  Others: Invalid</p> <p>a = 1 with remote-sense amplifier unit gain  a = 2 with remote-sense amplifier half-gain</p> <p>Coefficient b is determined by PRT_THRES_DIV_EN, which is MFR_ADV (56h on page 1), bit[14].</p> <p>b = 1 with PRT_THRES_DIV_EN = 0  b = 0.5 with PRT_THRES_DIV_EN = 1</p>
2:0	OVP1_THRESHOLD_SET	<p>Sets the over-voltage protection (OVP1) threshold, which is referred to VOUT_MAX. 50mV/LSB. The OVP1 threshold can be calculated with the following equation:</p> $VOUT\_MAX + 50mV \times (OVP1\_TH\_SET+1)$

### MFR\_UVP\_SET (E6h)

This command on page 1 sets the under-voltage protection (UVP) threshold for rail 2.

Command	MFR_UVP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X				

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3	UVP_PRT_SEL	<p>Selects the voltage point for VOUT under-voltage protection (UVP).</p> <p>1'b0: Select VDIFF as the VOUT UV protection point  1'b1: Select VFB as the VOUT UV protection point</p>
2:0	UVP_THRESHOLD_SET	<p>Sets the VOUT under-voltage protection (UVP), which is referred to the VID voltage. The UVP threshold is affected by PRT_THRES_DIV_EN, which is MFR_ADV (56h on page 1), bit[14]. 50mV/LSB. The UVP threshold can be calculated with the following equation:</p> $VID - 50mV \times (UVP\_TH\_SET + 1) \times a \times b$ <p>Coefficient a is determined by the remote-sense amplifier gain, which is the value of VOUT_SCALE_SET (29h on page 1), bit[11].</p> <p>a = 1 with remote-sense amplifier unit gain  a = 2 with remote-sense amplifier half gain</p> <p>Coefficient b is determined by PRT_THRES_DIV_EN, which is MFR_ADV (56h, page 1), bit[14].</p> <p>b = 1 with PRT_THRES_DIV_EN = 0  b = 0.5 with PRT_THRES_DIV_EN = 1</p>

**STORE\_NORMAL\_CODE (F1h)**

This command on page 1 instructs the PMBus device to copy the page 0 and page 1 contents to their matching locations in the MTP, excluding their trim registers. During the copying process, the device calculates a CRC code for all saved bits in the MTP. The CRC code checks whether the data is valid during the next start-up or restore.

This command is write-only. There is no data byte for this command.

**RESTORE\_NORMAL\_CODE (F2h)**

This command on page 1 instructs the PMBus device to copy the page 0 and page 1 contents from the MTP and overwrite their matching locations in the operating memory. Trim registers are excluded. During this process, the device calculates the CRC for all restored bits. If the calculated CRC does not match the CRC value saved in the MTP, the device reports a CRC error via bit[4] of register STATUS\_CML (7Eh).

**CLEAR\_CATFAULTS (FDh)**

This command on page 1 de-asserts the IMON/CAT\_FLT pin. It is only effective when register MFR\_VR\_CONFIG4 (B0h on page 1) is bit[8] = 0.

This command is write-only. There is no data byte for this command.

**CLEAR\_STOREFAULTS (FEh)**

This command on page 1 clears the last fault information that is stored in the MTP page2A, C0h, C1h, C2h, C3h, and C4h.

This command is write-only. There is no data byte for this command.

**CLEAR\_MTPFAULTS (FFh)**

This command on page 1 clears the MTP faults.

This command is write-only. There is no data byte for this command.

## REGISTER MAP (PAGE 2)

### PAGE (00h)

This command on page2 provides the ability to configure, control and monitor all registers including test mode and MTP through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	PAGE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	PAGE	<p>Registers page selector.</p> <p>0x00: Page 0, all PMBus commands address the operating registers on page 0      0x01: Page 1, all PMBus commands address the operating registers on page 1      0x02: Page 2, all PMBus commands address the operating multi-configuration registers on page 2      0x03: Page 3, all PMBus commands address the test mode registers      0x28: Page 28, all PMBus commands address the MTP registers that are mapped to the operating registers on page 0      0x29: Page 29, all PMBus commands address the MTP registers that are mapped to the operating registers on page 1      0x2A: Page 2A, all PMBus commands address the MTP registers that are mapped to the operating multi-configuration registers on page 2      Others: Ineffective input</p> <p>Note: MTP_BYTWR_EN, bit[2] of MFR_MTP_CTRL (C5h), determines whether Pages 28, 29, and 2A is accessible or not.</p> <p>MTP_BYTWR_EN = 0: Pages 28, 29, and 2A are not accessible      MTP_BYTWR_EN = 1: Pages 28, 29, and 2A are accessible</p>

### MFR\_HC\_SLEW\_RATE\_SET\_R1 (01h)

This command on page 2 sets some VR13.HC-related configurations for the MP297x. It is only for rail 1.

Command	MFR_HC_SLEW_RATE_SET_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X														

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	VR13_HC_SUPPORT	1'b0: VR13.HC mode not supported 1'b1: VR13.HC mode supported
12	VR13_HC_ACTIVE_INI	Enables VR13.HC initially. The CPU can enable or disable VR13.HC mode with the SVID command SLOW SLEW SELECTOR (2Ah). Per VR13.HC specifications, the default option is 1'b0.  1'b0: Disable VR13.HC initially 1'b1: Enable VR13.HC initially. The parameter setting for VR13.HC is effective and is returned to the SVID interface

11:8	SLEW_SLOW_SR	Sets the VID slow slew rate. 4'b1xxx: SLEW_SLOW_SR = FAST_SR / 16 4'b01xx: SLEW_SLOW_SR = FAST_SR / 8 4'b001x and 4'b0000: SLEW_SLOW_SR = FAST_SR / 4 4'b0001: SLEW_SLOW_SR = FAST_SR / 2 “x” means not applicable Where FAST_SR is the VID fast slew rate defined in register bit[7:0] in this command.
7	AC_DC_DROOP_SEL	Selects DC or AC droop injection. 1'b0: DC droop injection 1'b1: AC droop injection
6	LPF_GAIN_SET	Sets the resistor for droop compensation. 1'b0: 0.83kΩ 1'b1: 1.66kΩ
5:0	SLEW_FAST_CNT	Sets the VID fast slew rate by setting the time interval of each VID step. It is in direct format. 50ns/LSB. The slew rate can be calculated with the following equation: $\text{FAST_SR(mV/}\mu\text{s)} = \frac{\text{VID\_STEP(mV)}}{\text{SLEW\_FAST\_CNT} \cdot 0.05(\mu\text{s})}$ Where VID_STEP is in 5mV or 10mV. It is determined by bit[4] of register MFR_VR_MULTI_CONFIG_R1 (0Dh on page 2).

**MFR\_ICC\_MAX\_R1 (02h)**

This command on page 2 sets the  $I_{CCMAX}$  value for rail 1. It also sets the VR14 specified HIGH\_PWR register.

Command	MFR_ICC_MAX_R1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description																			
		VR14										VR13.HC and earlier									
15:13	W_PER_BIT_IN/ ICC_MAX_ADD [7:5]	<b>W_PER_BIT_IN</b> Corresponds to the VR14-specified high-current capability register (SVID register 50h) bit[4:2], for the PSYS rail only. Sets the step input power telemetry. Applies to PwrIn Max (SVID register 2Eh). Input power: 3'b000: 2W/LSB 3'b001: 4W/LSB 3'b010: 8W/LSB 3'b011: 16W/LSB Others: Unsupported																			
		<b>ICCMAX_ADD</b> Sets the VR13.HC SVID maximum report current 8HSB, (ICCMAX_ADD). For VR13.HC, the maximum SVID reported current can be calculated with the following equation: $\text{ICCMAX\_VR13.HC} = \text{ICCMAX} + \text{ICCMAX\_ADD} \times 2$ 2A/LSB.																			

12:10	W_PER_BIT_OUT/ ICC_MAX_ADD [4:2]	<b>W_PER_BIT_OUT</b>  Corresponds to the VR14-specified high-current capability register (SVID register 50h), bit[4:2]. Sets the step input and output power telemetry. Applies to the output power telemetry (SVID register 18h).  Output power:  3'b000: 1W/LSB 3'b001: 2W/LSB 3'b010: 4W/LSB 3'b011: 8W/LSB Others: Unsupported	
9:8	A_PER_BIT_OUT/ ICC_MAX_ADD [1:0]	<b>A_PER_BIT_OUT</b>  Corresponds to the VR14-specified high-current capability register (SVID register 50h), bit[1:0]. Sets the step of the ICC_MAX register (SVID reg 21h).  2'b00: 1A/LSB 2'b01: 2A/LSB 2'b10: 4A/LSB 2'b11: 8A/LSB	
7:0	ICCMAX	Sets the VR14 SVID maximum report current (FFh). The output will not boot if ICCMAX is set to 0. The resolution is set by bit[9:8] in this command.	Sets the VR13 SVID maximum report current (FFh) and the VR13.HC SVID maximum report current 8LSB. The output will not boot if ICCMAX is set to 0.1A/LSB.

**SVID\_CAPABILITY\_DC\_LL\_R1 (03h)**

This command on page 2 sets the Intel-specified CAPABILITY and DC\_LL. It is only for rail 1.

Command	SVID_CAPABILITY_DC_LL_R1																							
Format	Binary																							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Function	DC_LL								CAPABILITY															
15:8	DC_LL			Data register containing the programmed load line or AVP of the platform based on the output capacitance and $R_{PATH}$ . If the PWM IC supports resistor LL or AVP programming, this register is not used. The master does not read this register. 0.1mΩ/LSB.																				
7:0	CAPABILITY			The bitmapped register identifies which of the SVID optional telemetry registers are supported. The values are returned to SVID register 06h.  00h indicates only required registers are supported.  Bit[15] = 1, output current reported as a fraction of ICCMAX Bit[14] = 1, support temperature ADC (17h) Bit[13] = 1, support $V_{IN}$ ADC (1Ah) Bit[12] = 1, support $I_{IN}$ ADC (19h) Bit[11] = 1, support $P_{OUT}$ ADC (18h) Bit[9] = 1, support $V_{OUT}$ ADC (16h) Bit[8] = 1, support $I_{OUT}/J_{OUT}$ ADC format for pre-VR13 CPUs, and output current ADC for VR13 CPUs and more recent (15h)																				

Bits	Bit Name	Description
15:8	DC_LL	Data register containing the programmed load line or AVP of the platform based on the output capacitance and $R_{PATH}$ . If the PWM IC supports resistor LL or AVP programming, this register is not used. The master does not read this register. 0.1mΩ/LSB.
7:0	CAPABILITY	The bitmapped register identifies which of the SVID optional telemetry registers are supported. The values are returned to SVID register 06h.  00h indicates only required registers are supported.  Bit[15] = 1, output current reported as a fraction of ICCMAX Bit[14] = 1, support temperature ADC (17h) Bit[13] = 1, support $V_{IN}$ ADC (1Ah) Bit[12] = 1, support $I_{IN}$ ADC (19h) Bit[11] = 1, support $P_{OUT}$ ADC (18h) Bit[9] = 1, support $V_{OUT}$ ADC (16h) Bit[8] = 1, support $I_{OUT}/J_{OUT}$ ADC format for pre-VR13 CPUs, and output current ADC for VR13 CPUs and more recent (15h)

**SVID\_SR\_FAST\_SR\_SLOW\_R1 (04h)**

This command on page 2 sets the Intel specified rates for SR\_FAST and SR\_SLOW. It is only for rail 1.

<b>Command</b>	SVID_SR_FAST_SR_SLOW_R1															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	SR_SLOW								SR_FAST							

Bits	Bit Name	Description
15:8	SR_SLOW	Data register containing the capability of rail 1's slow slew rate. 1(mV/μs)/LSB.
7:0	SR_FAST	Data register containing the fast slew rate capability that rail 1 can sustain. 1(mV/μs)/LSB.

**MFR\_ADDR\_SVID\_AVSBUS (05h)**

This command on page 2 sets the SVID and AVS address for both rails.

<b>Command</b>	MFR_ADDR_SVID_AVSBUS															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	AVS_ADDR_EN2	Enables the AVSBus address for rail 2. 1'b0: Disable the AVSBus address for rail 2 1'b1: Enable the AVSBus address for rail 2
11	AVS_ADDR_EN1	Enables AVSBus address for rail 1. 1'b0: Disable the AVSBus address for rail 1 1'b1: Enable the AVSBus address for rail 1
10:9	SVID_ALLCALL_CTRL	Selects the SVID all-call address. 2'b00: No all-call address 2'b01: Set SVID address 0x0E as all-call address 2'b10: Set SVID address 0x0F as all-call address 2'b11: Set SVID address 0x0E and 0x0F as all-call addresses
8:4	ADDR_OFFSET	Sets the rail 2 SVID/AVSBus address offset based on rail 1. It is in two's complement format. The rail 2 SVID/AVSBus address can be calculated with the following equation:  $\text{ADDRS\_R2} = \text{ADDRS\_R1} + \text{ADDR\_OFFSET} + 1$ The values below list the binary data and real-world address offset: 5'b 0 0000: 0 5'b 0 0001: 1 5'b 0 1111: 15 5'b 1 0000: -16 5'b 1 0001: -15 5'b 1 1111: -1
3:0	SVID_AV_SADDR1	Sets the SVID/AVSBus address from the register.

**MFR\_IDROOP\_CTRL1\_R1 (06h)**

This command on page 2 sets the configurations related to the droop on rail 1.

Command	MFR_IDROOP_CTRL1_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description															
15:14	DROOP_TRIM_SET	2'b00: Select TRIM_IDROOP1 as the droop trim value 2'b01: Select TRIM_IDROOP2 as the droop trim value 2'b10: Select TRIM_IDROOP3 as the droop trim value 2'b11: Select TRIM_IDROOP4 as the droop trim value															
13	LPF2_EN	Enable bit for droop compensation component 2. 1'b0: Disable droop compensation component 2 1'b1: Enable droop compensation component 1															
12	LPF1_EN	Enable bit for droop compensation component 1. 1'b0: Disable droop compensation component 1 1'b1: Enable droop compensation component 2															
11	NON-LINEAR_AVG_EN	Enable bit for nonlinear AVP function 1'b0: Disable nonlinear AVP 1'b1: Enable nonlinear AVP															
10:9	RDROOP_SET	Sets the internal droop resistor value. 2'b00: 1000Ω 2'b01: 400Ω 2'b10: 235Ω 2'b11: Unconnected															
8	AC_DROOP_BW_SEL	Selects the bandwidth of AC droop regulation loop. It is only effective when bit[8] of register MFR_IDROOP_CTRL2_R1 (07h on page 2) = 1. <table border="1"> <tr> <th>DROOP_COMP_LOOP_BW (bit[10] 68h on Page 0)</th> <th>AC_DROOP_BW_SEL</th> <th>BW (Hz)</th> </tr> <tr> <td>0</td> <td>0</td> <td>25k</td> </tr> <tr> <td>0</td> <td>1</td> <td>50k</td> </tr> <tr> <td>1</td> <td>0</td> <td>250k</td> </tr> <tr> <td>1</td> <td>1</td> <td>500k</td> </tr> </table>	DROOP_COMP_LOOP_BW (bit[10] 68h on Page 0)	AC_DROOP_BW_SEL	BW (Hz)	0	0	25k	0	1	50k	1	0	250k	1	1	500k
DROOP_COMP_LOOP_BW (bit[10] 68h on Page 0)	AC_DROOP_BW_SEL	BW (Hz)															
0	0	25k															
0	1	50k															
1	0	250k															
1	1	500k															
7:0	IDROOP_GAIN_SET	Sets the internal current mirror gain of ( $I_{DROOP} / I_{CS\_SUM}$ ), which can be estimated with the following equation: $\frac{I_{DROOP}}{I_{CS\_SUM}} = \frac{IDROOP\_GAIN\_SET}{256}$ Where $I_{DROOP}$ is the current injected into the droop register to generate the droop voltage (in A), and $I_{CS\_SUM}$ is the total sensed current into the CS pin (in A).															

**MFR\_IDROOP\_CTRL2\_R1 (07h)**

This command on page 2 sets the configurations related to the rail 1 droop.

Command	MFR_IDROOP_CTRL2_R1	
Format	Direct	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W															
Function								X								

Bits	Bit Name	Description																					
15:12	LPF2_FIL_SET	Sets the RC filter parameter for droop compensation component 1. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs																					
11:8	LPF1_FIL_SET	Sets the RC filter parameter for droop compensation component 2. 4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03µs 4'b0110: 1.23µs 4'b0111: 1.42µs 4'b1000: 2.87µs 4'b1001: 3.16µs 4'b1010: 3.47µs 4'b1011: 3.74µs 4'b1100: 4.14µs 4'b1101: 4.40µs 4'b1110: 4.72µs 4'b1111: 4.98µs																					
7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.																					
6:0	VOUT_TRIM	Fine-tunes the output voltage. It is in two's complement format. The resolution is related to the VDIFF gain set by bit[11] of VOUT_SENSE_SET (29h on page 0). 0.5mV/LSB with VDIFF unit gain 0.8mV/LSB with VDIFF half-gain  The voltage table below shows the binary data and real-world values: <table border="1"> <thead> <tr> <th>VOUT_TRIM</th> <th>VDIFF Unit Gain</th> <th>VDIFF Half-Gain</th> </tr> </thead> <tbody> <tr> <td>7'b 000 0000</td> <td>0</td> <td>0</td> </tr> <tr> <td>7'b 000 0001</td> <td>0.5mV</td> <td>0.8mV</td> </tr> <tr> <td>7'b 011 1111</td> <td>31.5mV</td> <td>50.4mV</td> </tr> <tr> <td>7'b 100 0000</td> <td>-32mV</td> <td>-51.2mV</td> </tr> <tr> <td>7'b 100 0001</td> <td>-31.5mV</td> <td>-50.4mV</td> </tr> <tr> <td>7'b 111 1111</td> <td>-0.5mV</td> <td>-0.8mV</td> </tr> </tbody> </table>	VOUT_TRIM	VDIFF Unit Gain	VDIFF Half-Gain	7'b 000 0000	0	0	7'b 000 0001	0.5mV	0.8mV	7'b 011 1111	31.5mV	50.4mV	7'b 100 0000	-32mV	-51.2mV	7'b 100 0001	-31.5mV	-50.4mV	7'b 111 1111	-0.5mV	-0.8mV
VOUT_TRIM	VDIFF Unit Gain	VDIFF Half-Gain																					
7'b 000 0000	0	0																					
7'b 000 0001	0.5mV	0.8mV																					
7'b 011 1111	31.5mV	50.4mV																					
7'b 100 0000	-32mV	-51.2mV																					
7'b 100 0001	-31.5mV	-50.4mV																					
7'b 111 1111	-0.5mV	-0.8mV																					

**IOUT\_RPT\_GAIN\_SVID\_AVs\_R1 (08h)**

This command on page 2 sets the rail 1 IOUT report gain for the SVID and AVSBus interfaces.

Command	IOUT_RPT_GAIN_SVID_AVs_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	AVSBUS_GIMON_RES IMON_GAIN													

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:10	AVSBUS_GIMON_RES	<p>Selects the current-sense resolution for the AVSBus interface's IOUT report. It is only effective during AVSBus VID override. The resolution selection provides an intermediate variable that improves the AVSBus IOUT report accuracy. The final AVSBus IOUT report is always in 0.1A/LSB.</p> <p>4'b0001: 20mA/LSB, the maximum AVSBus report current is 41A          4'b0010: 40mA/LSB, the maximum AVSBus report current is 82A          4'b0100: 80mA/LSB, the maximum AVSBus report current is 164A          4'b1000: 160mA/LSB, the maximum AVSBus report current is 328A          4'b0000: 320mA/LSB, the maximum AVSBus report current is 656A          Other inputs are invalid.</p>
9:0	IMON_GAIN	<p>Sets the current-sense gain for SVID IOUT reporting and AVSBus IOUT reporting. In SVID override mode, calculate the IMON-sense gain with the following equation:</p> $\text{IMON\_GAIN} = 639 \times I_{\text{CCMAX}} \times K_{\text{CS}} \times G_{\text{IMON}} \times R_{\text{IMON}}$ <p><math>I_{\text{CCMAX}}</math> is the maximum current of Intel CPU (in A), <math>K_{\text{CS}}</math> is the Intelli-Phase™ current-sense gain (in A/A), <math>G_{\text{IMON}}</math> is the IMON current mirror gain selected by register MFR_IMON_DGTL_ANA_GAIN_R1 (0Ch on page 2) bit[12:11], and <math>R_{\text{IMON}}</math> is the internal IMON resistor (in Ω).</p> <p>In AVSBus VID override mode, the IMON-sense gain can be estimated with the following equation:</p> $\text{IMON\_GAIN} = \begin{cases} K_{\text{CS}} \times R_{\text{IMON}} \times G_{\text{IMON}} \times \frac{1023 \times 256}{1.6 \times 50} \times \text{AVSBUS\_GIMON\_RES} & \text{AVSBUS\_GIMON\_RES} > 0 \\ K_{\text{CS}} \times R_{\text{IMON}} \times G_{\text{IMON}} \times \frac{1023 \times 256}{1.6 \times 50} \times 16 & \text{AVSBUS\_GIMON\_RES} = 0 \end{cases}$ <p>Where <math>K_{\text{CS}}</math> is the Intelli-Phase™ current-sense gain (in A/A), <math>G_{\text{IMON}}</math> is the IMON current mirror gain selected by register MFR_IMON_DGTL_ANA_GAIN_R1 (0Ch on page 2) bit[12:11], <math>R_{\text{IMON}}</math> is the internal IMON resistor (in Ω), and <math>\text{AVSBUS\_GIMON\_RES}</math> is the decimal value set with bit[13:10].</p>

**MFR\_IIN\_CAL\_IMON\_OFFSET\_R1 (09h)**

This command on page 2 sets the offset for rail 1's SVID output current telemetry. It also provides bits to set the mode for input current and power calculation.

Command	MFR_IIN_CAL_IMON_OFFSET_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

12	R2_VINSEN_SEL	Selects the input voltage sense signal for rail 2. 1'b0: Select VINSEN1 as rail 2's input voltage sense 1'b1: Select PSYS/VINSEN2/VAUXSENSE as rail 2's input voltage sense
11:10	PIN_IIN_TOT_MODE	Selects the input current and power telemetry contents. It is only effective when bit[9] in this command = 1. 2'b01: Use rail 1's input current and power for the SVID/PMBus PIN telemetry 2'b10: Use rail 2's input current and power for the SVID/PMBus PIN telemetry 2'b11: Use the sum of rail 1 and rail 2's input current and power for the SVID/PMBus PIN telemetry
9	IIN_CAL_MODE	Sets the input current calculation mode. 1'b0: Use the PSYS pin's sensed value to calculate the input current 1'b1: Use the PWM on time and switching period to calculate the input current
8:0	IMON_OFFSET_SVID_AV_S_R1	Sets the SVID and AVSBus output current report offset. The value is in two's complement format. Bit[8] is the sign bit. The current resolution at SVID override mode can be calculated with the following equation: $(ICCMAX / 255) \text{ A / LSB}$ Where ICCMAX is the current value set with the PMBus command MFR_ICCMAX (BDh). The current resolution during AVSBus override follows the setting in IOUT_RPT_GAIN_SVID_AV_S_R1 (08h on page 2), bit[13:10].

**IOUT\_RPT\_GAIN\_HC\_R1 (0Ah)**

This command on page 0 sets the rail 1 IMON-sense gain for the VR13.HC output current report.

Command	IOUT_RPT_GAIN_HC_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IMON_GAIN_HC									

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON_GAIN_HC	Sets the IMON-sense gain for the VR13.HC IOUT report. In VR13 SVID override mode, calculate the IMON-sense gain with the following equation: $\text{IMON_GAIN_HC} = 639 \times I_{\text{CCMAX}} \times K_{\text{CS}} \times G_{\text{IMON}} \times R_{\text{IMON}}$ IccMAX is the maximum current of VR13.HC CPU (in A), Kcs is the Intelli-Phase™ current sense gain (in $\mu\text{A}/\text{A}$ ), GimON is the IMON current mirror gain, and RimON is the internal IMON resistor (in k $\Omega$ ).

**IOUT\_CAL\_GAIN\_PMBUS\_R1 (0Bh)**

This command on page 2 sets the gain for rail 1 output current PMBus reporting. The reported output current is returned with PMBus command READ\_IOUT (8Ch on page 0).

Command	IOUT_CAL_GAIN_PMBUS_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	IOUT_CAL_GAIN_PMBUS												

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:11	GAIN_SEL	Sets the exponent value for the equation to calculate IOUT_CAL_GAIN equation in this command.
10:0	IOUT_CAL_GAIN_PMBUS	Sets the current-sense gain for PMBus report. The sense gain can be calculated with the following equation:  $IOUT\_CAL\_GAIN\_PMBUS = \frac{512}{1.6} \times K_{CS} \times G_{IMON} \times R_{IMON} \times 2^{(11-GAIN\_SEL)}$ Where $K_{CS}$ is the Intelli-Phase™ current-sense gain (in A/A), $G_{IMON}$ is the IMON current mirror gain, $R_{IMON}$ is the internal IMON resistor (in Ω), and GAIN_SEL is bit[12:11] in this command.

### MFR\_IMON\_DGTL\_ANA\_GAIN\_R1 (0Ch)

This command on page 2 sets the rail 1 IMON current mirror gain and internal IMON resistor value. It also sets the digital calculaton gain for rail 1 IOUT reporting.

Command	MFR_IMON_DGTL_ANA_GAIN_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IMON_RES_SET											IMON_DGTL_GAIN				

Bits	Bit Name	Description
15:13	IMON_RES_SET	Sets the internal resistor value for IMON.  3'b100: 2.5kΩ 3'b101: 5kΩ 3'b110: 10kΩ 3'b111: 40kΩ others: Unconnected
12:11	IMON_GAIN_SET	Sets the current mirror gain from total CS current to IMON.  2'b00: 2/64 2'b01: 3/64 2'b10: 5/64 2'b11: 8/64
10:0	IMON_DGTL_GAIN	Sets the digital calculation gain for IOUT reporting. The gain is multiplied by the IMON ADC-sensed valued and forms the final IMON digital-sense value. The IMON digital-sense value is used for SVID and AVSBus output current reporting. The final IMON sensed value can be calculated with the following equation:  $IMON\_SNS\_FNL = 1023 \times \frac{I_{OUT} \times K_{CS} \times G_{IMON} \times R_{IMON}}{1.6} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where $I_{OUT}$ is the output current (in A), $K_{CS}$ is the Intelli-Phase™ current-sense gain (in A/A), $G_{IMON}$ is the IMON current mirror gain selected by register MFR_IMON_DGTL_ANA_GAIN_R1 (0Ch on page 2) bit[12:11], $R_{IMON}$ is the IMON resistor (in Ω), and IMON_DGTL_GAIN is a decimal value.

### MFR\_VR\_MULTI\_CONFIG\_R1 (0Dh)

This command on page 2 sets certain basic system configurations for rail 1.

Command	MFR_VR_MULTI_CONFIG_R1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Function	X	X					
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Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	IMVP9_EN	Enables IMVP9 VID table format. 1'b0: Disable IMVP9 VID table format 1'b1: Enable IMVP9 VID table format
12:5	VBOOT_SET	Sets the start-up voltage for rail 1 when VBOOT, set with register MFR_VR_CONFIG2 (50h on page 0) bit[12] = 0. It is in VID format. The VID resolution is selected by bit[4] in this command. 1 VID step/LSB.
4	VID_STEP_SEL	Selects the rail 1 VID resolution. 1'b0: 10mV per VID step 1'b1: 5mV per VID step
3:0	PHASE_CNT	Sets the full-phase count for rail 1. 4'b0000: 1-phase DCM 4'b0001: 1-phase CCM 4'b0010: 2-phase 4'b0011: 3-phase 4'b0100: 4-phase 4'b0101: 5-phase 4'b0110: 6-phase 4'b0111: 7-phase 4'b1000: 8-phase 4'b1001: 9-phase 4'b1010: 10-phase 4'b1011: 11-phase Others: 12-phase

### SVID\_VR\_CONFIG (0Eh)

This command on page 2 sets certain configurations related to Intel protocol.

Command	SVID_VR_CONFIG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	PSYS_SUP	Support bit for PSYS 2.0. 1'b0: Not supported 1'b1: Supported
14:11	PSYS_ADDR	Sets the SVID address for the PSYS rail.
10:5	PWR_IN_ALT_DLY	Sets PWR_IN_ALT# de-asserting blanking time. 3.375ms/LSB.
4, 1:0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3	HIGH_PREC_EN_PSYS	Enable bit for high-precision SVID telemetry format. It is only effective for the PSYSA rail. 1'b0: Disable high-precision SVID telemetry 1'b1: Enable high-precision SVID telemetry

2	HIGH_PREC_EN	Enable bit for high-precision telemetry format. It is effective for rail 1 and rail 2. 1'b0: Disable high-precision telemetry format on rail 1 and rail 2 1'b1: Enable high-precision telemetry format on rail 1 and rail 2
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### MFR\_IIN\_GAIN (0Fh)

This command on page 2 sets the input current-sense gain.

Command	MFR_IIN_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	GAIN_SEL				IIN_GAIN											

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:10	GAIN_SEL	Selects the parameter of IIN_GAIN calculation in the equation of bit[9:0] for this command.
9:0	IIN_GAIN	Sets the current-sense gain for the PMBus and SVID report.  Calculate the $I_{IN}$ sense gain with the following equation:  $IIN\_GAIN = \frac{K_{IN} \times R_{PSYS} \times 10230 \times 2^{GAIN\_SEL}}{1.6} \quad GAIN\_SEL < 6$  Where $K_{IN}$ is the e-fuse current-sense gain (in A/A), $R_{PSYS}$ is the resistor on PSYS pin (in $\Omega$ ), and GAIN_SEL is bit[12:10] in this command.

### MFR\_PIN\_MAX (10h)

This command on page 2 sets the maximum reported input power ( $P_{IN}$ ) of the SVID interface. It is used for input power report scaling in SVID command PWR\_IN (1Bh). The value in the command also sets the value return to SVID command Power In Max (2Eh), PwrInMax Register (51h), and the initial input power alert threshold.

Command	MFR_PIN_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:8	PIN_MAX_HC_ADD	Sets the additional maximum report input power for VR13.HC. The CPU total PIN MAX can be estimated with the following equation:  $PIN\_MAX\_HC(W) = PIN\_MAX \times 2 + PIN\_MAX\_HC\_ADD \times 4$ 4W/LSB.
7:0	PIN_MAX	Sets the VR13 and VR14 maximum reported input power of the SVID interface. Sets the 8LSB for the VR13.HC maximum report input current.  Resolution:  VR13 and VR13.HC: 2W/LSB(VR13) VR14: Determined by bit[12:10] of PMBus command MFR_ICCMAX_R1 (12h on page 2)

**MFR\_SLEW\_RATE\_SET\_R2 (11h)**

This command on page 2 sets the rail 2 VID fast and slow slew rate.

Command	MFR_SLEW_RATE_SET_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	SLEW_SLOW_SR	4'b1xxx: SLEW_SLOW_SR = FAST_SR/16 4'b01xx: SLEW_SLOW_SR = FAST_SR/8 4'b001x and 4'b0000: SLEW_SLOW_SR = FAST_SR/4 4'b0001: SLEW_SLOW_SR = FAST_SR/2 “x” means not applicable. Where FAST_SR is the VID fast slew rate defined in register bit[7:0] below.
7	AC_DC_DROOP_SEL	Selects DC or AC droop injection. 1'b0: DC droop injection 1'b1: AC droop injection
6	LPF_GAIN_SET	Sets the resistor for the droop compensation component. 1'b0: 0.83kΩ 1'b1: 1.66kΩ
5:0	SLEW_FAST_CNT	Sets the VID fast slew rate by setting the time interval of each VID step. It is in direct format. 50ns/LSB. The slew rate can be calculated with the following equation: $\text{FAST_SR(mV/μs)} = \frac{\text{VID\_STEP(mV)}}{\text{SLEW\_FAST\_CNT} \times 0.05(\mu\text{s})}$ Where VID_STEP is in 5mV or 10mV. It is determined by bit[3] of register MFR_VR_MULTI_CONFIG_R2 (1Dh on page 2).

**MFR\_ICC\_MAX\_R2 (12h)**

This command on page 2 sets the  $I_{CCMAX}$  value of rail 2. It also sets the VR14-specified high-current capability register.

Command	MFR_ICC_MAX_R2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ICCMAX															

Bits	Bit Name	Description	VR13.HC and earlier
		VR14	
15:13	A_PER_BIT_IN/ ICC_MAX_ADD [7:5]	<b>A_PER_BIT_IN</b> Corresponds to the VR14-specified high-current capability register (SVID register 50h), bit[7:5]. Sets the value in A/LSB step for the input current telemetry. 3'b000: 1A/LSB 3'b001: 2A/LSB 3'b010: 4A/LSB 3'b011: 0.5A/LSB 3'b100: 0.25A/LSB 3'b101: 0.125A/LSB 3'b110: 0.0625A/LSB 3'b111: 0.03125A/LSB	
12:10	W_PER_BIT_OUT/ ICC_MAX_ADD [4:2]	<b>W_PER_BIT_OUT</b> Corresponds to the VR14-specified high-current capability register (SVID register 50h), bit[4:2]. Sets the step input and output power telemetry. Applies to the output power telemetry (SVID register 18h). Output power: 3'b000: 1W/LSB 3'b001: 2W/LSB 3'b010: 4W/LSB 3'b011: 8W/LSB Others: Unsupported	<b>ICCMAX_ADD</b> Sets the VR13.HC SVID maximum report current 8HSB (ICCMAX_ADD). For VR13.HC, the maximum SVID reported current is: $\text{ICCMAX} = \text{ICCMAX} + \text{ICCMAX\_ADD} \times 2$ 2A/LSB.
9:8	A_PER_BIT_OUT/ ICC_MAX_ADD [1:0]	<b>A_PER_BIT_OUT</b> Corresponds to the VR14-specified high-current capability register (SVID register 50h), bit[1:0]. Set the value in 1A/LSB step for the ICC_MAX register (SVID reg 21h) 2'b00: 1A/LSB 2'b01: 2A/LSB 2'b10: 4A/LSB 2'b11: 8A/LSB	
7:0	ICCMAX	Sets the VR14 SVID maximum report current (FFh). The output will not start if ICCMAX is set to 0. The resolution is set by bit[9:8] in this command.	Sets the VR13 SVID maximum report current (FFh) and the VR13.HC SVID maximum report current 8LSB. The output will not start if ICCMAX is set to 0. 1A/LSB.

**SVID\_CAPABILITY\_DC\_LL\_R2 (13h)**

This command on page 2 sets the Intel-specified CAPABILITY and DC\_LL. It is only used for rail 2.

<b>Command</b>	SVID_CAPABILITY_DC_LL_R2															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	DC_LL								CAPABILITY							

Bits	Bit Name	Description
15:8	DC_LL	Data register containing the programmed load line or AVP of the platform based on the output capacitance and $R_{PATH}$ . If the PWM IC supports resistor LL or AVP programming, this register is not used. The master does not read this register. 0.1mΩ/LSB.
7:0	CAPABILITY	00h indicates that only required registers are supported. Bit[15] = 1, output current reported as a fraction of $I_{CCMAX}$ Bit[14] = 1, support temperature ADC (17h) Bit[13] = 1, support $V_{IN}$ ADC (1Bh) Bit[12] = 1, support $V_{IN}$ ADC (1Ah) Bit[11] = 1, support $I_{IN}$ ADC (19h) Bit[10] = 1, support $P_{OUT}$ ADC (18h) Bit[9] = 1, support $V_{OUT}$ ADC (16h) Bit[8] = 1, support $I_{OUT} / J_{OUT}$ ADC format for pre-VR13 CPU and output current ADC for VR13+ CPU (15h)

**SVID\_SR\_FAST\_SR\_SLOW\_R2 (14h)**

This command on page 2 sets the Intel-specified SR\_FAST and SR\_SLOW. It is only for rail 2.

<b>Command</b>	SVID_SR_FAST_SR_SLOW_R2															
<b>Format</b>	Binary															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>	SR_SLOW								SR_FAST							

Bits	Bit Name	Description
15:8	SR_SLOW	Data register containing the capability of rail 2's slow slew rate. 1(mV/μs)/LSB.
7:0	SR_FAST	Data register containing the capability of rail 2's fast slew rate. 1(mV/μs)/LSB.

**SVID\_PHSHD\_VR\_CONFIG (15h)**

This command on page 2 sets the Intel-specified EN2SVID\_RDY. It also has some bits to set phase-shedding method and enable negative edge response for both rails.

<b>Command</b>	SVID_PHSHD_VR_CONFIG															
<b>Format</b>	Direct															
<b>Bit</b>	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Access</b>	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
<b>Function</b>																

Bits	Bit Name	Description
15	PHSHED_MODE_R2	Sets the phase-shedding control mode. 1'b0: SVID mode. The phase-shedding method is set by SVID interface 1'b1: PMBus mode. The phase-shedding method is set by PHSCHED_ACT_R1, bit[14:13] in this command
14:13	PHSHED_ACT_R2	Sets the PMBus phase-shedding method. It is effective when PHSCHED_MODE_R2 = 1. It also sets the default value in register SVID PHSCHED_ACT (SVID register 50h). 2'b00: Automatic phase-shedding 2'b01: Manual phase-shedding 2'b10: Follow set PS command 2'b11: Not used
12	NEGVREN_MODE_R2	Sets the enable control's negative edge response mode (EN shutdown mode). 1'b0: SVID mode. The enable control's negative edge response is set by the SVID interface 1'b1: PMBus mode. The enable negative edge response is set by NEGVREN_ACT_R1, bit[11:10] in this command
11:10	NEGVREN_ACT_R2	Sets the EN shutdown slew rate. It is effective when NEGVREN_MODE_R2 = 1. It also sets the default value in register SVID NEGVREN_ACT (SVID 50h). 2'b00: Decay 2'b01: Slow slew rate 2'b10: Fast slew rate 2'b11: Slew rate defined by VOUT_TRANSITION_RATE (27h on page 1)
9	PHSHED_MODE_R1	Sets the phase-shedding control mode 1'b0: SVID mode. The phase-shedding method is set by the SVID interface 1'b1: PMBus mode. The phase-shedding method is set by PHSCHED_ACT_R1, bit[8:7] in this command
8:7	PHSHED_ACT_R1	Sets the PMBus phase-shedding method. It is effective when PHSCHED_MODE_R1 = 1. It also sets the default value in register SVID PHSCHED_ACT (SVID register 50h). 2'b00: Automatic phase-shedding 2'b01: Manual phase shedding 2'b10: Follow set PS command 2'b11: Not used
6	NEGVREN_MODE_R1	Sets the enable control's negative edge response mode (EN shutdown mode). 1'b0: SVID mode. The enable control's negative edge response is set by the SVID interface 1'b1: PMBus mode. The enable control's negative edge response is set by NEGVREN_ACT_R1, bit[5:4] in this command
5:4	NEGVREN_ACT_R1	Sets the EN shutdown slew rate. It is effective when NEGVREN_MODE_R1 = 1. it also sets the default value in register SVID NEGVREN_ACT (SVID register 50h). 2'b00: Decay 2'b01: Slow slew rate 2'b10: Fast slew rate 2'b11: Slew rate defined by VOUT_TRANSITION_RATE (27h on page 0)
3	VSYS_MODE	Sets the initial values for the SVID register multi-VR and PSYS configuration (34h) bit[2] for PSYS rail. 1'b0: PSYS mode. PSYS_CRIT# low indicates that PSYS has exceeded the critical threshold 1'b1: VSYS mode. PSYS_CRIT# low indicates that VSYS is below the critical threshold

2	VR_READY_0V_PSYS	Sets the initial value for SVID register multi-VR and PSYS configuration (34h) bit[0], which determines whether to assert VRRDY_PSYS or not when VID is set to 0 for the PSYS rail.  1'b0: VRRDY_PSYS de-asserts when SetVID = 0 1'b1: VRRDY_PSYS asserts when SetVID = 0  The MP297X does not provide external VRRDY_PSYS indication, so it should be set to 0 for normal operation
1	VR_READY_0V_R2	Sets the initial value for SVID register multi-VR and PSYS configuration (34h) bit[0], which determines whether to assert VRRDY2 when SetVID = 0 for rail 2.  1'b0: VRRDY2 de-asserts when SetVID = 0 1'b1: VRRDY2 asserts when SetVID = 0
0	VR_READY_0V_R1	Sets the initial value for SVID register multi-VR and PSYS configuration (34h) bit[0], which determines whether to assert VRRDY1 when SetVID = 0 for rail 1.  1'b0: VRRDY1 de-asserts when SetVID = 0 1'b1: VRRDY1 asserts when SetVID = 0

**MFR\_IDROOP\_CTRL1\_R2 (16h)**

This command on page 2 sets the configurations related to rail 2's droop.

Command	MFR_IDROOP_CTRL1_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:14	DROOP_TRIM_SET	2'b00: Select TRIM_IDROOP1 as the droop trim value 2'b 01: Select TRIM_IDROOP2 as the droop trim value 2'b 10: Select TRIM_IDROOP3 as the droop trim value 2'b 11: Select TRIM_IDROOP4 as the droop trim value
13	LPF2_EN	Enable bit for droop compensation component 2. 1'b0: Disable droop compensation component 2 1'b1: Enable droop compensation component 1
12	LPF1_EN	Enable bit for droop compensation component 1. 1'b0: Disable droop compensation component 1 1'b1: Enable droop compensation component 2
11	NON-LINEAR_AVF_EN	Enable bit for nonlinear AVF function. 1'b0: Disable nonlinear AVF 1'b1: Enable nonlinear AVF
10:9	RDROOP_SET	Sets the internal droop resistor value. 2'b00: 1000Ω 2'b01: 400Ω 2'b10: 235Ω 2'b11: Unconnected
8	AC_DROOP_BW_SEL	Selects the bandwidth of the AC droop regulation loop. It is only effective when bit[8] of register MFR_IDROOP_CTRL2_R2 (17h on page 2) = 1. 1'b0: 25kHz 1'b1: 50kHz

7:0	IDROOP_GAIN_SET	Sets the internal current mirror gain of ( $I_{DROOP} / I_{CS\_SUM}$ ), estimated with the following equation: $\frac{I_{DROOP}}{I_{CS\_SUM}} = \frac{IDROOP\_GAIN\_SET}{256}$ Where $I_{DROOP}$ is the current injected into the droop register to generate the droop voltage (in A), and $I_{CS\_SUM}$ is the total sensed current into the CS pin (in A).
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**MFR\_IDROOP\_CTRL2\_R2 (17h)**

This command on page 2 sets the configurations related to rail 2's droop.

Command	MFR_IDROOP_CTRL2_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								X								

Bits	Bit Name	Description
15:12	LPF2_FIL_SET	Sets the RC filter parameter for droop compensation component 1.  4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03μs 4'b0110: 1.23μs 4'b0111: 1.42μs 4'b1000: 2.87μs 4'b1001: 3.16μs 4'b1010: 3.47μs 4'b1011: 3.74μs 4'b1100: 4.14μs 4'b1101: 4.40μs 4'b1110: 4.72μs 4'b1111: 4.98μs
11:8	LPF1_FIL_SET	Sets the RC filter parameter for droop compensation component 2.  4'b0000: 5.8ns 4'b0001: 190ns 4'b0010: 396ns 4'b0011: 582ns 4'b0100: 846ns 4'b0101: 1.03μs 4'b0110: 1.23μs 4'b0111: 1.42μs 4'b1000: 2.87μs 4'b1001: 3.16μs 4'b1010: 3.47μs 4'b1011: 3.74μs 4'b1100: 4.14μs 4'b1101: 4.40μs 4'b1110: 4.72μs 4'b1111: 4.98μs

7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.																					
6:0	VOUT_TRIM	<p>Fine-tunes the output voltage. It is in two's complement format. The resolution is related to the VDIFF gain set by bit[11] of VOUT_SENSE_SET (29h on page 1).</p> <p>0.5mV/LSB with VDIFF unit gain 0.8mV/LSB with VDIFF half-gain</p> <p>The voltage table below shows the binary data and real-world values:</p> <table border="1"> <thead> <tr> <th>VOUT_TRIM</th> <th>VDIFF Unit Gain</th> <th>VDIFF Half-Gain</th> </tr> </thead> <tbody> <tr> <td>7'b 000 0000</td> <td>0</td> <td>0</td> </tr> <tr> <td>7'b 000 0001</td> <td>0.5mV</td> <td>0.8mV</td> </tr> <tr> <td>7'b 011 1111</td> <td>31.5mV</td> <td>50.4mV</td> </tr> <tr> <td>7'b 100 0000</td> <td>-32mV</td> <td>-51.2mV</td> </tr> <tr> <td>7'b 100 0001</td> <td>-31.5mV</td> <td>-50.4mV</td> </tr> <tr> <td>7'b 111 1111</td> <td>-0.5mV</td> <td>-0.8mV</td> </tr> </tbody> </table>	VOUT_TRIM	VDIFF Unit Gain	VDIFF Half-Gain	7'b 000 0000	0	0	7'b 000 0001	0.5mV	0.8mV	7'b 011 1111	31.5mV	50.4mV	7'b 100 0000	-32mV	-51.2mV	7'b 100 0001	-31.5mV	-50.4mV	7'b 111 1111	-0.5mV	-0.8mV
VOUT_TRIM	VDIFF Unit Gain	VDIFF Half-Gain																					
7'b 000 0000	0	0																					
7'b 000 0001	0.5mV	0.8mV																					
7'b 011 1111	31.5mV	50.4mV																					
7'b 100 0000	-32mV	-51.2mV																					
7'b 100 0001	-31.5mV	-50.4mV																					
7'b 111 1111	-0.5mV	-0.8mV																					

### IOUT\_RPT\_GAIN\_SVID\_AV\_S\_R2 (18h)

This command on page 2 sets rail 2's IOUT report gain for the SVID and AVSBus interface.

Command	IOUT_RPT_GAIN_SVID_AV_S_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	AVSBUS_GIMON_RES				IMON_GAIN									

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	AVSBUS_GIMON_RES	<p>Selects the current-sense resolution for the AVSBus interface IOUT report. It is only effective in AVSBus VID override mode. The resolution selection acts as an intermediate variable to improve the AVSBus IOUT report accuracy. The final AVSBus IOUT report is always in 0.1A/LSB.</p> <p>4'b0001: 20mA/LSB, the maximum AVSBus report current is 41A 4'b0010: 40mA/LSB, the maximum AVSBus report current is 82A 4'b0100: 80mA/LSB, the maximum AVSBus report current is 164A 4'b1000: 160mA/LSB, the maximum AVSBus report current is 328A 4'b0000: 320mA/LSB, the maximum AVSBus report current is 656A</p> <p>Others are invalid input.</p>
9:0	IMON_GAIN	<p>Sets the current-sense gain for the SVID IOUT and AVSBus IOUT reporting. In SVID override mode, calculate the IMON-sense gain with the following equation:</p> $\text{IMON_GAIN} = 639 \times I_{CCMAX} \times K_{CS} \times G_{IMON} \times R_{IMON}$ <p>Where <math>I_{CCMAX}</math> is the maximum current of the Intel CPU (in A), <math>K_{CS}</math> is the Intelli-Phase™ current sense gain (in A/A), <math>G_{IMON}</math> is the IMON current mirror gain selected by register MFR_IMON_DGTL_ANA_GAIN_R2 (1Ch on page 2) bit[12:11], and <math>R_{IMON}</math> is the internal IMON resistor (in <math>\Omega</math>).</p> <p>In AVSBus VID override mode, calculate the IMON-sense gain with the following equation:</p> $\text{IMON_GAIN} = \begin{cases} K_{CS} \times R_{IMON} \times G_{IMON} \times \frac{1023 \times 256}{1.6 \times 50} \times \text{AVSBUS_GIMON_RES} & \text{AVSBUS_GIMON_RES} > 0 \\ K_{CS} \times R_{IMON} \times G_{IMON} \times \frac{1023 \times 256}{1.6 \times 50} \times 16 & \text{AVSBUS_GIMON_RES} = 0 \end{cases}$ <p>Where <math>K_{CS}</math> is the Intelli-Phase™ current-sense gain (in A/A), <math>G_{IMON}</math> is the IMON current mirror gain selected by register MFR_IMON_DGTL_ANA_GAIN_R2 (1Ch on page 2) bit[12:11], <math>R_{IMON}</math> is the internal IMON resistor (in <math>\Omega</math>), and <math>AVSBUS_GIMON_RES</math> is the decimal value set with bit[13:10] in this command.</p>

**MFR\_IMON\_OFFSET\_R2 (19h)**

This command on page 2 sets the offset of rail 2's SVID output current telemetry.

Command	MFR_IMON_OFFSET_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IMON_OFFSET_SVID_AVIS	<p>Set the SVID and AVSBus output current report offset. The value is in two's complement format. Bit[8] is the sign bit.</p> <p>The current resolution at SVID override mode is (ICCMAX / 255) A/LSB.</p> <p>Where ICCMAX is the current value set with PMBus command MFR_ICCMAX (BDh).</p> <p>The current resolution in AVSBus override mode follows the setting in IOUT_RPT_GAIN_SVID_AVIS_R2 (18h on page 2), bit[13:10].</p>

**MFR\_PMBUS\_ADDR\_IIN\_OFFSET (1Ah)**

This command on page 2 sets PMBus slave address. It also provides 1 byte to set the input current offset for SVID/PMBus telemetry.

Command	MFR_PMBUS_ADDR_IIN_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															IIN_OFFSET

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:12	ADDR_PMBUS_3MSB	Sets the 3MSB of the PMBus address.
11:8	ADDR_PMBUS_4LSB	<p>Sets the 4LSB of the PMBus address.</p> <p>When bit[11] of register MFR_VR_CONFIG5 (C6h on page 1) = 1, the PMBus address 4LSB is set by the ADDR_PL pin. ADDR_PMBUS_4LSB returns the 4LSB.</p> <p>When bit[11] of register MFR_VR_CONFIG5 (C6h on page 1) = 0, the 4LSB of PMBus address is set by ADDR_PMBUS_4LSB.</p>
7:0	IIN_OFFSET	Sets the input current offset added on IIN SVID telemetry (19h). It is in two's complement format. Bit[7] is the sign bit. 0.5A/LSB.

**IOUT\_CAL\_GAIN\_PMBUS\_R2 (1Bh)**

This command on page 2 sets the gain for rail 2 output current PMBus reporting. The reported output current is returned with PMBus command READ\_IOUT (8Ch on page 1).

Command	IOUT_CAL_GAIN_PMBUS_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X													IOUT_CAL_GAIN_PMBUS

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:11	GAIN_SEL	Sets the exponent value for the IOUT_CAL_GAIN_PMBUS calculation equation in this command.
10:0	IOUT_CAL_GAIN_PMBUS	Sets the current-sense gain for the PMBus report. The sense gain can be calculated with the following equation:  $IOUT\_CAL\_GAIN\_PMBUS = \frac{512}{1.6} \times K_{CS} \times G_{IMON} \times R_{IMON} \times 2^{(10-GAIN\_SEL)}$ Where $K_{CS}$ is the Intelli-Phase™ current-sense gain (in A/A), $G_{IMON}$ is the IMON current mirror gain, $R_{IMON}$ is the internal IMON resistor (in Ω), and GAIN_SEL is bit[12:11] in this command.

### MFR\_IMON\_DGTL\_ANA\_GAIN\_R2 (1Ch)

This command on page 2 sets the rail 2 IMON current mirror gain and internal IMON resistor value. It also sets the digital calculation gain for rail 2 IOUT reporting.

Command	MFR_IMON_DGTL_ANA_GAIN_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IMON_RES_SET IMON_DGTL_GAIN															

Bits	Bit Name	Description
15:13	IMON_RES_SET	Sets the internal resistor value for IMON. 3'b100: 2.5kΩ 3'b101: 5kΩ 3'b110: 10kΩ 3'b111: 40kΩ Others: Unconnected
12:11	IMON_GAIN_SET	Sets the current mirror gain from the total CS current to $I_{MON}$ . 2'b00: 2/64 2'b01: 3/64 2'b10: 5/64 2'b11: 8/64
10:0	IMON_DGTL_GAIN	Sets the digital calculation gain for IOUT reporting. The gain is multiplied by the IMON ADC-sensed value to form the final IMON digital-sense value. The IMON digital-sense value is used for SVID and AVSBus output current reporting. The final IMON-sensed value can be estimated with the following equation:  $IMON\_SNS\_FNL = 1023 \times \frac{I_{OUT} \times K_{CS} \times G_{IMON} \times R_{IMON}}{1.6} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where $I_{OUT}$ is the output current (in A), $K_{CS}$ is the Intelli-Phase™ current-sense gain (in A/A), $G_{IMON}$ is the IMON current mirror gain, $R_{IMON}$ is the IMON resistor (in Ω), and IMON_DGTL_GAIN is the decimal value.

### MFR\_VR\_MULTI\_CONFIG\_R2 (1Dh)

This command on page 2 sets basic system configurations for rail 2. It also provides certain bits to set the DDR-related options when the MP297x is used for memory power supply.

Command	MFR_VR_MULTI_CONFIG_R2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Access	R/W															
Function	x															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	R2_HALF_TRK_EN	Enable bit for rail 2 VOUT to track half of rail 1 VOUT. 1'b0: Rail 2's VOUT is independent from rail 1 1'b1: Rail 2's VOUT is half of rail 1 VOUT
13	REJ_SVID_ADDR2	Sets rail 2 to reject any SVID command from the CPU. 1'b0: Rail 2 will react to the SVID command it receives 1'b1: Rail 2 will reject any SVID command from the CPU
12	IMVP9_EN	Enables IMVP9 VID table format. 1'b0: Disable IMVP9 VID table format 1'b1: Enable IMVP9 VID table format
11:4	VBOOT_SET	Sets the start-up voltage for rail 1 when VBOOT is set via register MFR_VR_CONFIG2 (50h on page 1), bit[12] = 0. It is in VID format. The VID resolution is selected by bit[4] in this command. 1 VID step/LSB.
3	VID_STEP_SEL	Selects the rail 2 VID resolution. 1'b0: 10mV per VID step 1'b1: 5mV per VID step
2:0	PHASE_CNT	Sets full-phase count for rail 2. 3'b000: Off 3'b001: 1-phase CCM 3'b010: 2-phase 3'b011: 3-phase 3'b100: 4-phase 3'b101: 5-phase 3'b11x: 6-phase

### VOUT\_OFFSET (1Eh)

This command on page 2 instructs the device to add an offset over the VID from the SVID, AVSBus, or PMBus interface, and affects the final reference voltage. The data is in direct format. It is also referred to as overclocking tracking mode.

Command	VOUT_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	VOUT_OFFSET_R2								VOUT_OFFSET_R1							

Bits	Bit Name	Description
15:8	VOUT_OFFSET_R2	Adds an offset over the VID from the SVID, AVSBus, or PMBus interface, and affects the final reference voltage of rail 2. 1 VID step/LSB. This value is in two's complement format. Bit[7] is the sign bit.  The list below shows the binary data and real-world values: 8'b 0000 0000: 0 8'b 0000 0001: +1 VID step 8'b 0111 1111: +127 VID steps 8'b 1000 0000: -128 VID steps 8'b 1000 0001: -127 VID steps 8'b 1111 1111: -1 VID step

7:0	VOUT_OFFSET_R1	Adds an offset over the VID from the SVID, AVSBus, or PMBus interface, and affects the final reference voltage of rail 1. 1 VID step/LSB.
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**STORE\_NORMAL\_CODE (F1h)**

This command on page 2 instructs the PMBus to copy the page 2 contents to their matching locations in the MTP. During the copying process, the device calculates a CRC code for all the saved bits in the MTP. The CRC code checks whether the data is valid at the next start-up or restore.

This command is write-only. There is no data byte for this command.

**RESTORE\_NORMAL\_CODE (F2h)**

This command on page 2 instructs the PMBus device to copy the page 2 contents from the MTP and overwrite their matching locations in the operating memory. During this process, the device calculates CRC value for all restored bits. If the calculated CRC does not match the CRC value saved in the MTP, the device reports a CRC error via bit[4] of register STATUS\_CML (7Eh).

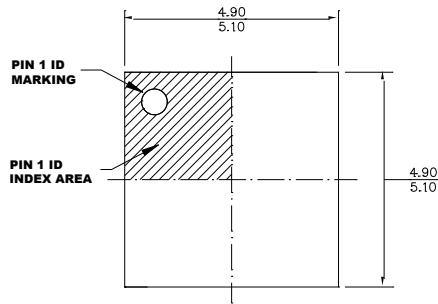
**STORE\_MULTI\_CODE (F3h)**

This command on page 2 instructs the PMBus to start writing the MTP multi-configuration zone. After this command, the user can change to page 2A and write multi-configuration register values to the MTP.

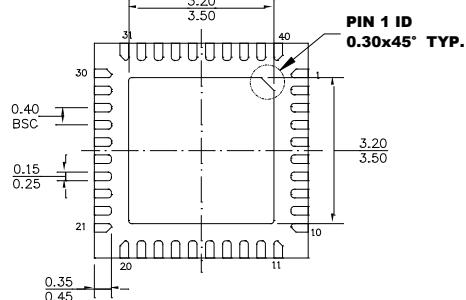
This command is write-only. There is no data byte for this command.

## PACKAGE INFORMATION

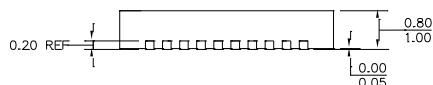
**QFN-40 (5mmx5mm)**



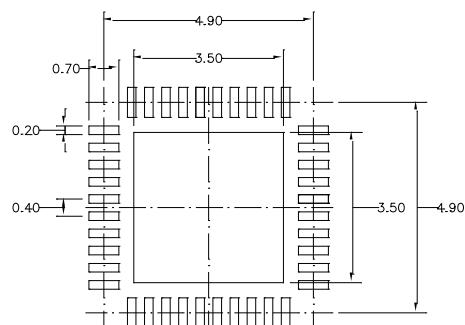
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

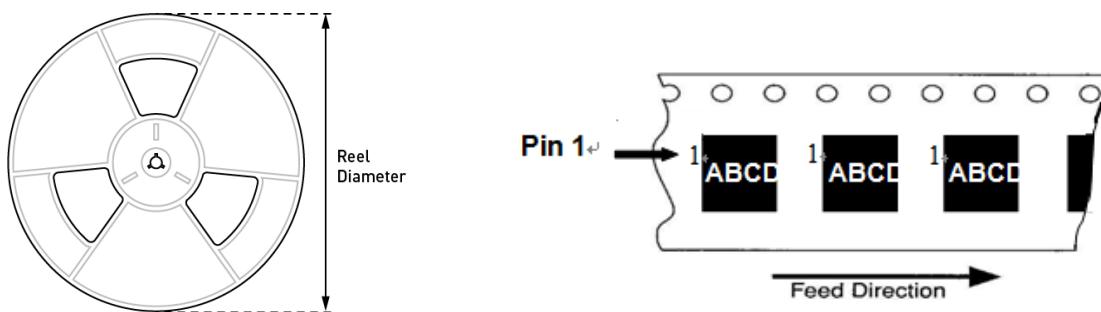


**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHE-1
- 5) DRAWING IS NOT TO SCALE.

**RECOMMENDED LAND PATTERN**

## CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2975GU-xxxx-Z	QFN (5mmx5mm)	5000	N/A	13in	12mm	8mm

## Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	2/28/2020	Initial Release	-
1.02	10/15/2020	Add 3Ch.p0	P59
		Add BFh.p0	P96
		Add B7h.p0	P96
		Add B2h.p1	P167
		Delete 28h.p0/1/D1h.p0/1 from DS	P55,P117
		Delete D1h.p0/1 from DS	P100,P176

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