Chiplet Placement for 2.5D IC with Sequence Pair Based Tree and Thermal Consideration

Hong-Wen Chiou, Jia-Hao Jiang, Yu-Teng Chang, Yu-Min Lee, Chi-Wen Pan

National Yang Ming Chiao Tung University, Hsinchu, Taiwan

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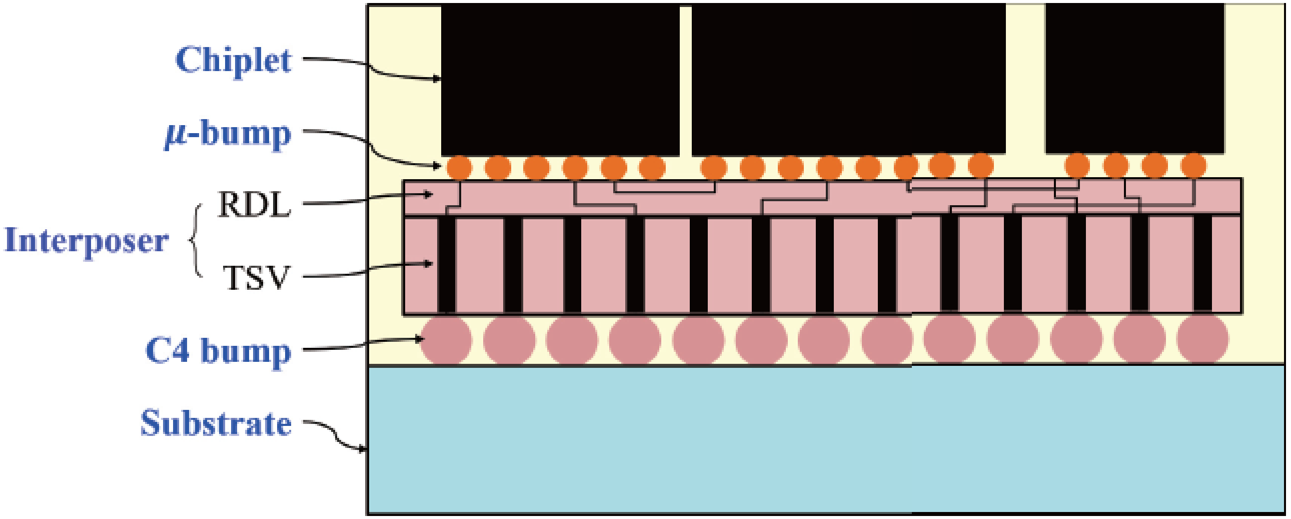
- Chiplet placement with SP-based tree
- Post Chiplet placement (post-cp) with thermal consideration
- Experimental results

Abstract

- This work develops an efficient chiplet placer with thermal consideration for 2.5D ICs
- Combine the way of **sequence-pair based tree**, **branchand-bound method**, and **advanced placement/pruning techniques** to find the optimal TWL solution on HPWL fastly
- With the post placement procedure, the placer reduces maximum temperatures with slight increase of wirelength
- Can reduce 1.035% HPWL, and the placer can speed up at most 2 orders
- Can reduce maximum temperature up to 8.214℃ with 5.376% increase of TWL on average

Introduction

2.5D ICs (or called interposer-based 3D IC) can provide better performance and yield than 2D ICs



Introduction

- Develop an efficient chiplet placer : **SP-CP** (Sequence-pair Chiplet placer)
- Build the **sequence pair based tree** (SP-Tree), which contains the rotation and partial/complete SP representation.
- Apply **B&B method** to get the optimal solution.
- Apply **advance placement/pruning techniques** for faster runtime
- Apply **post placement procedure** to reduce the operating temperatures but increase TWL slightly

Preliminary

1. Parallel B&B method for the chiplet placement

To considers the interconnect of chiplets and constructs a complete graph, the weight is calculate by:

$$w(i,j) = n(i,j) \times [w(i) + h(i) + w(j) + h(j)]/2$$

- n(i, j) : the # of nets between c(i) and c(j)
- w(i) : the width of c(i)
- h(i) : the height of c(i)
- w(j) : the width of c(j)
- h(j) : the height of c(j)

Preliminary

1. Parallel B&B method for the chiplet placement

這篇paper使用OpenMP來對B&B algorithm進行平行處理，並且每當更新best TWL，他們就會暫停其他thread來更新值以確保效率。

Consist of 2 parts:

(a) **branching part**

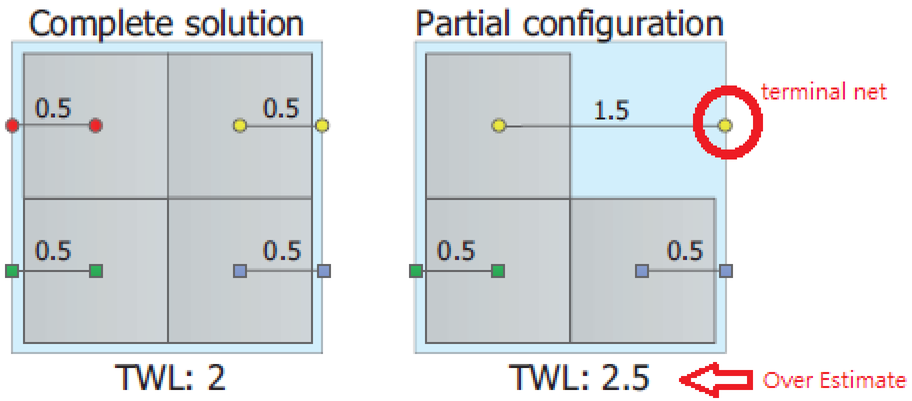
Apply DFS to traverse the SP-Tree, and add a chiplet at a time. The paper will generate 4 new nodes for the partial SP node and ${n_k}^2$new nodes for the rotational nodes.

(b) **bounding(pruning) part**

we prune the nodes which do not meet placement constraints, the nodes with estimated HPWL larger than the current best TWL, and the nodes which do not satisfy the A1 algorithm.

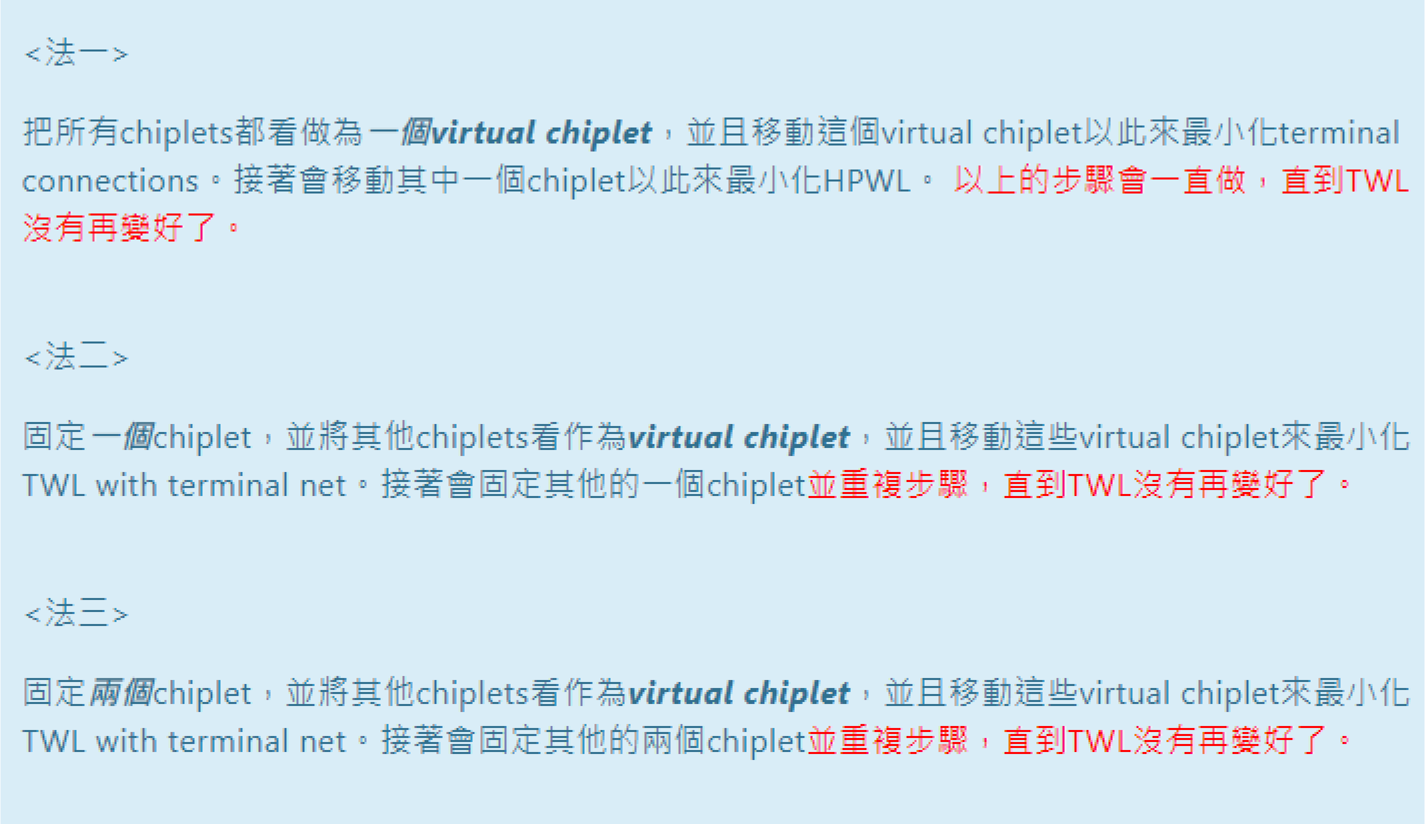
Preliminary

2. Placement optimization with whitespace



Preliminary

2. Placement optimization with whitespace



<法一>

把所有chiplets都看做為***一個virtual chiplet***，並且移動這個virtual chiplet以此來最小化terminal connections。接著會移動其中一個chiplet以此來最小化HPWL。 以上的步驟會一直做，直到TWL沒有再變好了。

<法二>

固定***一個***chiplet，並將其他chiplets看作為***virtual chiplet***，並且移動這些virtual chiplet來最小化TWL with terminal net。接著會固定其他的一個chiplet並重複步驟，直到TWL沒有再變好了。

<法三>

固定***兩個***chiplet，並將其他chiplets看作為***virtual chiplet***，並且移動這些virtual chiplet來最小化TWL with terminal net。接著會固定其他的兩個chiplet並重複步驟，直到TWL沒有再變好了。

Preliminary

3. Terminal Handling (TH)

- Minimal HPWL between die and related terminals
- When a chiplet is added to a partial placement, we looks forward to predicting WL augmentation from its terminal nets (use the way of “placement optimization of whhitespace”)
- Total 4 TH values because of the rotation

Preliminary

4. Forward Wirelength Checking (FC)

- minimal HPWL between two dies
- calculates the minimum WL for each chiplet pair with the nets only connected between them (use the way of “placement optimization of whitespace”)
- total 64 TH values because of the rotation + topology

Preliminary

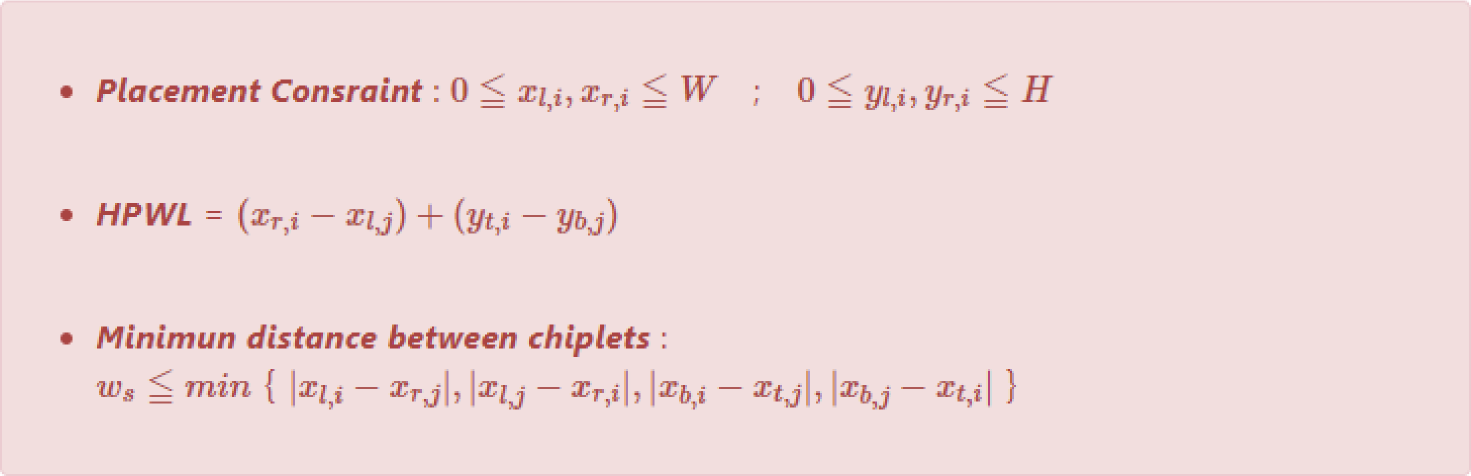
5. Sequence-pair Representation Methods

- (… i … j … , … i … j …) → C(i) is on the left side of C(j)
- (… j … i … , … j … i …) → C(i) is on the right side of C(j)
- (… i … j … , … j … i …) → C(i) is under of C(j)
- (… j … i … , … i … j …) → C(i) is above of C(j)

Problem formulation

1. Optimize HPWL

$$min \sum_{num\ of\ nets}^{k} HPWL_k$$



- ***Placement Consraint*** : $0 \leqq x_{l,i}, x_{r,i} \leqq W \quad ; \quad 0 \leqq y_{l,i}, y_{r,i} \leqq H$
- ***HPWL*** = $(x_{r,i} - x_{l,j}) + (y_{t,i} - y_{b,j})$
- ***Minimun distance between chiplets*** :
  $w_s \leqq min\ \{\ |x_{l,i} - x_{r,j}|, |x_{l,j} - x_{r,i}|, |x_{b,i} - x_{t,j}|, |x_{b,j} - x_{t,i}|\ \}$

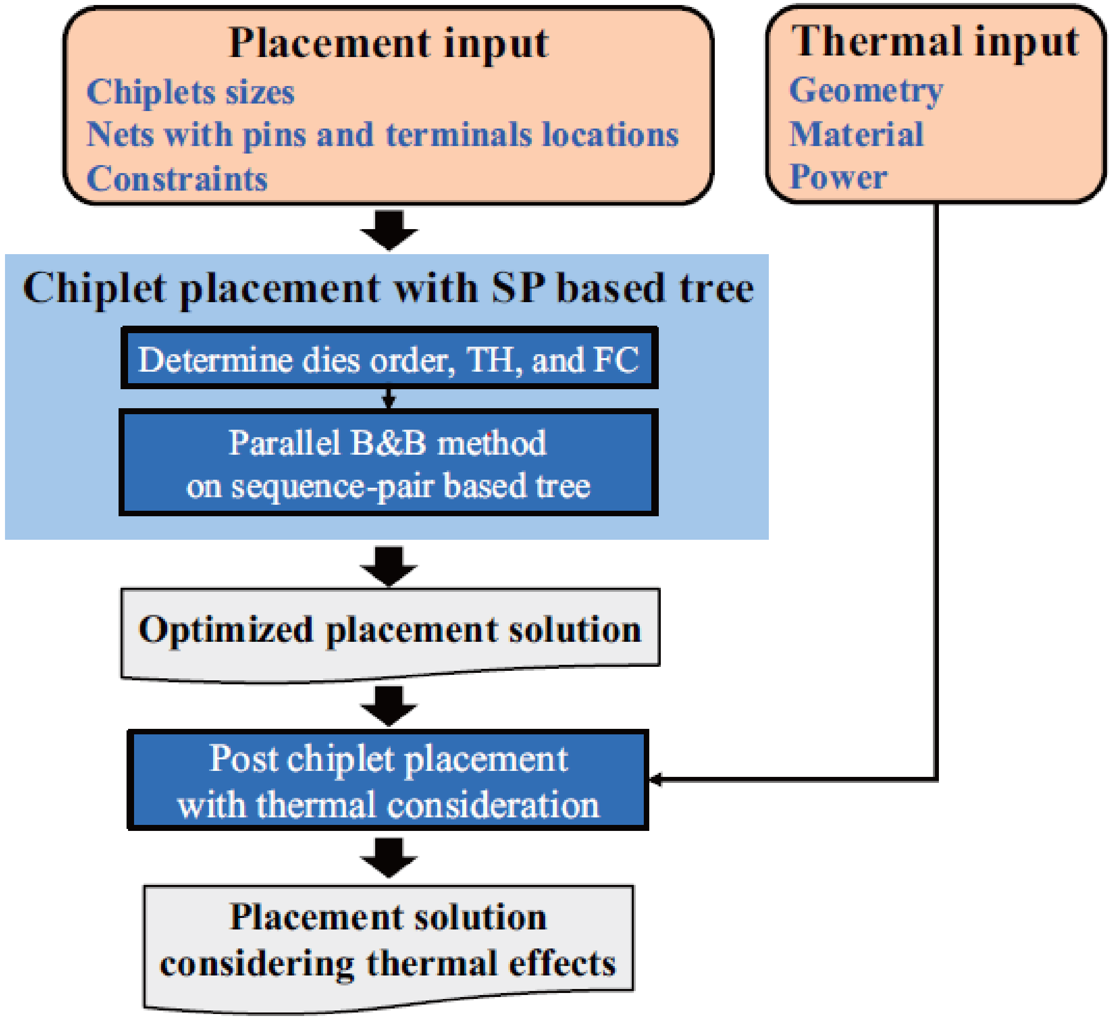
Problem formulation

2. Optimize maximum temperature

- We have found the optimal HPWL (TWL_{opt}), and this step we the goal is to satisfy the thermal constraint T_{cstr} ， and satisfy the constraint of $\frac{TWL_{mod}}{TWL_{OPT}} < \eta\%$

$$cost = \phi \times \frac{\mathrm{TWL} - \mathrm{TWL}^{opt}}{\mathrm{TWL}^{max} - \mathrm{TWL}^{opt}} + (1 - \phi) \times \frac{T_{max} - T_{max}^{min}}{T_{max}^{max} - T_{max}^{min}}$$

Chiplet placement with SP-based tree



Placement input
Chiplets sizes
Nets with pins and terminals locations
Constraints

Thermal input
Geometry
Material
Power

Chiplet placement with SP based tree
Determine dies order, TH, and FC
Parallel B&B method on sequence-pair based tree

Optimized placement solution

Post chiplet placement with thermal consideration

Placement solution considering thermal effects

Chiplet placement with SP-based tree

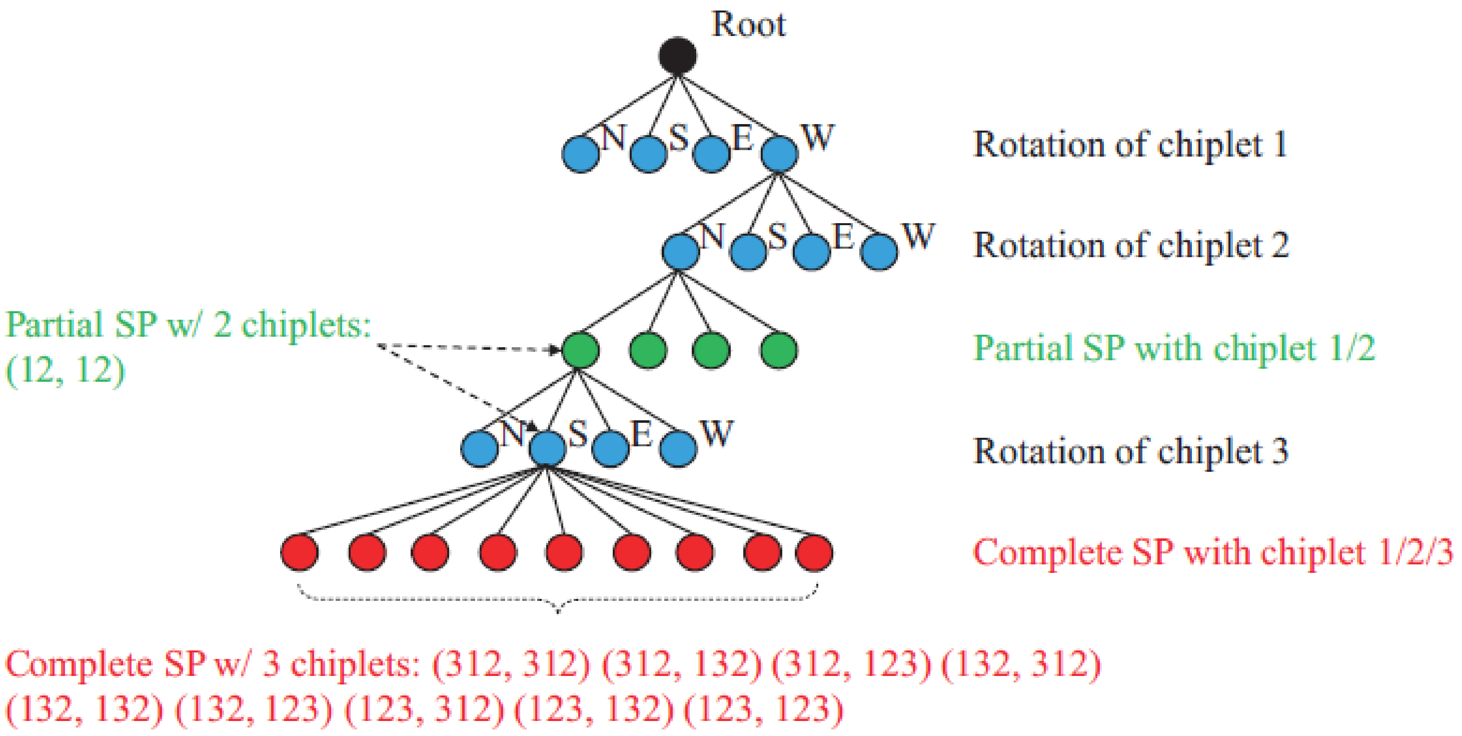
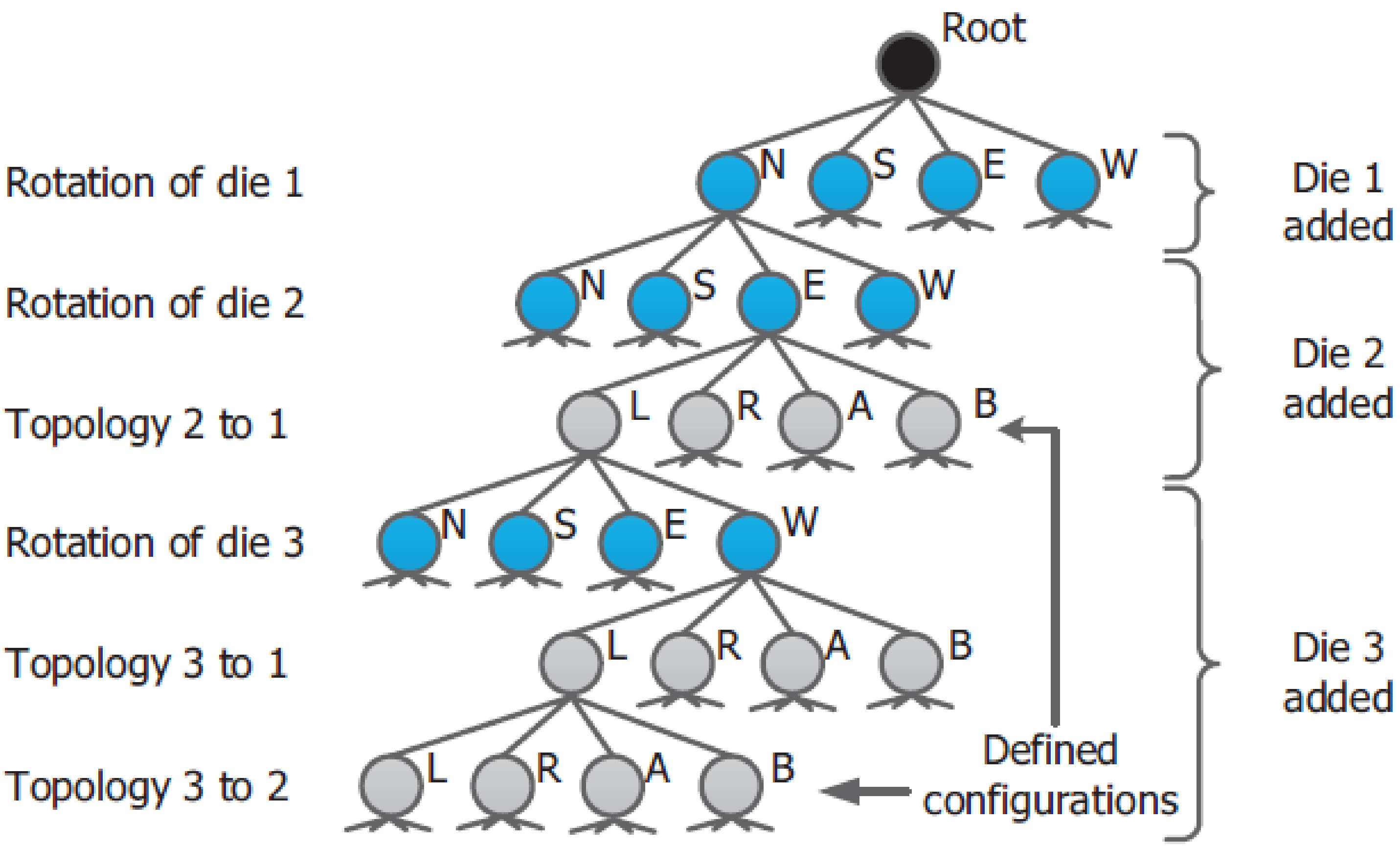

Root
N
S
E
W
Rotation of chiplet 1
N
S
E
W
Rotation of chiplet 2
Partial SP w/ 2 chiplets:
(12, 12)
Partial SP with chiplet 1/2
N
S
E
W
Rotation of chiplet 3
Complete SP with chiplet 1/2/3
Complete SP w/ 3 chiplets: (312, 312) (312, 132) (312, 123) (132, 312)
(132, 132) (132, 123) (123, 312) (123, 132) (123, 123)

Figure 3: Sequence pair based tree.

Chiplet placement with SP-based tree



Chiplet placement with SP-based tree

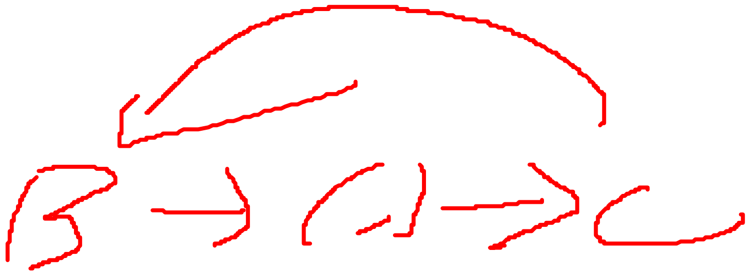
1. Some of topology nodes in CSP-Tree might not be packed into a placement.

E.g.

(a) chiplet B (cB) is at the left of chiplet A (cA)

(b) chiplet C (cC) is at the right of chiplet A (cA)

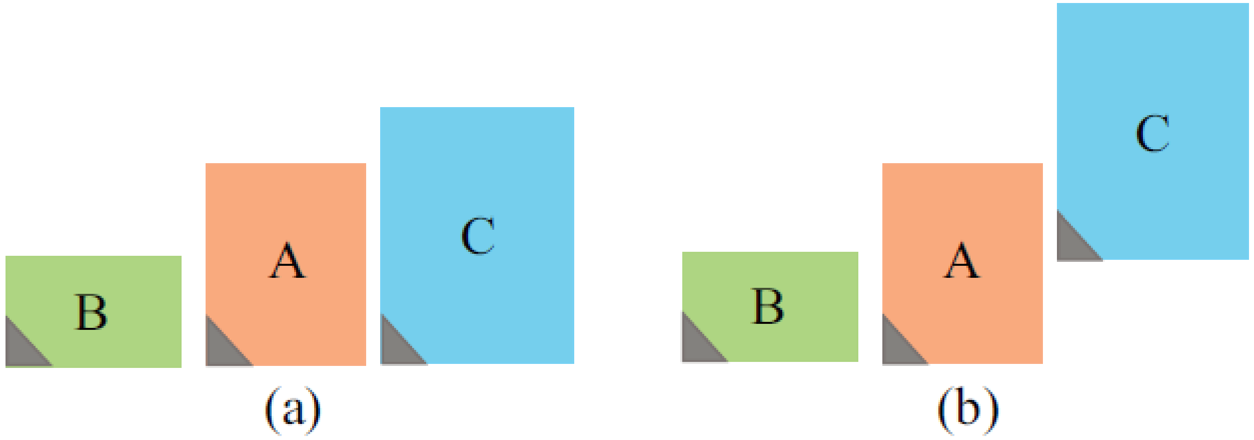
(c) chiplet C (Cc) is at the left of chiplet B (cB)



-> form a cyclic horizontal constraint graph

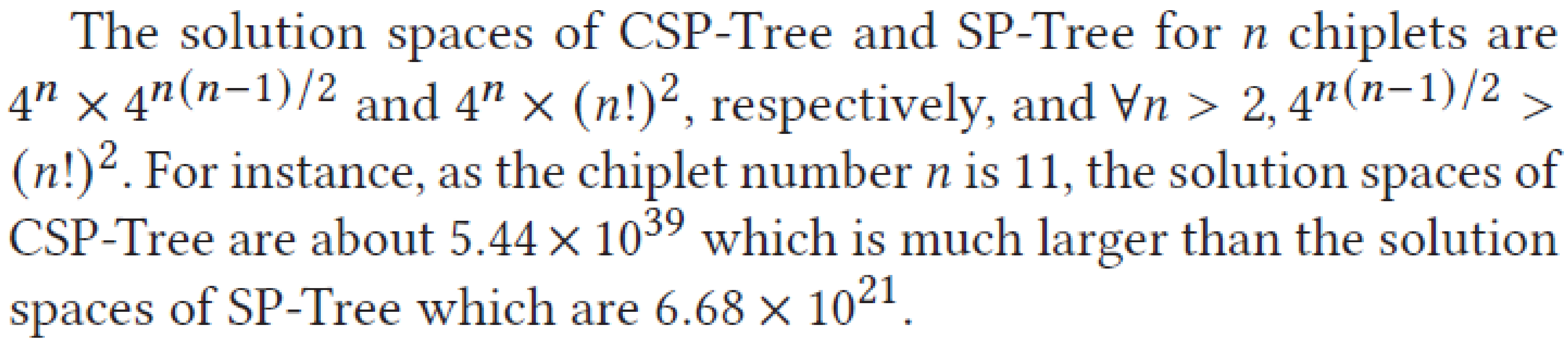
Chiplet placement with SP-based tree

2. one SP representation might cover multiple topology nodes in CSP-Tree

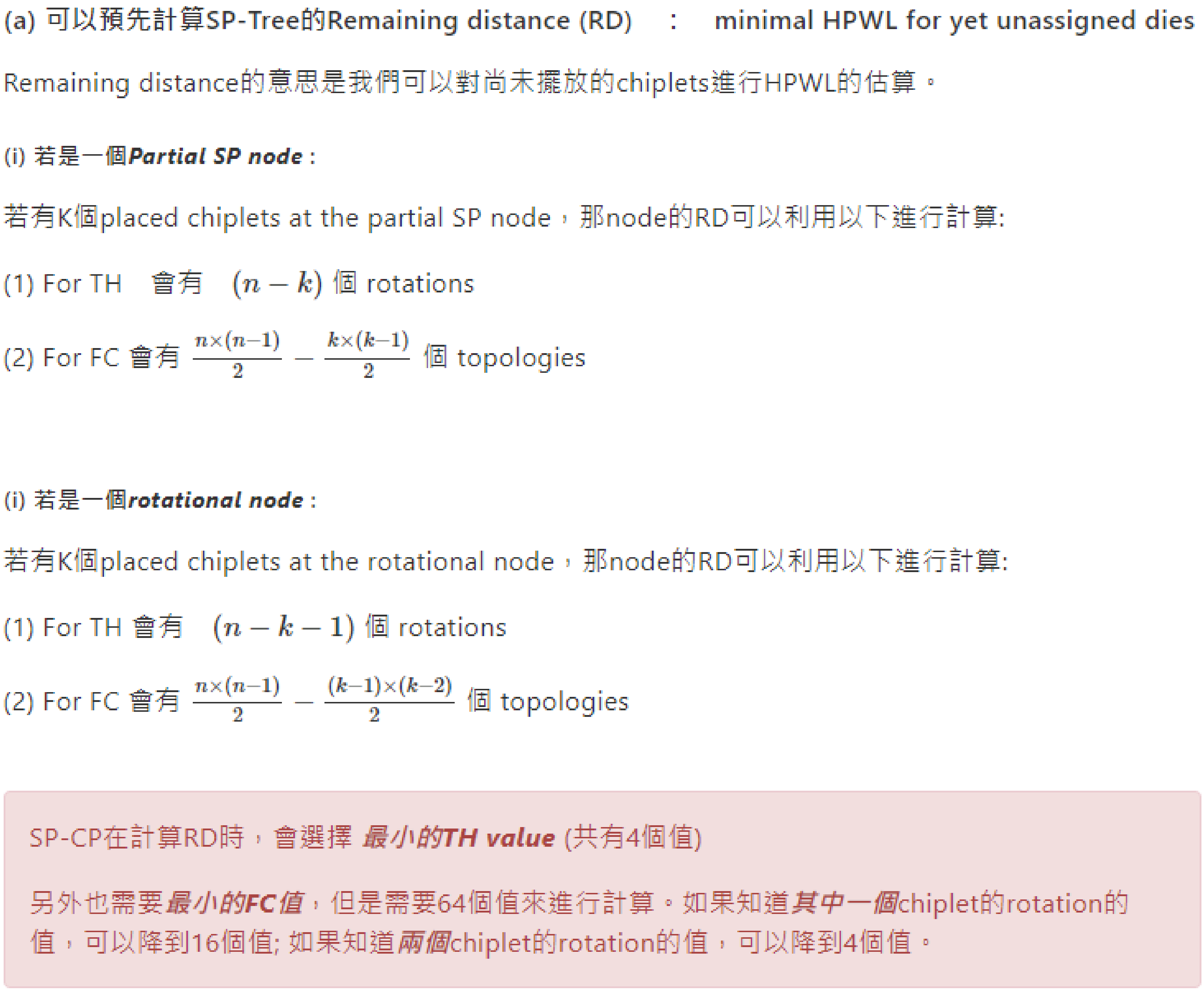


Chiplet placement with SP-based tree

3. CSP-Tree has higher complexity



The solution spaces of CSP-Tree and SP-Tree for n chiplets are $4^n \times 4^{n(n-1)/2}$ and $4^n \times (n!)^2$, respectively, and $\forall n > 2, 4^{n(n-1)/2} > (n!)^2$. For instance, as the chiplet number n is 11, the solution spaces of CSP-Tree are about 5.44×10^{39} which is much larger than the solution spaces of SP-Tree which are 6.68×10^{21}.



(a) 可以預先計算SP-Tree的Remaining distance (RD)　:　minimal HPWL for yet unassigned dies

Remaining distance的意思是我們可以對尚未擺放的chiplets進行HPWL的估算。

(i) 若是一個***Partial SP node*** :

若有K個placed chiplets at the partial SP node，那node的RD可以利用以下進行計算:

(1) For TH　會有　$(n-k)$ 個 rotations

(2) For FC 會有 $\frac{n\times(n-1)}{2}-\frac{k\times(k-1)}{2}$ 個 topologies

(i) 若是一個***rotational node*** :

若有K個placed chiplets at the rotational node，那node的RD可以利用以下進行計算:

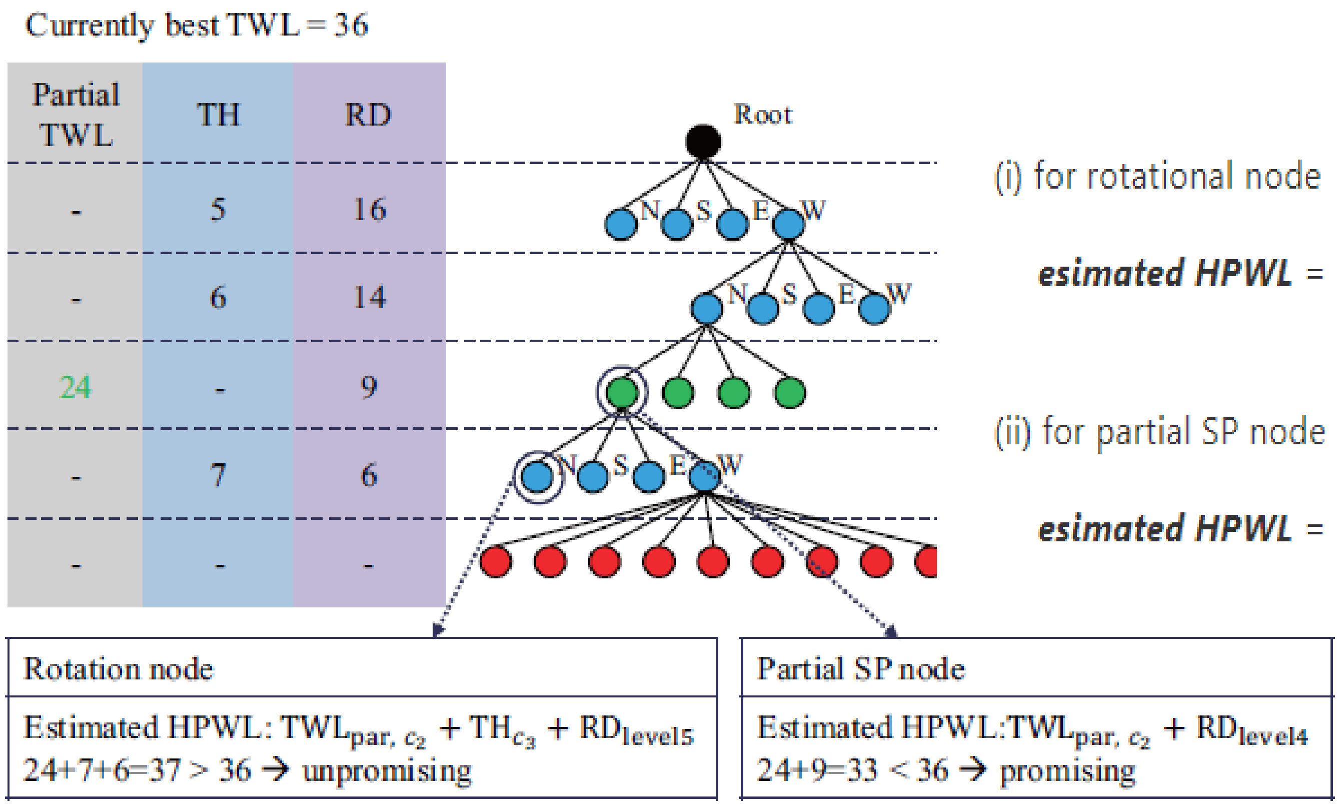
(1) For TH 會有　$(n-k-1)$ 個 rotations

(2) For FC 會有 $\frac{n\times(n-1)}{2}-\frac{(k-1)\times(k-2)}{2}$ 個 topologies

SP-CP在計算RD時，會選擇 ***最小的TH value*** (共有4個值)

另外也需要***最小的FC值***，但是需要64個值來進行計算。如果知道***其中一個***chiplet的rotation的值，可以降到16個值; 如果知道***兩個***chiplet的rotation的值，可以降到4個值。

Advanced placement/pruning techniques



Currently best TWL = 36

Partial TWL	TH	RD
-	5	16
-	6	14
24	-	9
-	7	6
-	-	-

Rotation node

Estimated HPWL: $TWL_{par,\,c_2} + TH_{c_3} + RD_{level5}$
24+7+6=37 > 36 → unpromising

Partial SP node

Estimated HPWL:$TWL_{par,\,c_2} + RD_{level4}$
24+9=33 < 36 → promising

(i) for rotational node

esimated HPWL = $TWL_{par,c2}$ + 現在node的TH + RD (the minimun value of c2 and c3)

(ii) for partial SP node

esimated HPWL = $TWL_{par,c2}$ + RD (the minimun value of c3)

Advanced placement/pruning techniques

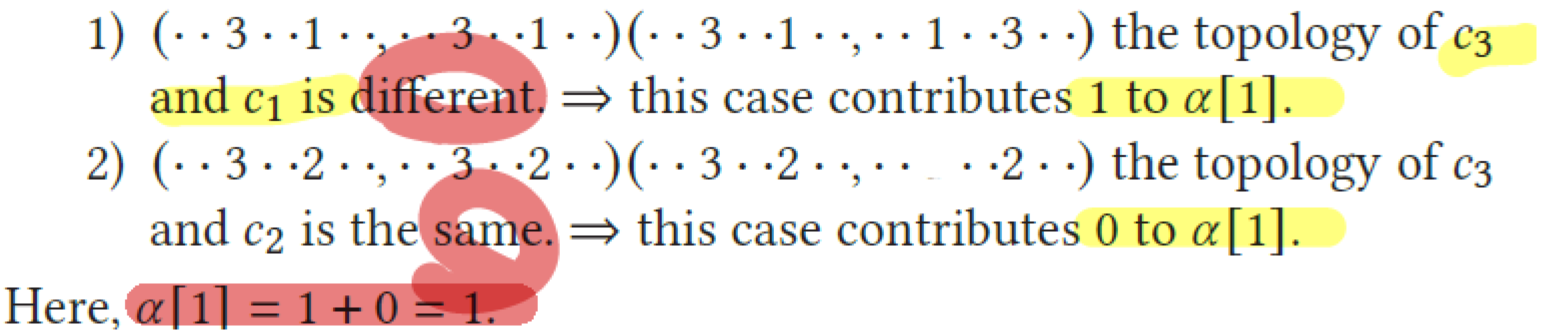
- **PDSP** : when the estimated HPWL is larger than bestTWL，then will prune the amount of $\frac{\text{bestTWL}}{n_k+1}$ nodes

- **PDSP&A1** : while a partial SP node in SP-Tree represents multiple topology relationships, the paper will prune the amount of γ[i] $\times$ $\frac{\text{bestTWL}}{n_k+1}$ topology nodes

Advanced placement/pruning techniques

E.g.

We inserting C3 into partial SP (12, 12), and we assume (312, 312) have the minimum estimated HPWL at the same level. we compare the topology of C3 with C1, and the topology of C3with C2:

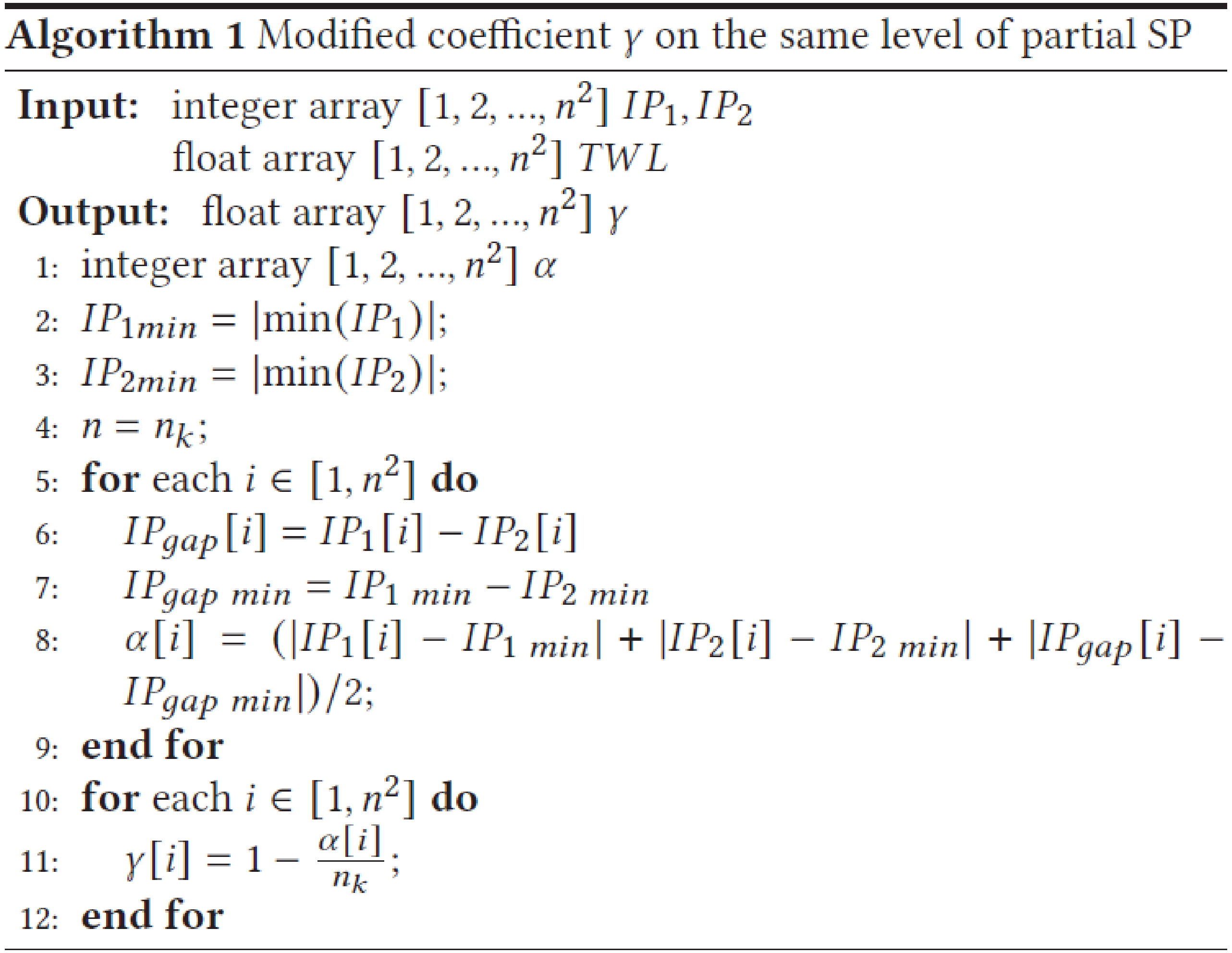


1) $(\cdot\cdot 3 \cdot\cdot 1 \cdot\cdot, \cdot\cdot 3 \cdot\cdot 1 \cdot\cdot)(\cdot\cdot 3 \cdot\cdot 1 \cdot\cdot, \cdot\cdot 1 \cdot\cdot 3 \cdot\cdot)$ the topology of c_3 and c_1 is different. ⇒ this case contributes 1 to $\alpha[1]$.

2) $(\cdot\cdot 3 \cdot\cdot 2 \cdot\cdot, \cdot\cdot 3 \cdot\cdot 2 \cdot\cdot)(\cdot\cdot 3 \cdot\cdot 2 \cdot\cdot, \cdot\cdot \quad \cdot\cdot 2 \cdot\cdot)$ the topology of c_3 and c_2 is the same. ⇒ this case contributes 0 to $\alpha[1]$.

Here, $\alpha[1] = 1 + 0 = 1$.

Advanced placement/pruning techniques



Algorithm 1 Modified coefficient γ on the same level of partial SP

```
Input:  integer array $[1, 2, ..., n^2]$ $IP_1, IP_2$
        float array $[1, 2, ..., n^2]$ $TWL$
Output: float array $[1, 2, ..., n^2]$ $\gamma$
integer array $[1, 2, ..., n^2]$ $\alpha$
$IP_{1min} = |\min(IP_1)|$;
$IP_{2min} = |\min(IP_2)|$;
$n = n_k$;
for each $i \in [1, n^2]$ do
    $IP_{gap}[i] = IP_1[i] - IP_2[i]$
    $IP_{gap\ min} = IP_{1\ min} - IP_{2\ min}$
    $\alpha[i] = (|IP_1[i] - IP_{1\ min}| + |IP_2[i] - IP_{2\ min}| + |IP_{gap}[i] - IP_{gap\ min}|)/2$;
end for
for each $i \in [1, n^2]$ do
    $\gamma[i] = 1 - \frac{\alpha[i]}{n_k}$;
end for
```

Post Chiplet placement (post-cp) with thermal consideration

1. Chip thermal simulation:

$$GT = P$$

G : thermal conductance matrix

T : thermal vector

P : power source vector

Post Chiplet placement (post-cp) with thermal consideration

To model a 2.5D IC, 5 layers should be included:

(a) The mesh size is 64×64×5

(b) The heat transfer coefficient for top/bottom side of the 2.5D IC is 8700/2017 W/m^2K

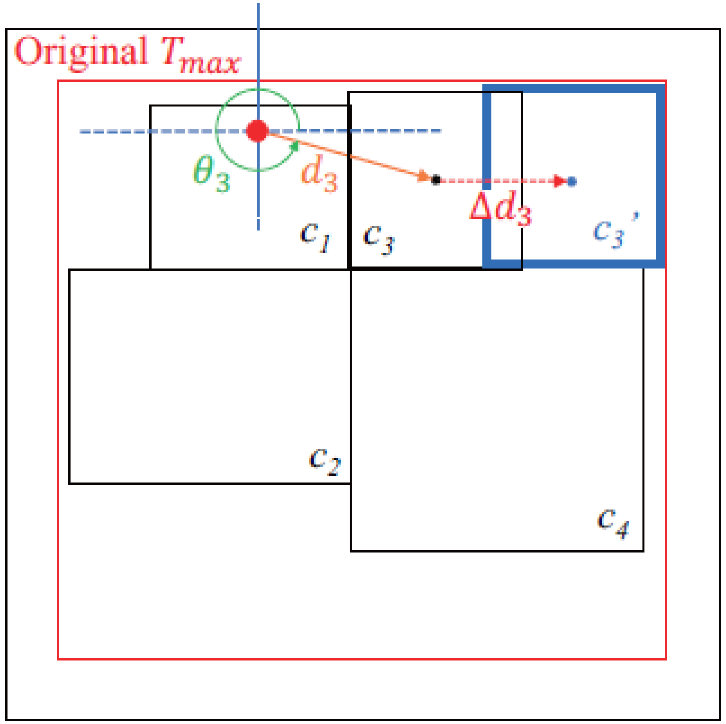
(c) It is adiabatic for the literal sides of 2.5D IC

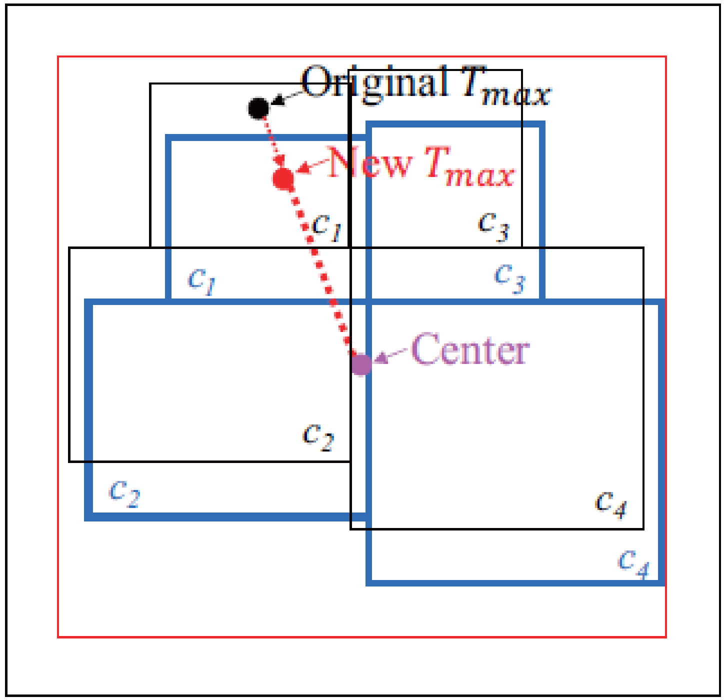
(d) Above condition model the primary heat flow to heat sink and secondary heat flow to PCB

(e) Solve T with the sparse matrix solver, SuperLU 5.3.0

Post Chiplet placement (post-cp) with thermal consideration

2. Placement refinement with thermal effects

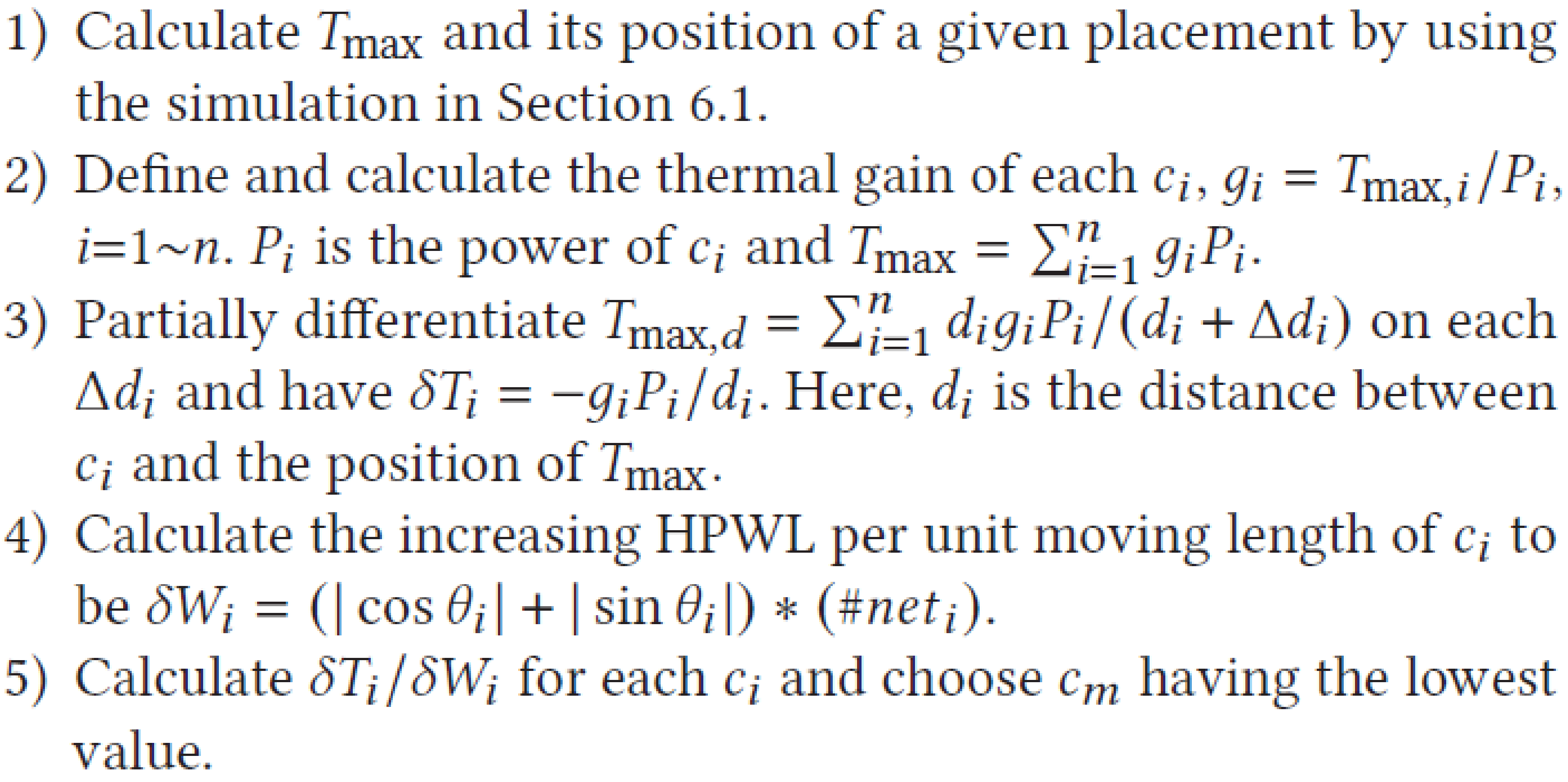




↑ Move one chiplet at a time

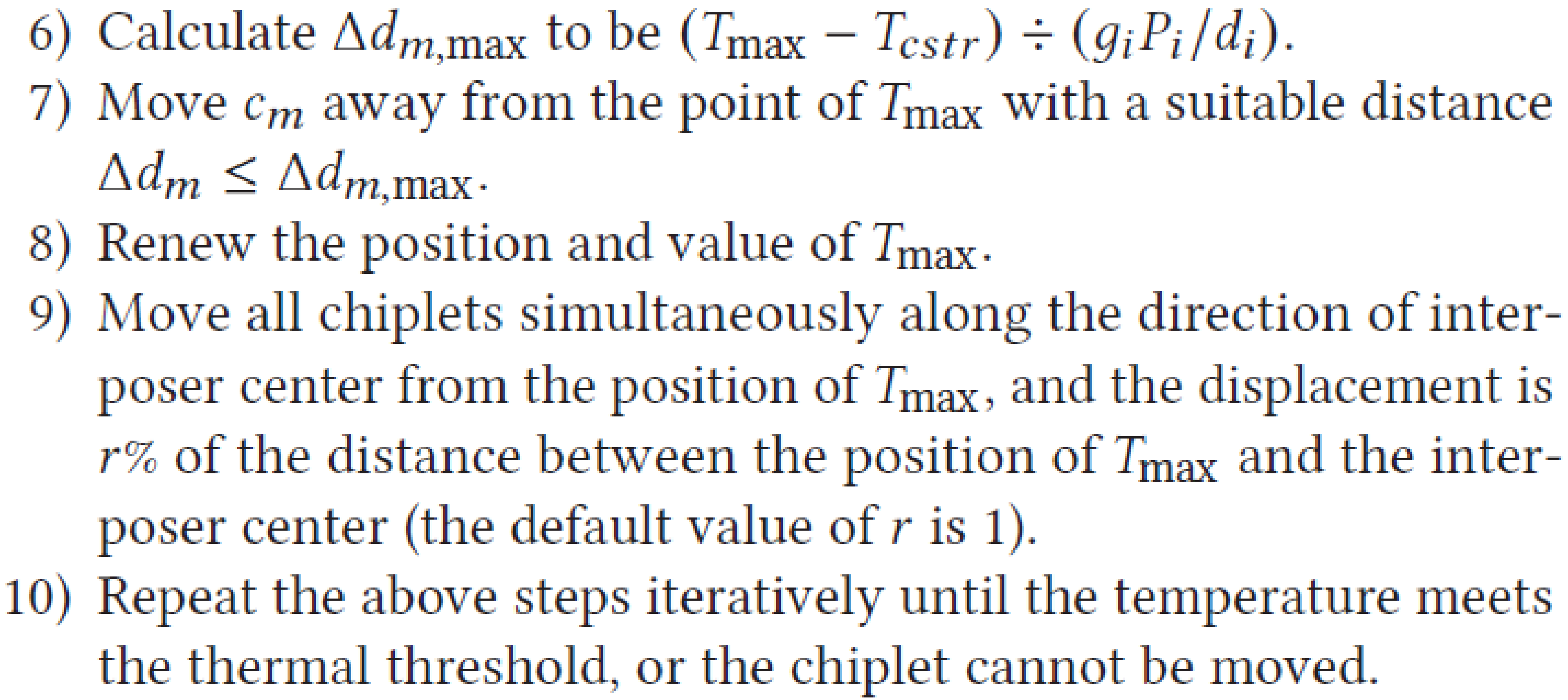
↑ Move all chiplet toward the center

Post Chiplet placement (post-cp) with thermal consideration



1) Calculate $T_{\max}$ and its position of a given placement by using the simulation in Section 6.1.
2) Define and calculate the thermal gain of each c_i, $g_i = T_{\max,i}/P_i$, i=1~n. P_i is the power of c_i and $T_{\max} = \sum_{i=1}^{n} g_i P_i$.
3) Partially differentiate $T_{\max,d} = \sum_{i=1}^{n} d_i g_i P_i/(d_i + \Delta d_i)$ on each Δd_i and have $\delta T_i = -g_i P_i/d_i$. Here, d_i is the distance between c_i and the position of $T_{\max}$.
4) Calculate the increasing HPWL per unit moving length of c_i to be $\delta W_i = (|\cos\theta_i| + |\sin\theta_i|) * (\#net_i)$.
5) Calculate $\delta T_i/\delta W_i$ for each c_i and choose c_m having the lowest value.

Post Chiplet placement (post-cp) with thermal consideration



6) Calculate $\Delta d_{m,\max}$ to be $(T_{\max} - T_{cstr}) \div (g_i P_i / d_i)$.
7) Move c_m away from the point of $T_{\max}$ with a suitable distance $\Delta d_m \leq \Delta d_{m,\max}$.
8) Renew the position and value of $T_{\max}$.
9) Move all chiplets simultaneously along the direction of interposer center from the position of $T_{\max}$, and the displacement is $r\%$ of the distance between the position of $T_{\max}$ and the interposer center (the default value of r is 1).
10) Repeat the above steps iteratively until the temperature meets the thermal threshold, or the chiplet cannot be moved.

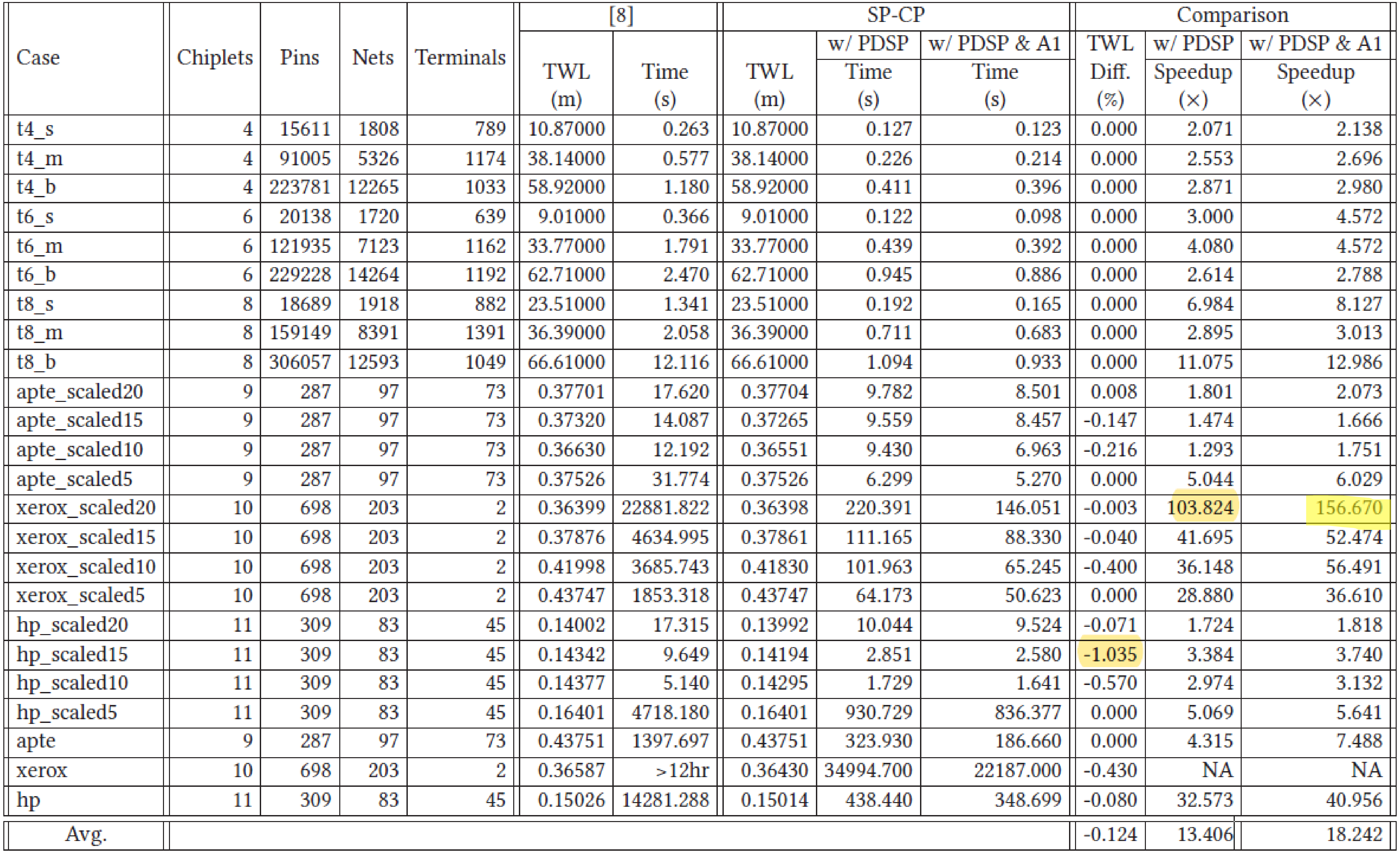
Experimental results

- C++ language with compiler gcc 8.3.1
- Execute on linux workstation
- CPU : Intex Xeon E5-2620 v4 with 8 cores at 2.10 GHz

- Benchmarks:

(1) Interposer-based chiplets case with 4, 6, 8 chiplets (t4/t6/t8)
(2) MCNC benchmarks with 9, 10, 11 chiplets (apte/xeron/hp)
(3) Modified MCNC benchmarks for practical 2.5D IC within whitespace from 5%~20%

Experimental results



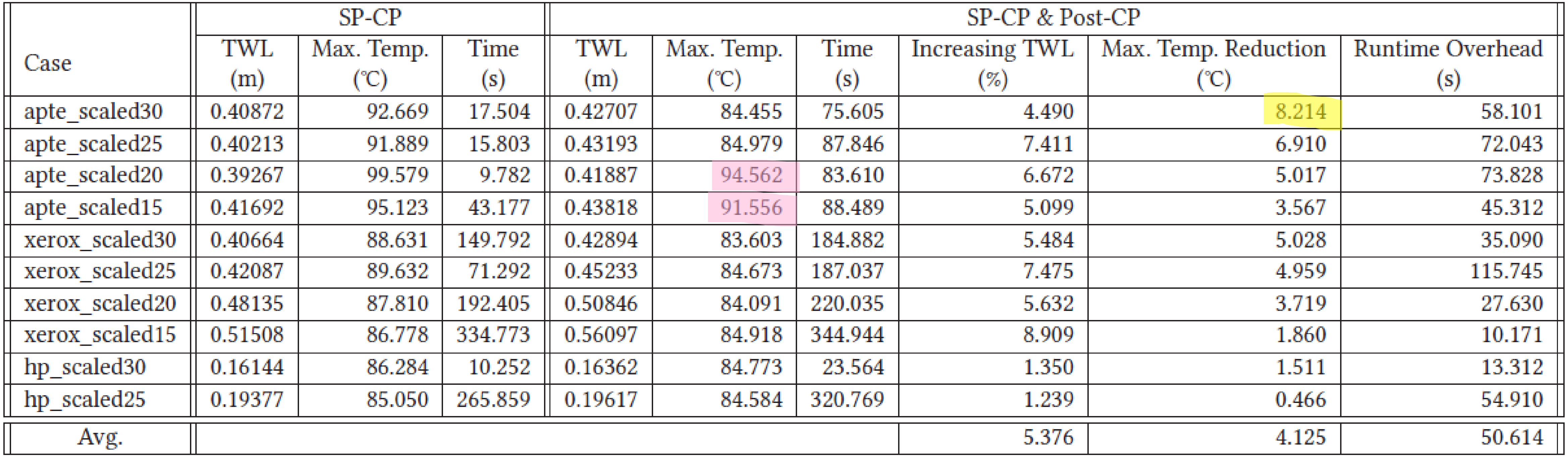
Case	Chiplets	Pins	Nets	Terminals	[8]		SP-CP			Comparison		
					TWL (m)	Time (s)	TWL (m)	w/ PDSP Time (s)	w/ PDSP & A1 Time (s)	TWL Diff. (%)	w/ PDSP Speedup (×)	w/ PDSP & A1 Speedup (×)
t4_s	4	15611	1808	789	10.87000	0.263	10.87000	0.127	0.123	0.000	2.071	2.138
t4_m	4	91005	5326	1174	38.14000	0.577	38.14000	0.226	0.214	0.000	2.553	2.696
t4_b	4	223781	12265	1033	58.92000	1.180	58.92000	0.411	0.396	0.000	2.871	2.980
t6_s	6	20138	1720	639	9.01000	0.366	9.01000	0.122	0.098	0.000	3.000	4.572
t6_m	6	121935	7123	1162	33.77000	1.791	33.77000	0.439	0.392	0.000	4.080	4.572
t6_b	6	229228	14264	1192	62.71000	2.470	62.71000	0.945	0.886	0.000	2.614	2.788
t8_s	8	18689	1918	882	23.51000	1.341	23.51000	0.192	0.165	0.000	6.984	8.127
t8_m	8	159149	8391	1391	36.39000	2.058	36.39000	0.711	0.683	0.000	2.895	3.013
t8_b	8	306057	12593	1049	66.61000	12.116	66.61000	1.094	0.933	0.000	11.075	12.986
apte_scaled20	9	287	97	73	0.37701	17.620	0.37704	9.782	8.501	0.008	1.801	2.073
apte_scaled15	9	287	97	73	0.37320	14.087	0.37265	9.559	8.457	-0.147	1.474	1.666
apte_scaled10	9	287	97	73	0.36630	12.192	0.36551	9.430	6.963	-0.216	1.293	1.751
apte_scaled5	9	287	97	73	0.37526	31.774	0.37526	6.299	5.270	0.000	5.044	6.029
xerox_scaled20	10	698	203	2	0.36399	22881.822	0.36398	220.391	146.051	-0.003	103.824	156.670
xerox_scaled15	10	698	203	2	0.37876	4634.995	0.37861	111.165	88.330	-0.040	41.695	52.474
xerox_scaled10	10	698	203	2	0.41998	3685.743	0.41830	101.963	65.245	-0.400	36.148	56.491
xerox_scaled5	10	698	203	2	0.43747	1853.318	0.43747	64.173	50.623	0.000	28.880	36.610
hp_scaled20	11	309	83	45	0.14002	17.315	0.13992	10.044	9.524	-0.071	1.724	1.818
hp_scaled15	11	309	83	45	0.14342	9.649	0.14194	2.851	2.580	-1.035	3.384	3.740
hp_scaled10	11	309	83	45	0.14377	5.140	0.14295	1.729	1.641	-0.570	2.974	3.132
hp_scaled5	11	309	83	45	0.16401	4718.180	0.16401	930.729	836.377	0.000	5.069	5.641
apte	9	287	97	73	0.43751	1397.697	0.43751	323.930	186.660	0.000	4.315	7.488
xerox	10	698	203	2	0.36587	>12hr	0.36430	34994.700	22187.000	-0.430	NA	NA
hp	11	309	83	45	0.15026	14281.288	0.15014	438.440	348.699	-0.080	32.573	40.956
Avg.										-0.124	13.406	18.242

Experimental results

$w_{space} = 0.1\ mm$ $T_{cstr} = 85℃$

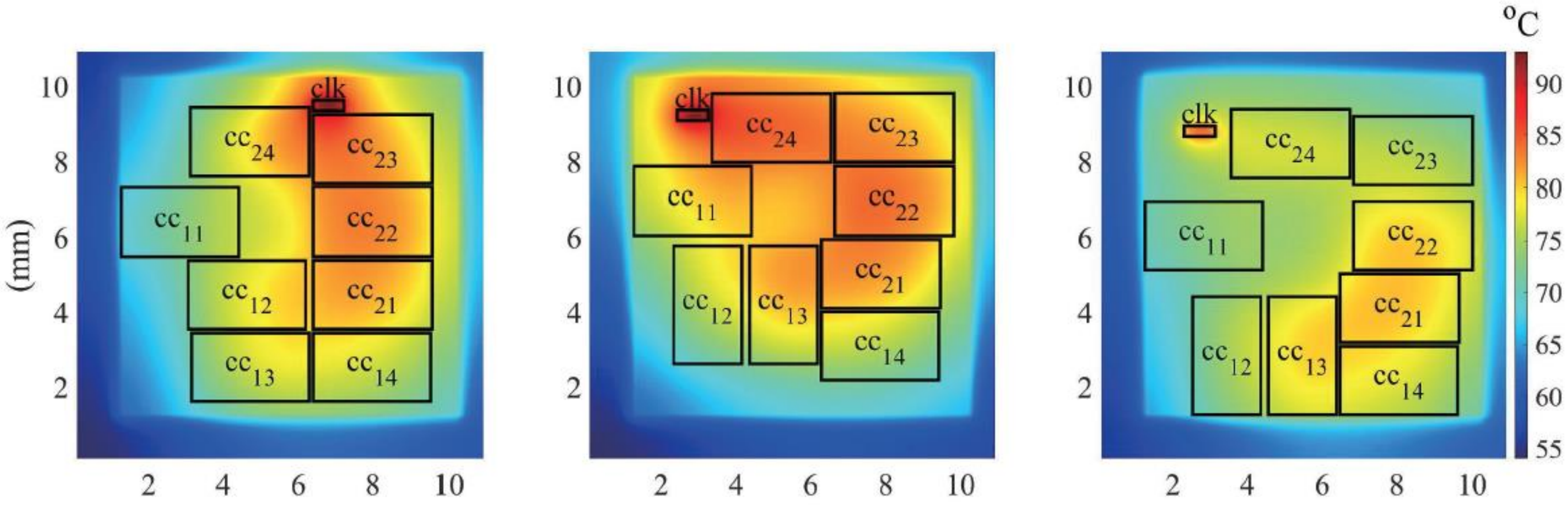
$\eta = 10$

$\Phi = 0.5$



Case	SP-CP			SP-CP & Post-CP					
	TWL (m)	Max. Temp. (℃)	Time (s)	TWL (m)	Max. Temp. (℃)	Time (s)	Increasing TWL (%)	Max. Temp. Reduction (℃)	Runtime Overhead (s)
apte_scaled30	0.40872	92.669	17.504	0.42707	84.455	75.605	4.490	8.214	58.101
apte_scaled25	0.40213	91.889	15.803	0.43193	84.979	87.846	7.411	6.910	72.043
apte_scaled20	0.39267	99.579	9.782	0.41887	94.562	83.610	6.672	5.017	73.828
apte_scaled15	0.41692	95.123	43.177	0.43818	91.556	88.489	5.099	3.567	45.312
xerox_scaled30	0.40664	88.631	149.792	0.42894	83.603	184.882	5.484	5.028	35.090
xerox_scaled25	0.42087	89.632	71.292	0.45233	84.673	187.037	7.475	4.959	115.745
xerox_scaled20	0.48135	87.810	192.405	0.50846	84.091	220.035	5.632	3.719	27.630
xerox_scaled15	0.51508	86.778	334.773	0.56097	84.918	344.944	8.909	1.860	10.171
hp_scaled30	0.16144	86.284	10.252	0.16362	84.773	23.564	1.350	1.511	13.312
hp_scaled25	0.19377	85.050	265.859	0.19617	84.584	320.769	1.239	0.466	54.910
Avg.							5.376	4.125	50.614

Experimental results



Thank you for listening