Siemens S7-1200

CPU 1212C AC/DC/Relay

Bit Logic Operations

- **SET** and **RESET** Instructions
- **Exercise Example**

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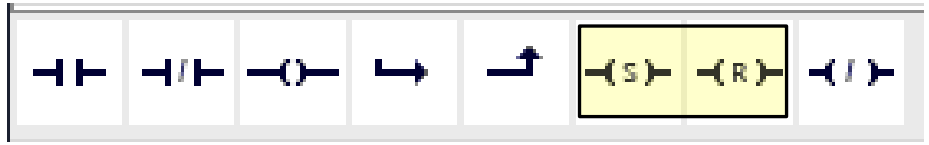
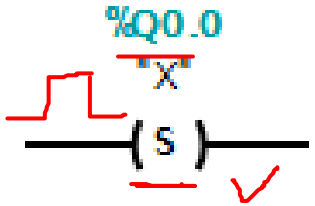
Bit Logic Instructions in LAD – SET and RESET (1)



SET Instruction

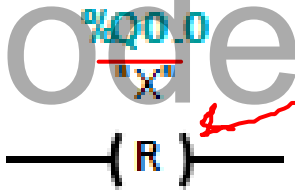
Symbol



When **S (Set) is activated**, then the data value at the **OUT address is set to 1**. When **S is not activated,** OUT is **not changed.**

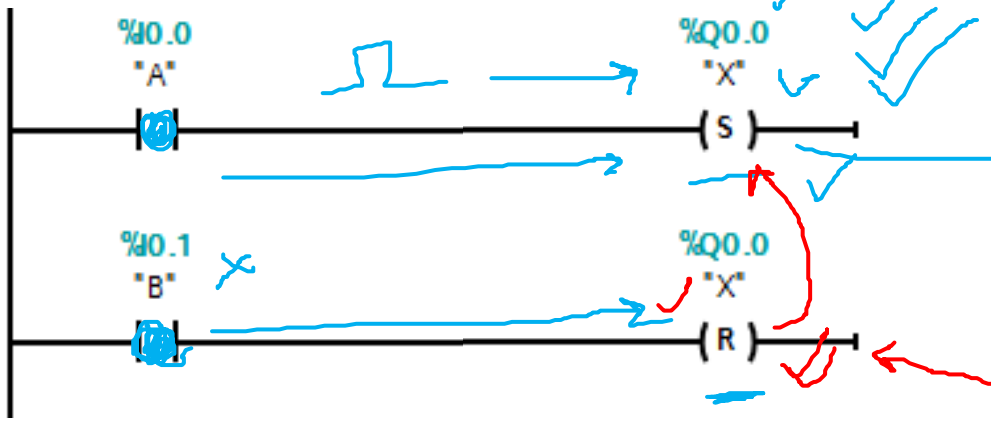
RESET Instruction

Symbol



When **R (Reset) is activated**, then the data value at the **OUT address is set to 0**. When **R is not activated,** OUT is **not changed.**

Example

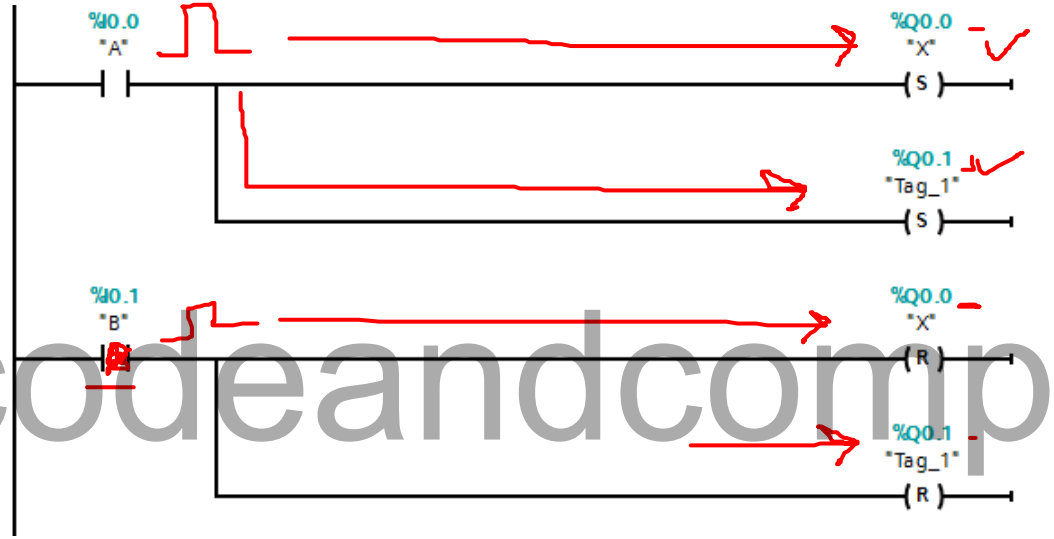


SET	RESET	OUT
I0.0	I0.1	Q0.0
0	0	Last State
0	1	0
1	0	1
1	1	0

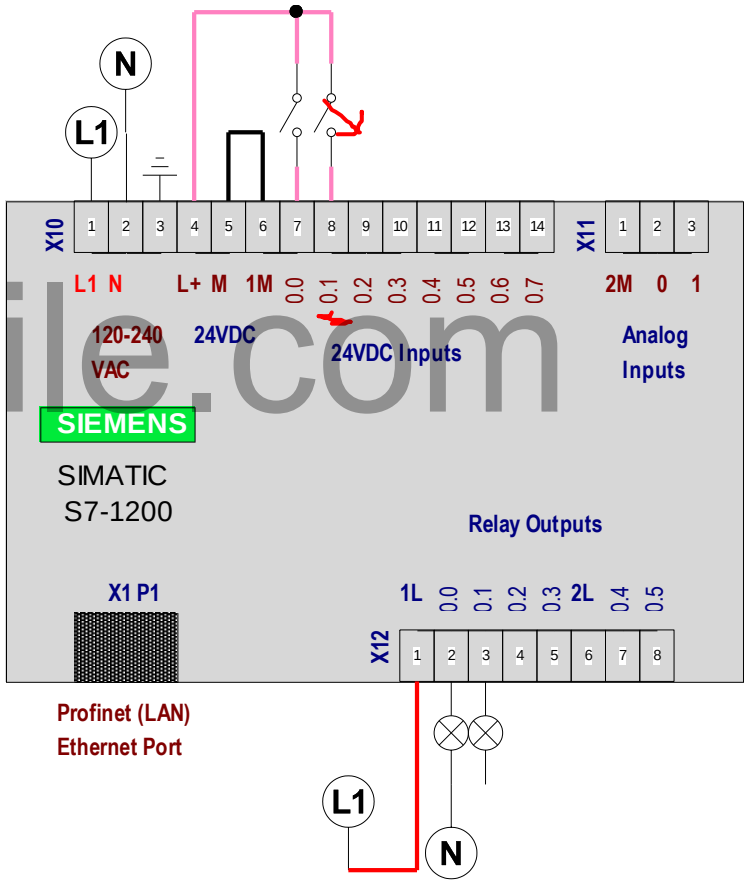
Exercise Example in Ladder

Write a Logic to latch two outputs Q0.0 & Q0.1 with I0.0 and unlatch it using I0.1

Ladder Solution



PLC Wiring



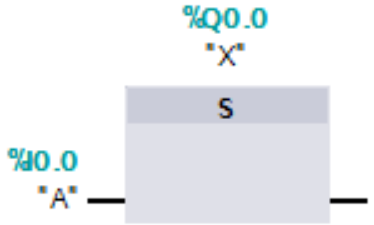
Required Condition

I0.0	I0.1	Q0.0	Q0.1
0	0	Last State	Last State
0	1	0	0
1	0	1	1
1	1	0	0

Bit Logic Instructions in FBD- SET & RESET (1)

SET Instruction

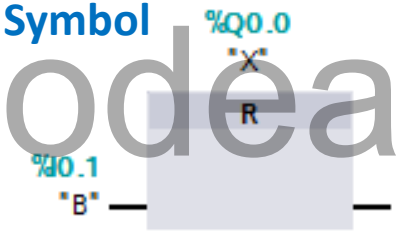
Symbol



When **S (Set) is activated**, then the data value at the **OUT address is set to 1**. When **S is not activated,** OUT is **not changed.**

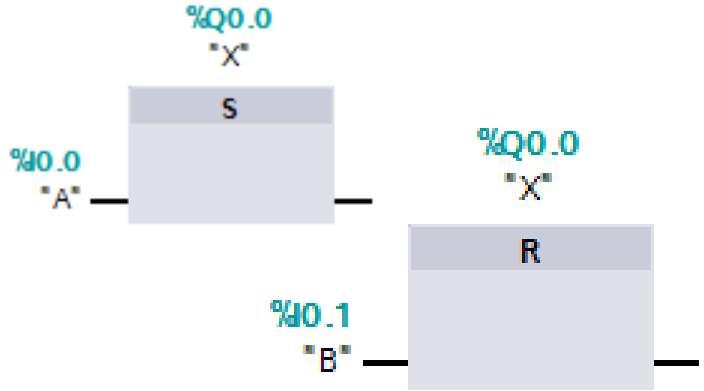
RESET Instruction

Symbol



When **R (Reset) is activated**, then the data value at the **OUT address is set to 0**. When **R is not activated,** OUT is **not changed.**

Example

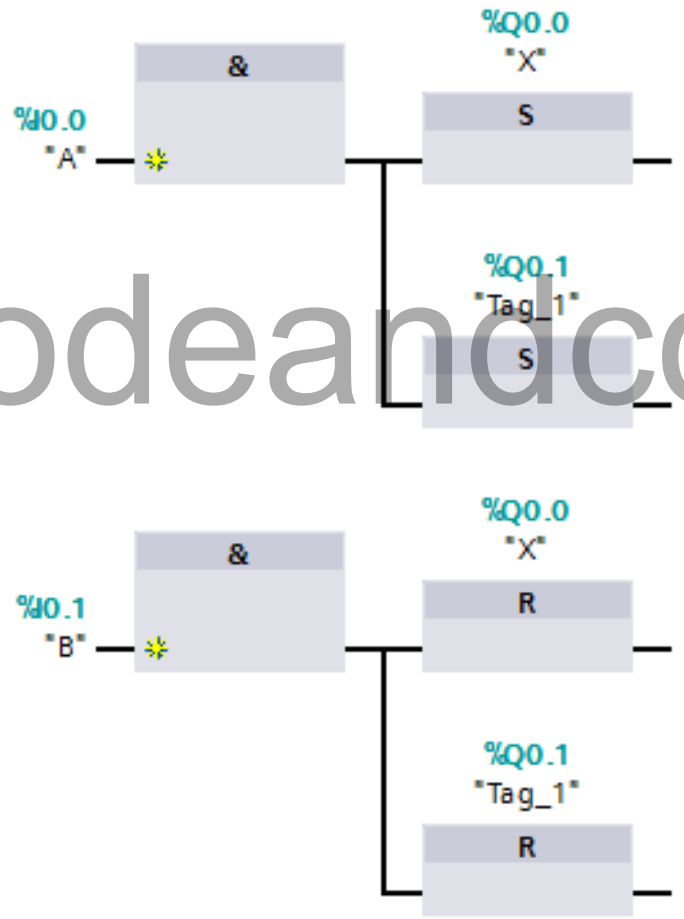


SET	RESET	OUT
I0.0	I0.1	Q0.0
0	0	Last State
0	1	0
1	0	1
1	1	0

Exercise Example in FBD

Write a Logic to latch two outputs Q0.0 & Q0.1 with I0.0 and unlatch it using I0.1

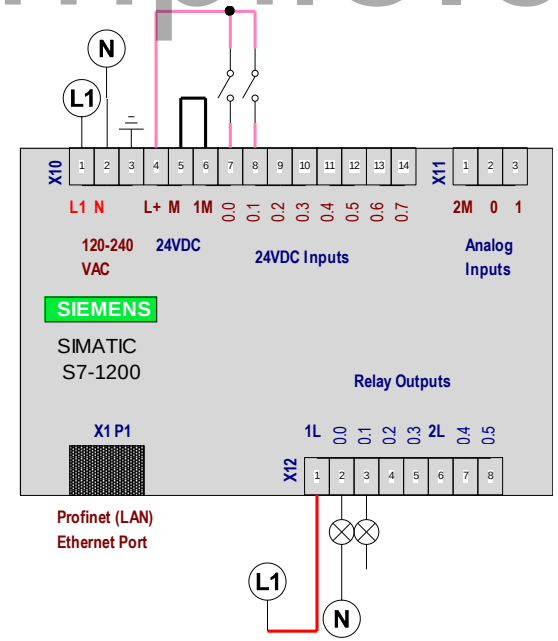
FBD Solution



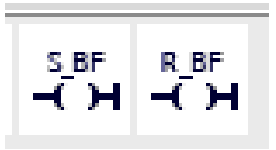
Required Condition

I0.0	I0.1	Q0.0	Q0.1
0	0	Last State	Last State
0	1	0	0
1	0	1	1
1	1	0	0

PLC Wiring

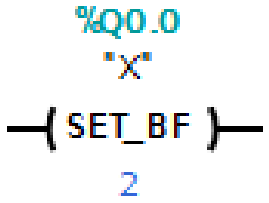


Bit Logic Instructions in LAD – **SET and RESET (Field)**



SET Instruction

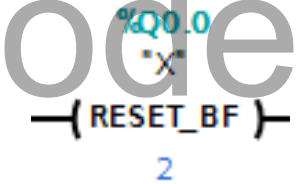
Symbol



When SET_BF is activated, a data value of 1 is assigned to "n“ bits starting at address tag OUT. When SET_BF is not activated, OUT is not changed

RESET Instruction

Symbol



RESET_BF writes a data value of 0 to "n" bits starting at address tag OUT. When RESET_BF is not activated, OUT is not changed.

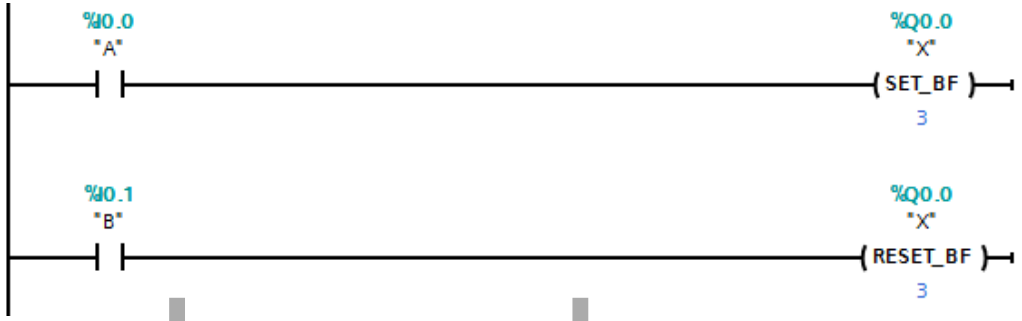
Example

SET	RESET	OUT 1	OUT 2	OUT 3
I0.0	I0.1	Q0.0	Q0.1	Q0.2
0	0	Last State	Last State	Last State
0	1	0	0	0
1	0	1	1	0
1	1	0	0	0

Exercise Example in LADDER

1. Write a Logic to latch three outputs Q0.0 ~ Q0.2 with I0.0 and unlatch all using I0.1

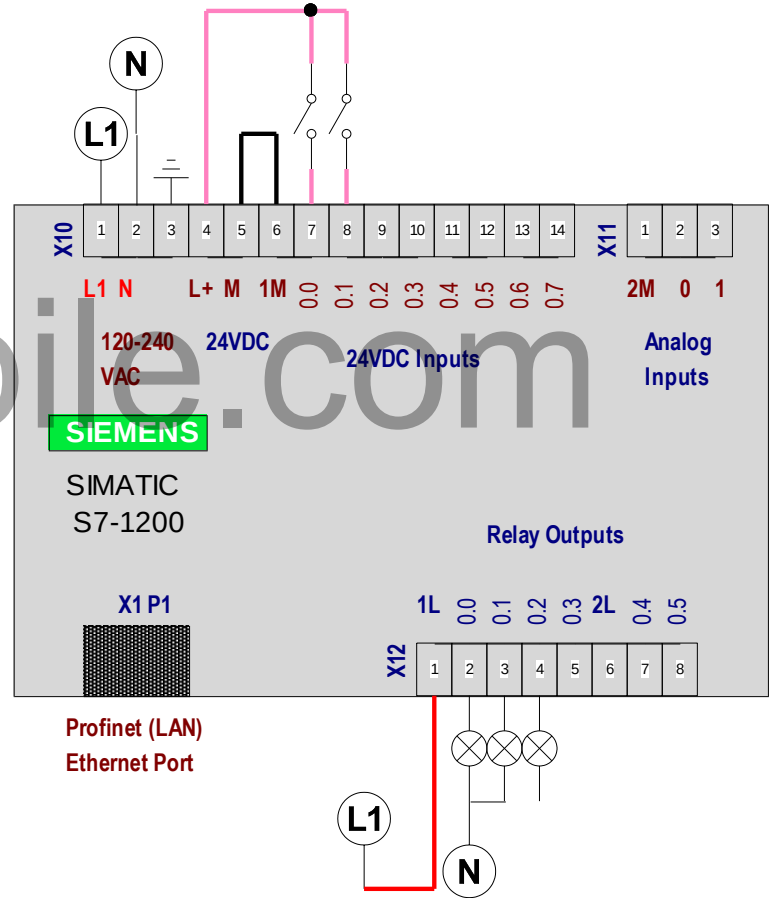
Ladder Solution



Required Condition

I0.0	I0.1	Q0.0	Q0.1	Q0.2
0	0	Last State	Last State	Last State
0	1	0	0	0
1	0	1	1	1
1	1	0	0	0

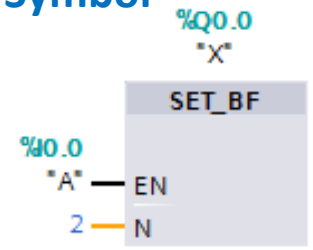
PLC Wiring



Bit Logic Instructions in FBD- SET & RESET (Field)

SET Instruction

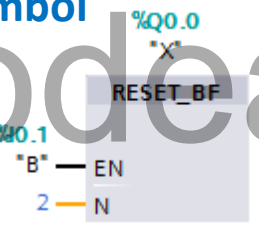
Symbol



When SET_BF is activated, a data value of 1 is assigned to "n“ bits starting at address tag OUT. When SET_BF is not activated, OUT is not changed

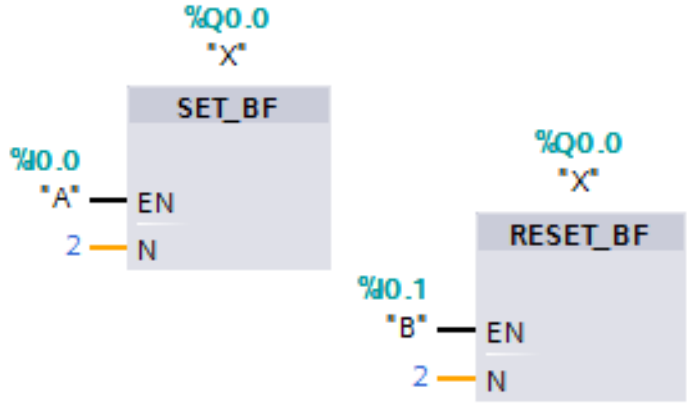
RESET Instruction

Symbol



RESET_BF writes a data value of 0 to "n" bits starting at address tag OUT. When RESET_BF is not activated, OUT is not changed.

Example

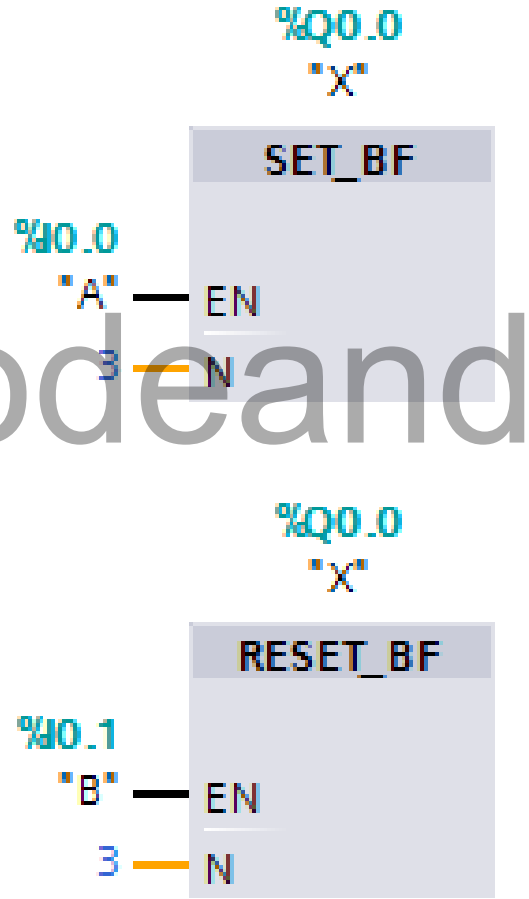


SET	RESET	OUT 1	OUT 2	OUT 3
I0.0	I0.1	Q0.0	Q0.1	Q0.2
0	0	Last State	Last State	Last State
0	1	0	0	0
1	0	1	1	0
1	1	0	0	0

Exercise Example in FBD

Write a Logic to latch three outputs Q0.0 ~ Q0.2 with I0.0 and unlatch all using I0.1

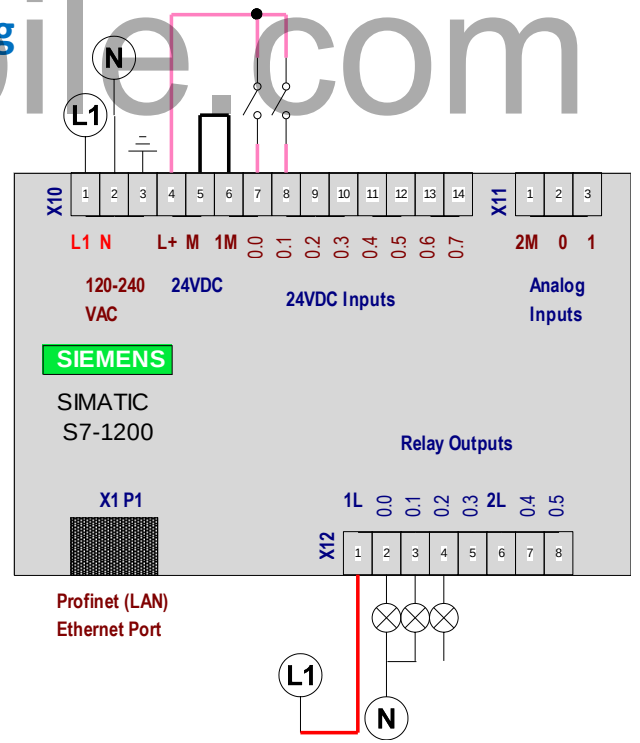
FBD Solution



Required Condition

I0.0	I0.1	Q0.0	Q0.1	Q0.2
0	0	Last State	Last State	Last State
0	1	0	0	0
1	0	1	1	1
1	1	0	0	0

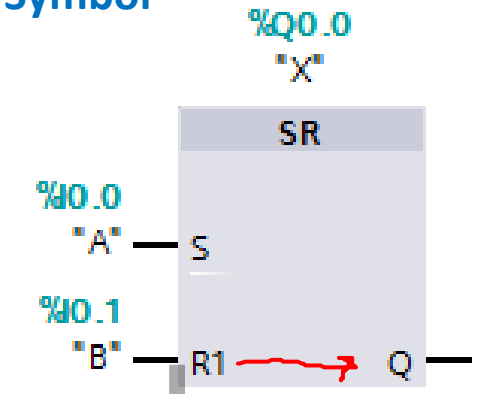
PLC Wiring



Bit Logic Instructions in FBD- SET Dominant & RESET Dominant

SET/ Reset Flip Flop

Symbol



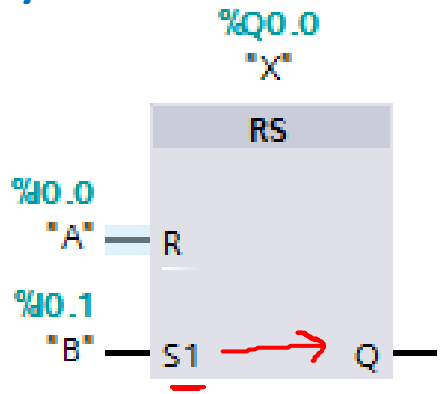
SR is a **reset dominant** latch where the **reset dominates. If the set (S) and reset (R1) signals** are both true, the value at address **Q0.0 will be 0.**

Truth Table

SET	RESET	OUT 1
I0.0	I0.1	Q0.0
0	0	Last State
0	1	0
1	0	1
1	1	0

Reset/ SET Flip Flop

Symbol



RS is a **set dominant** latch where the **set dominates**. If the **set (S1) and reset (R) signals are both true**, the value at **address Q0.0 will be 1.**

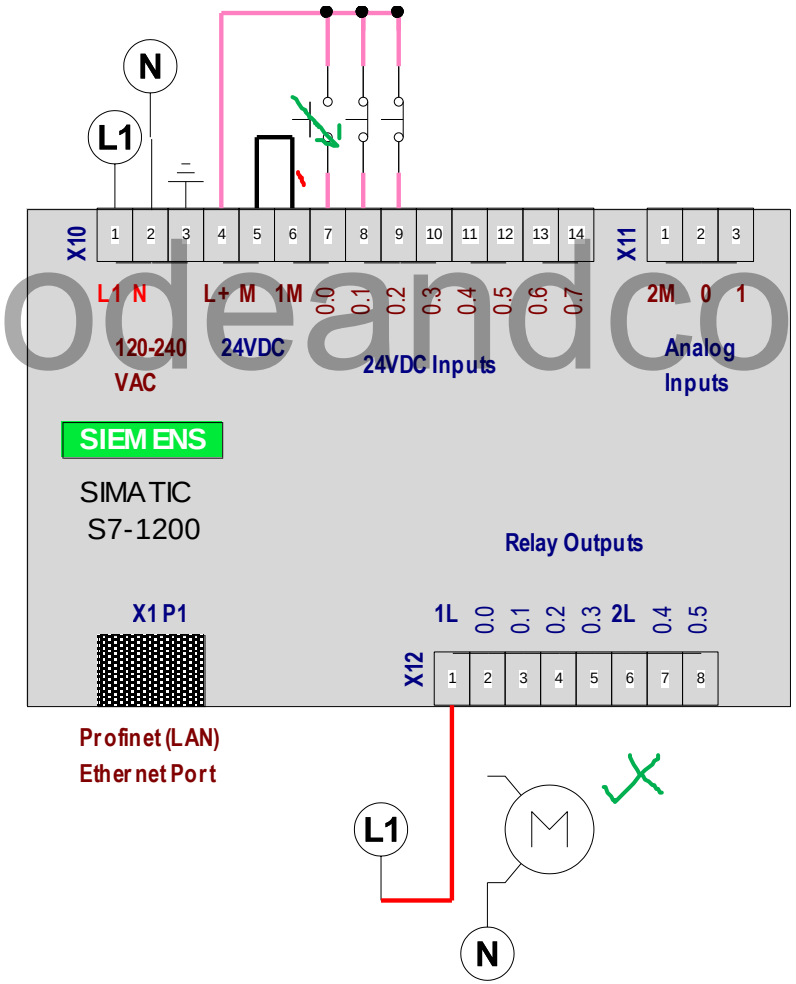
Truth Table

RESET	SET	OUT 1
I0.0	I0.1	Q0.0
0	0	Last State
0	1	1
1	0	0
1	1	0

Exercise Example in FBD

Write a Logic to latch the Motor Q0.0 with I0.0 (PB) and include two emergency switches I0.2 and I0.3 to unlatch it. Which Flip Flop you will use?

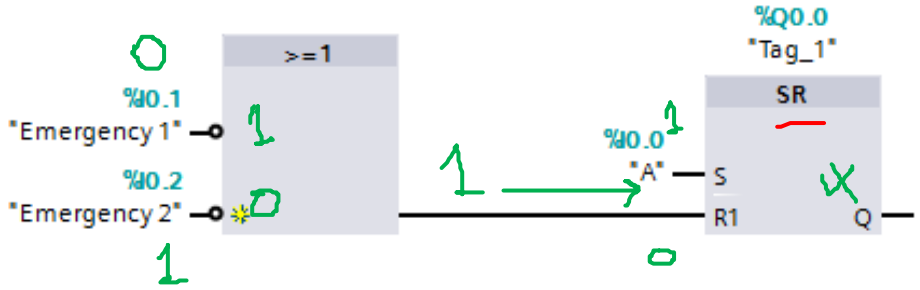
PLC Wiring



Required Condition

Contacts	Description
I0.0	Start the Motor
I0.2	Emergency Stop
I0.3	Emergency Stop
Q0.0	Motor

FBD Solution



What did we learn in this lesson?

- The **SET & RESET Bit** instruction is used to latch or unlatch **only one bit**.
- The **SET & RESET Field instruction** is used to latch or unlatch **multiple bits.**
- In **SET/RESET Flip Flop** the OUTPUT will be **FALSE** if both the inputs are **HIGH**
- In **RESET/SET Flip Flop** the OUTPUT will be **TRUE** if both the inputs are **HIGH**

Thank you

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