Siemens S7-1200

CPU 1212C AC/DC/Relay

Bit Logic Operations

- Understanding NO/ NC and OUT
- **Exercise Example**

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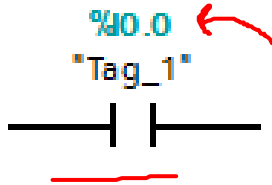
Bit Logic Instructions in LAD - NO

Normally Open Contact

Symbol



The Normally Open contact is **closed (ON)** when the assigned bit value **I0.0 is TRUE or equal to 1** and is **Open (OFF)** when **I0.0 is FALSE or equal to 0.**

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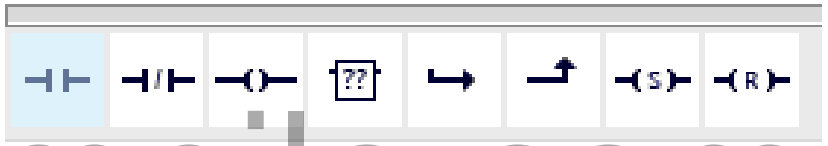
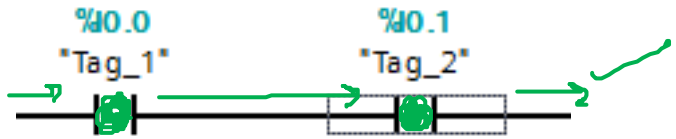
Normally Open contact

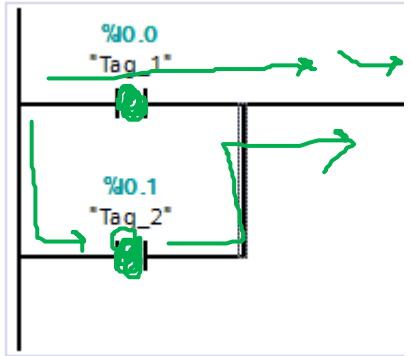


Example in Series – AND Logic



I0.0	I0.1	Output
0	0	FALSE
0	1	FALSE
1	0	FALSE
1	1	TRUE

Example in Parallel- OR Logic

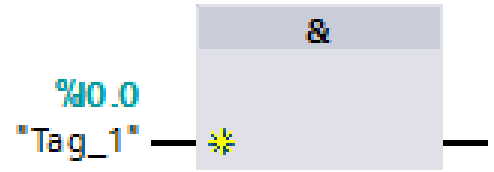


I0.0	I0.1	Output
0	0	FALSE
0	1	TRUE
1	0	TRUE
1	1	TRUE

Bit Logic Instructions in FBD- NO

Normally Open Contact

Symbol



The block “&” is **TRUE** when the assigned bit value **I0.0 is TRUE or equal to 1 and is FALSE** when the assigned bit value **I0.0 is FALSE or equal to 0 .**

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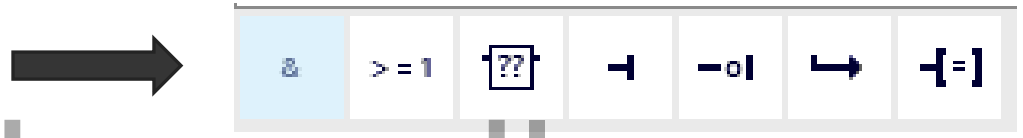
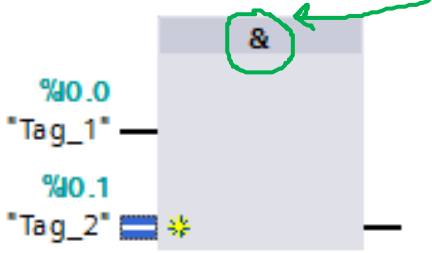
Normally Open contact

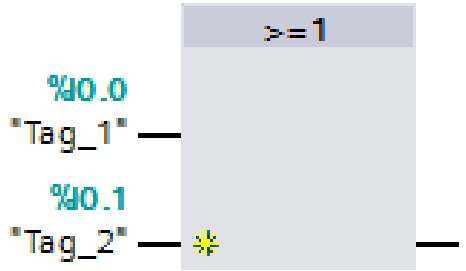


Example in Series – AND Logic



I0.0	I0.1	Output
0	0	FALSE
0	1	FALSE
1	0	FALSE
1	1	TRUE

Example in Parallel- OR Logic



I0.0	I0.1	Output
0	0	FALSE
0	1	TRUE
1	0	TRUE
1	1	TRUE

Bit Logic Instructions in LAD- NC

Normally Close Contact

Symbol

The Normally Close contact is **closed (ON)** when the assigned bit value **I0.0 is FALSE** or equal to 0 and it's **open (OFF)** when the assigned bit value **I0.0 is TRUE** or equal to 1.

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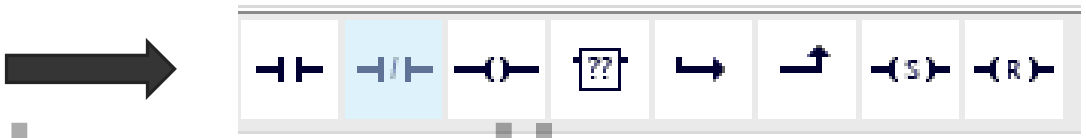
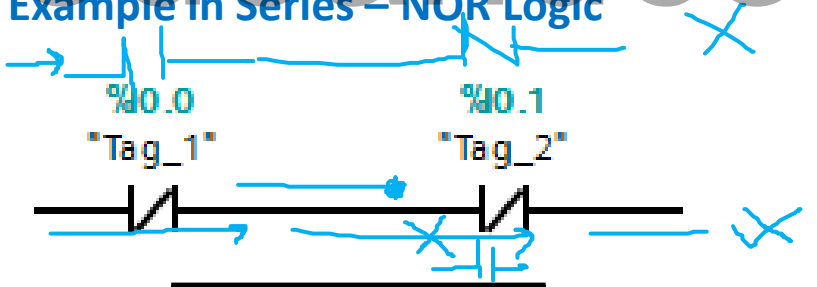
Normally Close contact

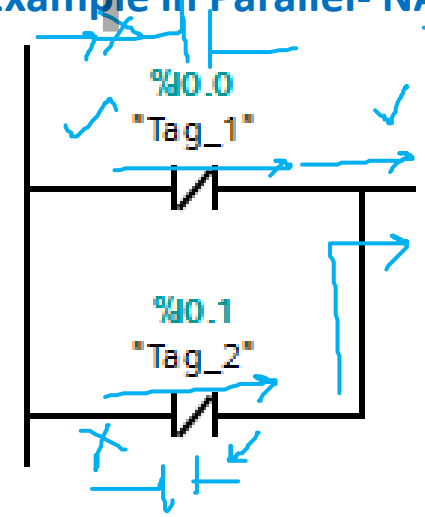


Example in Series – NOR Logic



I0.0	I0.1	Output
0	0	TRUE
0	1	FALSE
1	0	FALSE
1	1	FALSE

Example in Parallel- NAND Logic

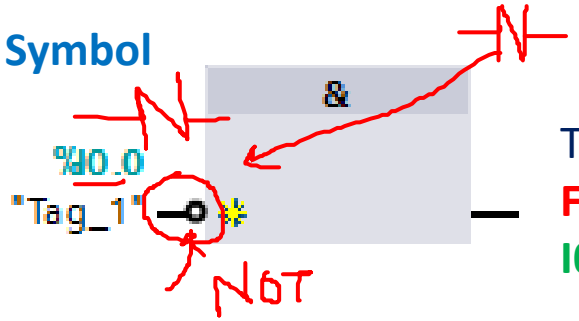


I0.0	I0.1	Output
0	0	TRUE
0	1	TRUE
1	0	TRUE
1	1	FALSE

Bit Logic Instructions in FBD- NC

Normally Close Contact

Symbol



The block "&" is **TRUE** when the assigned bit value **I0.0 is FALSE or equal to 0** and is **FALSE** when the assigned bit value **I0.0 is TRUE of equal to 1**

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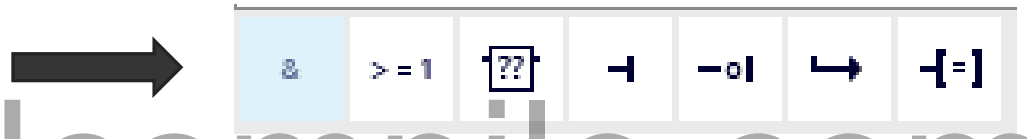
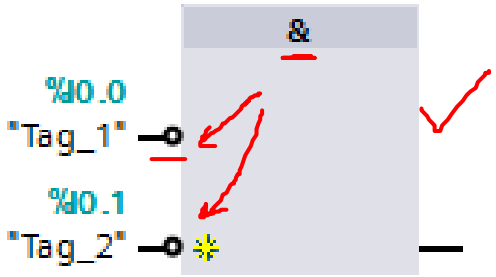
Normally close contact

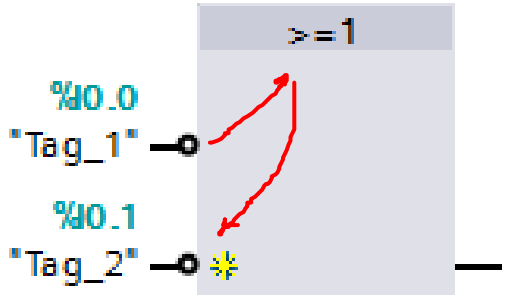


Example in Series – NOR Logic



I0.0	I0.1	Output
0	0	TRUE
0	1	FALSE
1	0	FALSE
1	1	FALSE

Example in Parallel- NAND Logic



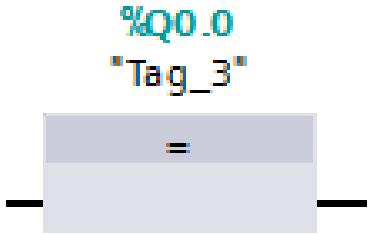
I0.0	I0.1	Output
0	0	TRUE
0	1	TRUE
1	0	TRUE
1	1	FALSE

Bit Logic Instructions in LAD & FBD- OUT

Output Coil

Ladder Symbol

FBD Symbol



The **coil output instruction** writes a value for an output bit. The OUT instruction is **TRUE** when state before in the branch is **TRUE**

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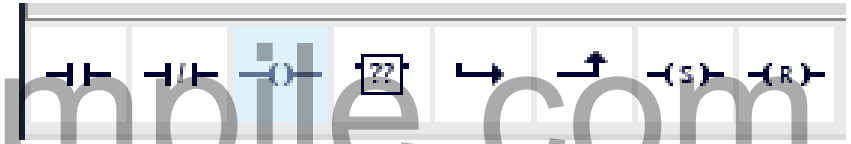
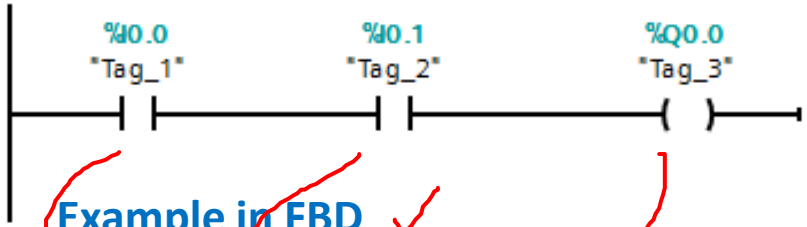
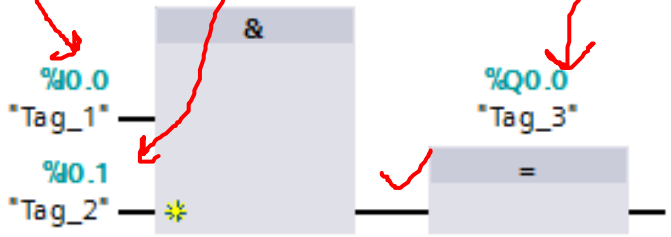
Output Coil



Example in Ladder



Example in FBD



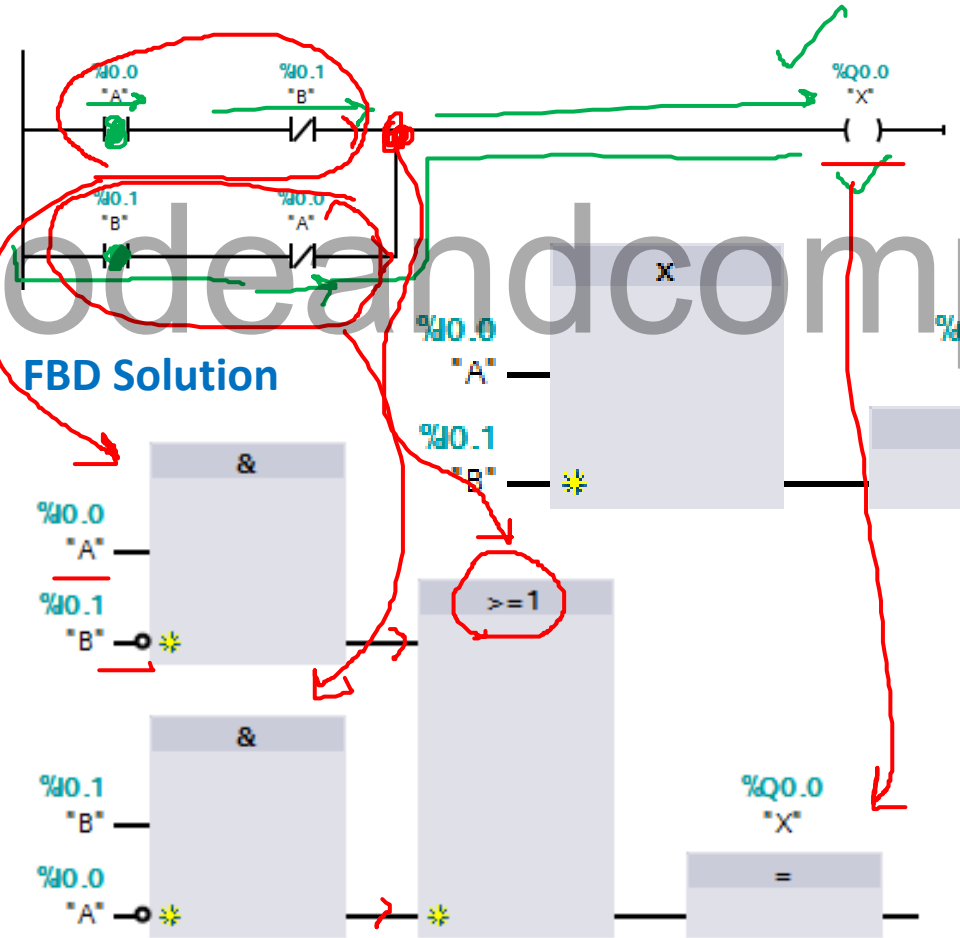
Truth Table

I0.0	I0.1	Q0.0
0	0	FALSE
0	1	FALSE
1	0	FALSE
1	1	TRUE

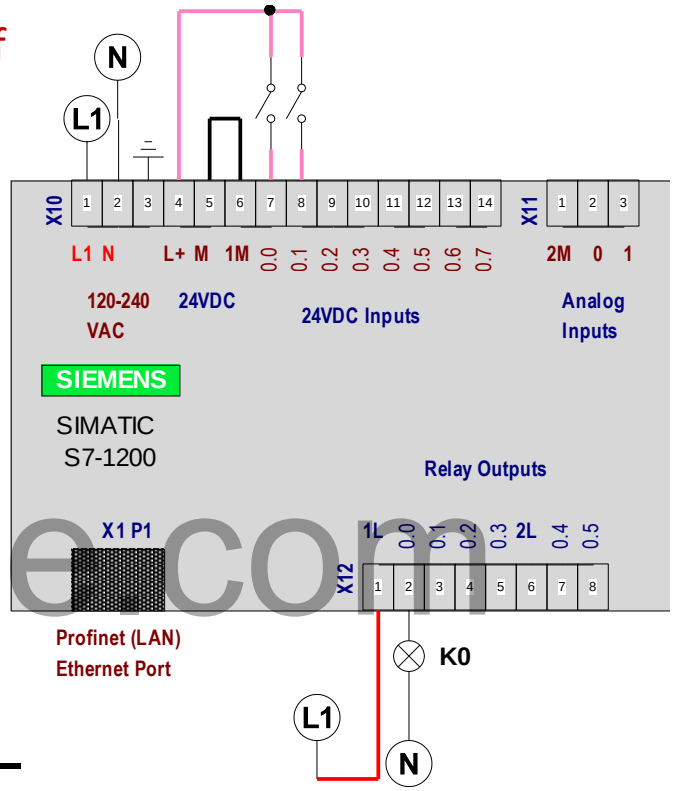
Exercise Example

1. Design XOR gate such that output is TRUE if only one of the two inputs is TRUE. - Assume you have two toggle buttons connected to PLC input

Ladder Solution



FBD Solution



Required Condition

I0.0	I0.1	Q0.0
0	0	FALSE
0	1	TRUE
1	0	TRUE
1	1	FALSE

What did we learn in this lesson?

- The **Normally Open contact** is closed (**ON**) when the assigned bit value is **equal to 1**.
- The **Normally Closed contact** is closed (**ON**) when the assigned bit value is **equal to 0.**
- The LAD **NOT contact** **inverts** the logical state of power flow input.
- If there is power flow through an output coil or an FBD "=" box is **enabled**, then the **output bit** is **set to 1**.

Thank you

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