

# SoC-NTM (T-DNC/NTM-SoC)

QueenField

## **0. Introduction**

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##### **0.0.1.2. Hardware Design Plan**

##### **0.0.1.3. Hardware Validation Plan**

##### **0.0.1.4. Hardware Verification Plan**

##### **0.0.1.5. Hardware Configuration Management Plan**

##### **0.0.1.6. Hardware Process Assurance Plan**

#### **0.0.2. HARDWARE DESIGN PROCESS**

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##### **0.0.2.2 Conceptual Design Process**

##### **0.0.2.3 Detailed Design Process**

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##### **0.0.3.2 Verification Process**

#### **0.0.4. CONFIGURATION MANAGEMENT PROCESS**

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**0.3.1. VHDL**

**0.3.2. Verilog**

**0.4. Design**

**0.4.1. VHDL**

**0.4.2. Verilog**

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**2.2.3. OR/NOR Gate**

**2.2.4. XOR/XNOR Gate**

**2.3. Combinational Logic**

**2.3.1. Arithmetic Circuits**

**2.3.2. Logic Circuits**

## 2.4. Finite State Machine

## 2.5. Pushdown Automaton

# 3. Neural Network

## 3.1. Feedforward Neural Network

## 3.2. Long Short Term Memory Neural Network

## 3.3. Transformer Neural Network

# 4. Turing Machine

## 4.1. Neural Turing Machine

### 4.1.1. Feedforward Neural Turing Machine

### 4.1.2. LSTM Neural Turing Machine

### 4.1.3. Transformer Neural Turing Machine

## 4.2. Differentiable Neural Computer

### 4.2.1. Feedforward Differentiable Neural Computer

### 4.2.2. LSTM Differentiable Neural Computer

### 4.2.3. Transformer Differentiable Neural Computer

# 5. Computer Architecture

## 5.1. von Neumann Architecture

### 5.1.1. Control Unit

### 5.1.2. ALU

### 5.1.3. Memory Unit

### 5.1.4. I/O Unit

## 5.2. Harvard Architecture

### 5.2.1. Control Unit

#### **5.2.2. ALU**

#### **5.2.3. Memory Unit**

#### **5.2.4. I/O Unit**

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##### **6.1.2. SIMD**

##### **6.1.3. MISD**

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#### **6.2. System on Chip**

##### **6.2.1. Bus on Chip**

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