

# MPSoC-NTM (T-DNC/NTM-MPSoC)

QueenField

## **0. Introduction**

### **0.1. Model**

#### **0.1.1. MatLab Language**

#### **0.1.2. Rust Language**

### **0.2. Design**

#### **0.2.1. VHDL**

#### **0.2.2. Verilog**

### **0.3. Verification**

#### **0.3.1. OSVVM-VHDL**

#### **0.3.2. UVM-Verilog**

## **1. Mechanics**

## **2. Information**

### **2.1. Bit**

### **2.2. Logic Gate**

#### **2.2.1. YES/NOT Gate**

#### **2.2.2. AND/NAND Gate**

#### **2.2.3. OR/NOR Gate**

#### **2.2.4. XOR/XNOR Gate**

### **2.3. Combinational Logic**

#### **2.3.1. Arithmetic Circuits**

#### **2.3.2. Logic Circuits**

#### 2.4. Finite State Machine

#### 2.5. Pushdown Automaton

### 3. Neural Network

#### 3.1. Feedforward Neural Network

#### 3.2. Long Short Term Memory Neural Network

#### 3.3. Transformer Neural Network

### 4. Turing Machine

#### 4.1. Neural Turing Machine

##### 4.1.1. Feedforward Neural Turing Machine

##### 4.1.2. LSTM Neural Turing Machine

##### 4.1.3. Transformer Neural Turing Machine

#### 4.2. Differentiable Neural Computer

##### 4.2.1. Feedforward Differentiable Neural Computer

##### 4.2.2. LSTM Differentiable Neural Computer

##### 4.2.3. Transformer Differentiable Neural Computer

### 5. Computer Architecture

#### 5.1. von Neumann Architecture

##### 5.1.1. Control Unit

##### 5.1.2. ALU

##### 5.1.3. Memory Unit

##### 5.1.4. I/O Unit

#### 5.2. Harvard Architecture

##### 5.2.1. Control Unit

##### 5.2.2. ALU

##### 5.2.3. Memory Unit

##### 5.2.4. I/O Unit

### 6. Advanced Computer Architecture

#### 6.1. Processing Unit

##### 6.1.1. SISD

**6.1.2. SIMD**

**6.1.3. MISD**

**6.1.4. MIMD**

**6.2. System on Chip**

**6.2.1. Bus on Chip**

**6.2.2. Network on Chip**

**6.3. Multi Processor System on Chip**