

# MPSoC-NTM (T-DNC/NTM-MPSoC)

QueenField

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#### 2.2.2. AND/NAND Gate

#### 2.2.3. OR/NOR Gate

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### 2.3. Combinational Logic

#### 2.3.1. Arithmetic Circuits

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### 3.1. Feedforward Neural Network

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### 4.1. Neural Turing Machine

#### 4.1.1. Feedforward Neural Turing Machine

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#### 4.1.3. Transformer Neural Turing Machine

### 4.2. Differentiable Neural Computer

#### 4.2.1. Feedforward Differentiable Neural Computer

#### 4.2.2. LSTM Differentiable Neural Computer

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## **5. Computer Architecture**

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#### **5.1.1. Control Unit**

#### **5.1.2. ALU**

#### **5.1.3. Memory Unit**

#### **5.1.4. I/O Unit**

### **5.2. Harvard Architecture**

#### **5.2.1. Control Unit**

#### **5.2.2. ALU**

#### **5.2.3. Memory Unit**

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#### **6.1.3. MISD**

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### **6.2. System on Chip**

#### **6.2.1. Bus on Chip**

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### **6.3. Multi Processor System on Chip**