PU-NTM (T-DNC/NTM-PU)

QueenField

0. INTRODUCTION

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- 1.1.2. Behavioral UML diagrams
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- 1.4. Validation
- 1.4.1. VHDL
- 1.4.2. Verilog
- 1.5. Design
- 1.5.1. VHDL
- 1.5.2. Verilog
- 1.6. Verification
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- 1.6.1.1. OSVVM Checker
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- 2.2.2.2. AND/NAND Gate
- 2.2.2.3. OR/NOR Gate
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- 2.2.3.1. Arithmetic Circuits
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- 2.2.4. Finite State Machine
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- 2.4.2.1. Feedforward Differentiable Neural Computer
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- 2.5.2.1. Control Unit
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- 2.5.2.3. Memory Unit
- 2.5.2.4. I/O Unit
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