# PU-NTM (T-DNC/NTM-PU)

# QueenField

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0.0.1.2. Hardware Design Plan
0.0.1.3. Hardware Validation Plan
0.0.1.4. Hardware Verification Plan
0.0.1.5. Hardware Configuration Management Plan
0.0.1.6. Hardware Process Assurance Plan
0.0.2. HARDWARE DESIGN PROCESS
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0.0.2.2 Conceptual Design Process
0.0.2.3 Detailed Design Process
0.0.2.4 Implementation Process
0.0.2.5 Production Transition Process
0.0.3. VALIDATION AND VERIFICATION PROCESS
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# 0.0.6. CERTIFICATION LIAISON PROCESS

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- 0.1.1.3. Composite diagram
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- 0.1.1.6. Package diagram
- 0.1.1.7. Profile diagram

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- 0.1.2.4. Sequence diagram
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- 0.2.1. MatLab Language
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- 0.3. Model
- 0.3.1. VHDL
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- 0.4.1. VHDL
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- 0.5. Verification
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- 0.5.1.1. OSVVM Checker
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- ${\bf 0.5.2.7.~UVM~Sequencer}$
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- 2.5. Pushdown Automaton
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- 4.2.2. LSTM Differentiable Neural Computer
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- 5.2. Harvard Architecture
- 5.2.1. Control Unit

- **5.2.2. ALU**
- 5.2.3. Memory Unit
- 5.2.4. I/O Unit
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