From the Processing Unit to the Multi-Processor System on Chip

A Multi-Processor System on Chip (MPSoC) is a System on Chip (SoC) which includes multiple Processing Units (PU). As such, it is a Multi-Core System-on-Chip. All PUs are linked to each other by a Network on Chip (NoC). These technologies meet the performance needs of multimedia applications, telecommunication architectures or network security.

1. INTRODUCTION

- 2. PROJECTS
- 2.1. Processing Unit
- 2.1.1. RISC-V PU
- 2.1.2. OpenRISC PU
- 2.1.3. MSP430 PU
- 2.2. Peripheral Devices
- 2.2.1. Debugger on Chip
- 2.2.2. Direct Access Memory
- 2.2.3. Master-Slave Interface
- 2.2.4. Network on Chip
- 2.2.5. Message Passing Interface
- 2.2.6. General Purpose Input Output
- 2.2.7. Multi-Port RAM for Instruction & Data

- 2.2.8. Single-Port RAM for Instruction & Data
- ${\bf 2.2.9.} \ \, {\bf Universal \ Asynchronous \ Receiver-Transmitter}$
- 2.3. System on Chip
- 2.3.1. RISC-V SoC
- 2.3.2. OpenRISC SoC
- 2.3.3. MSP430 SoC
- 2.4. Multi-Processor System on Chip
- 2.4.1. RISC-V MPSoC
- 2.4.2. OpenRISC MPSoC
- 2.4.3. MSP430 MPSoC

3. WORKFLOW

- 3.01. Modeling System Level Hardware
- 3.02. Simulating System Level Hardware
- 3.03. Verifying System Level Hardware
- 3.04. Describing Register Transfer Level Hardware
- 3.05. Simulating Register Transfer Level Hardware
- 3.06. Synthesizing Register Transfer Level Hardware
- 3.07. Optimizing Register Transfer Level Hardware
- 3.08. Verifying Register Transfer Level Hardware
- 3.09. Planning Switch Level Hardware
- 3.10. Placing Switch Level Hardware
- 3.11. Timing Switch Level Hardware
- 3.12. Routing Switch Level Hardware
- 3.13. Simulating Switch Level Hardware
- 3.14. Verifying Switch Level Hardware LVS
- 3.15. Checking Switch Level Hardware DRC
- 3.16. Printing Switch Level Hardware GDS

4. CONCLUSION