Francisco Javier Reina Campo
Electronic Engineer (Hardware and Software Engineer)
https://queenfield.tech

Integrated Circuits (ASIC & FPGA) described in VHDL & Verilog; verified and synthesized with **open source tools**; and printed with **open standard cells**

Modeling System ICs
Integrated Circuits modeled in System Description Languages such as SystemC or SystemVerilog

Simulating System ICs
Integrated Circuits simulated with open source tools such as Verilator (SystemC / SystemVerilog)

Verifying System ICs
Integrated Circuits verified using Universal Verification Methodology

Describing RTL ICs
Integrated Circuits described in traditional Hardware Description Languages such as VHDL or Verilog

Simulating RTL ICs
Integrated Circuits simulated with open source tools such as GHDL (VHDL) or Icarus Verilog (Verilog)

Synthesizing RTL ICs
Integrated Circuits synthesized with open source tools such as Yosys (Verilog)

Optimizing RTL ICs
Integrated Circuits optimized with open source tools such as ABC

Verifying RTL ICs
Integrated Circuits verified with open source tools such as SymbiYosys and using Formal Verification

Planning Switch ICs
Integrated Circuits floor-planned with open source tools such as Magic and using open standard cells

Placing Switch ICs
Integrated Circuits placed with open source tools such as Graywolf and using open standard cells

Timing Switch ICs
Integrated Circuits timing-analyzed with open source tools such as STA and using open standard cells

Routing Switch ICs
Integrated Circuits routed with open source tools such as Qrouter and using open standard cells

Simulating Switch ICs
Integrated Circuits simulated with open source tools such Irsim and using open standard cell

Verifying Switch ICs
Integrated Circuits verified with open source tools such Netgen LVS and using open standard cells

Checking Switch ICs
Integrated Circuits checked with open source tools such Magic DRC and using open standard cells

Printing Switch ICs
Integrated Circuits printed with open source tools such as Magic GDS and using open standard cells