***Open Source Projects*** *described, simulated, verified and synthesized with and* ***Open Source Tools*** *and printed with* ***Open Standard Cells****.*

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| **Processing Unit**  A Processing Unit (PU) is an electronic system within a computer that carries out instructions of a program by performing the basic arithmetic, logic, controlling, and I/O operations specified by instructions. Instruction-level parallelism is a measure of how many instructions in a computer can be executed simultaneously. The PU is contained on a single Metal Oxide Semiconductor (MOS) Integrated Circuit (IC). | | **Peripheral Devices**  The Peripheral Devices (PD) are systems that perform a specific function within a larger system (System on Chip). PDs need a PU and a SoC to work on their specific task.   |  |  |  | | --- | --- | --- | | *DBG* | *UART* | *MPI* | | *DMA* | *MSI* | *MPRAM* | | *SPRAM* | *GPIO* | *NoC* | | |
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|  | **PU-MSP430**  The MSP430 implementation has a 16 bit Microarchitecture, 3 stages data pipeline and an Instruction Set Architecture based on Reduced Instruction Set Computer. Compatible with Wishbone Bus. Only For Researching. | There are three levels of system organization:  · **PU Level**: this is the brain of the system.  · **SoC Level**: the brain and peripherals are integrated at this level.  · **MPSoC Level**: this is a communications system based on a Network on Chip (NoC). | |
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|  | **PU-OR1K**  The OpenRISC implementation has a 32/64 bit Microarchitecture, 5 stages data pipeline and an Instruction Set Architecture based on Reduced Instruction Set Computer. Compatible with Wishbone Bus. Only For Researching. |
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|  | **PU-RISCV**  The RISC-V implementation has a 32/64/128 bit Microarchitecture, 6 stages data pipeline and an Instruction Set Architecture based on Reduced Instruction Set Computer. Compatible with AMBA and Wishbone Buses. For Researching and Developing. |
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| **System on Chip**  A System on Chip (SoC) is an integrated circuit that integrates components of a computer system (PU, RAM, GPIO, etc). As they are integrated on a single substrate, SoCs consume much less power and take up much less area than multi-chip designs with equivalent functionality. SoCs are common in the mobile computing, embedded systems and the Internet of Things. | | **Multi-Processor System on Chip**  A Multi-Processor System on Chip (MPSoC) is a System on Chip (SoC) which includes multiple Processing Units (PU). As such, it is a Multi-Core System-on-Chip. All PUs are linked to each other by a Network on Chip (NoC). These technologies meet the performance needs of multimedia applications, telecommunication architectures or network security. | |
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|  | **SoC-MSP430**  System on Chip with MSP430-16 |  | **MPSoC-MSP430**  Multi-Processor System on Chip with MSP430-16 |
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|  | **SoC-OR1K**  System on Chip with OR1K-32 |  | **MPSoC-OR1K**  Multi-Processor System on Chip with OR1K-32 |
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|  | **SoC-RISCV**  System on Chip with RISCV-64 |  | **MPSoC-RISCV**  Multi-Processor System on Chip with RISCV-64 |