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|  |  | Integrated Circuits (ASIC & FPGA) described in VHDL & Verilog; verified and synthesized with **open source tools**; and printed with **open standard cells** |
| **Modeling System ICs** | **Simulating System ICs** |
| Integrated Circuits modeled in System Description Languages such as SystemC or SystemVerilog | Integrated Circuits simulated with open source tools such as Verilator (SystemC / SystemVerilog) |
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| **Verifying System ICs** | **Describing RTL ICs** |
| Integrated Circuits verified using Universal Verification Methodology | Integrated Circuits described in traditional Hardware Description Languages such as VHDL or Verilog |
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| **Simulating RTL ICs** | **Synthesizing RTL ICs** |
| Integrated Circuits simulated with open source tools such as GHDL (VHDL) or Icarus Verilog (Verilog) | Integrated Circuits synthesized with open source tools such as Yosys (Verilog) |
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| **Optimizing RTL ICs** | **Verifying RTL ICs** |
| Integrated Circuits optimized with open source tools such as ABC | Integrated Circuits verified with open source tools such as SymbiYosys and using Formal Verification |
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| **Planning Switch ICs** | **Placing Switch ICs** |
| Integrated Circuits floor-planned with open source tools such as Magic and using open standard cells | Integrated Circuits placed with open source tools such as Graywolf and using open standard cells |
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| **Timing Switch ICs** | **Routing Switch ICs** |
| Integrated Circuits timing-analyzed with open source tools such as STA and using open standard cells | Integrated Circuits routed with open source tools such as Qrouter and using open standard cells |
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| **Simulating Switch ICs** | **Verifying Switch ICs** |
| Integrated Circuits simulated with open source tools such Irsim and using open standard cell | Integrated Circuits verified with open source tools such Netgen LVS and using open standard cells |
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| **Checking Switch ICs** | **Printing Switch ICs** |
| Integrated Circuits checked with open source tools such Magic DRC and using open standard cells | Integrated Circuits printed with open source tools such as Magic GDS and using open standard cells |
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