

Paco Reina Campo

Abstract

Systems.

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		5.2.2 SoC-DNC

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OVERVIEW

1.1 DEPENDENCES

Sc. MSP430

Architecture

MPSoC DAG

MPSoC DAG

MPSoC DAG

Architecture

Architecture

Architecture

Architecture

MSoC DAG

MSoC DAG

Architecture

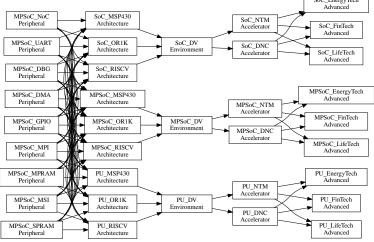


Figure 1.1: Dependences

1.2 HARDWARE PROJECT

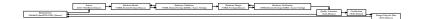


Figure 1.2: Hardware Project

1.3 SOFTWARE PROJECT
Software Deleted Software De
Figure 1.3: Software Project

PERIPHERAL

	MPSoC-DBG
2.2	MPSoC-DMA
	MPSoC-GPIO
2.4	MPSoC-MPI
	MPSoC-MPRAM

2.6	MPSoC-MSI
2.7	MPSoC-NoC
2.8	MPSoC-SPRAM
2.9	MPSoC-UART
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ARCHITECTURE

	PROCESSIGN UNIT
3.1.1	PU-MSP430
3.1.2	PU-OR1K
3.1.3	PU-RISCV
3.2	SYSTEM ON CHIP
	SoC-MSP430

	SoC-OR1K
	SoC-RISCV
	MULTI-PROCESSOR SYSTEM ON CHIP
	MPSoC-MSP430
··· ··· ·· ·	
	MPSoC-OR1K
	MPSoC-RISCV

ENVIRONMENT

	
4.1	DESIGN AND VERIFICATION
4.1.1	$\operatorname{PU-DV}$
	$\mathbf{SoC} ext{-}\mathbf{DV}$
4.1.3	MPSoC-DV
4.2	REAL TIME OPERATING SYSTEM
	
4.2.1	PU-RTOS

4.2.2	SoC-RTOS
4.2.3	MPSoC-RTOS

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INTELLIGENCE

	•
5.1	NEURAL TURING MACHINE
	·
5.1.1	PU-NTM
K 1 9	$\mathbf{SoC} ext{-}\mathbf{NTM}$
5.1.3	MPSoC-NTM
	· ••••
5.2	DIFFERENTIABLE NEURAL COMPUTER
5.2.1	PU-DNC

5.2.2 SoC-DNC		
5.2.3 MPSoC-DNC		
5.2.3 MPSoC-DNC		
5.2.3 MPSoC-DNC	522	SoC-DNC
5.2.3 MPSoC-DNC	0.2.2	500-0110
5.2.3 MPSoC-DNC		
5.2.3 MPSoC-DNC		
5.2.3 MPSoC-DNC		
		AFDG G DAIG
	5.2.3	MPSoC-DNC

...

APPLICATION

6.1	FINANCIAL TECHNOLOGY	
0.1	TINANCIAL TECHNOLOGI	
6.1.1	PU-FinTech	
	MPSoC_GPIO	
	Peripheral	
	MPSoC_MPI Peripheral	
	MPSoC_MPRAM	
	Peripheral PU_MSP430	
	MPSoC_MSI Peripheral Peripheral	
	PU_OR1K PU_DV PU_FinfTech Advanced PU_DNC PU_DNC PU_DNC PU_DNC PU_DNC	
	Peripheral PU_RISCV Advanced	
	MPSoC_UART Architecture Peripheral	
	MPSoC_DBG	
	Peripheral	
	MPSoC_DMA Peripheral	
	Figure 6 1. PH FinTech	

6.1.2 SoC-FinTech

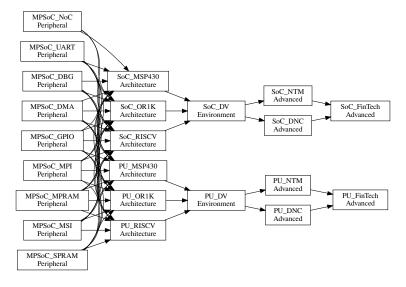


Figure 6.2: SoC FinTech

6.1.3 MPSoC-FinTech

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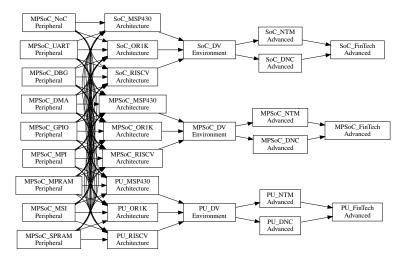


Figure 6.3: MPSoC FinTech

ENERGY TECHNOLOGY 6.2.1 PU-EnergyTech ... MPSoC_GPIO Peripheral MPSoC_MPI Peripheral MPSoC_MPRAM Peripheral PU_MSP430 Architecture MPSoC MSI PU NTM Peripheral PU OR1K PU DV PU_EnergyTech Advanced Architecture Environment MPSoC SPRAM PU DNC Peripheral PU_RISCV Architecture MPSoC_UART Peripheral MPSoC_DBG Peripheral MPSoC_DMA Peripheral Figure 6.4: PU EnergyTech 6.2.2 SoC-EnergyTech MPSoC_NoC Peripheral MPSoC UART SoC_MSP430 Architecture MPSoC_DBG Peripheral SoC_NTM Advanced MPSoC_DMA Peripheral SoC_OR1K Architecture SoC_DV Environment SoC_EnergyTech Advanced SoC_DNC Advanced MPSoC_GPIO Peripheral SoC RISCV Architecture MPSoC_MPI Peripheral PU_MSP430 Architecture

Figure 6.5: SoC EnergyTech

PU_DV Environment

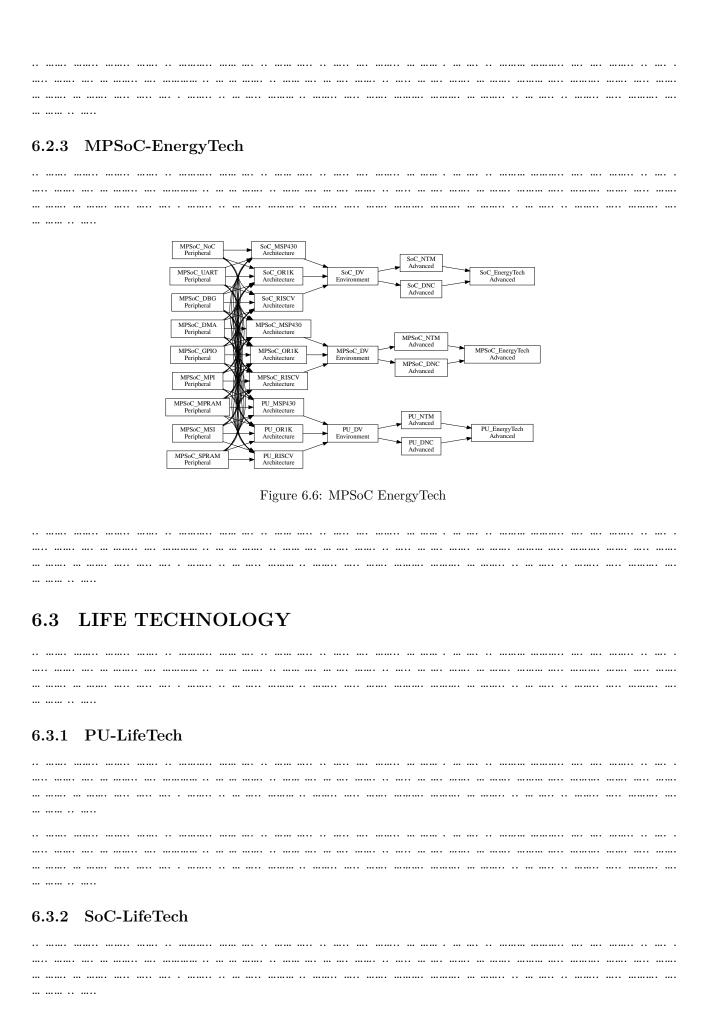
PU_DNC Advanced PU_EnergyTech Advanced

MPSoC_MPRAM Peripheral

MPSoC MSI

MPSoC_SPRAM Peripheral PU_OR1K Architecture

PU RISCV



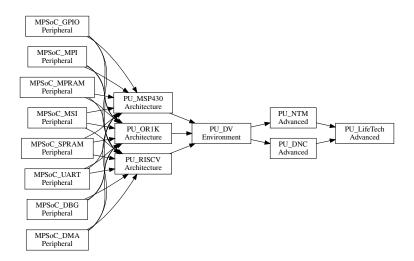


Figure 6.7: PU LifeTech

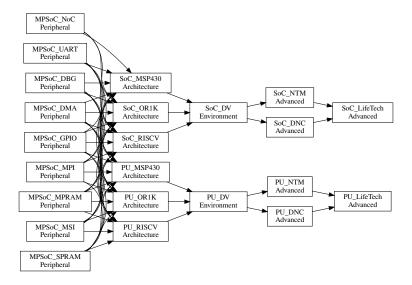


Figure 6.8: SoC LifeTech

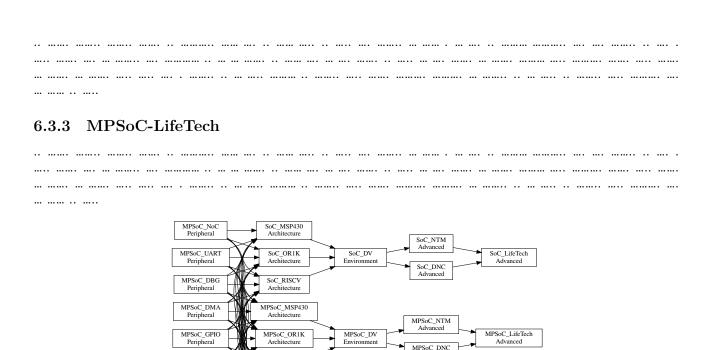


Figure 6.9: MPSoC LifeTech

PU_DV Environment

MPSoC_MPI Peripheral

MPSoC_MPRAM Peripheral

MPSoC_MSI

MPSoC_SPRAM Peripheral MPSoC_RISCV Architecture

PU_MSP430

PU OR1K

PU_RISCV Architecture Advanced

PU_NTM Advanced

> PU_DNC Advanced

PU_LifeTech

Advanced