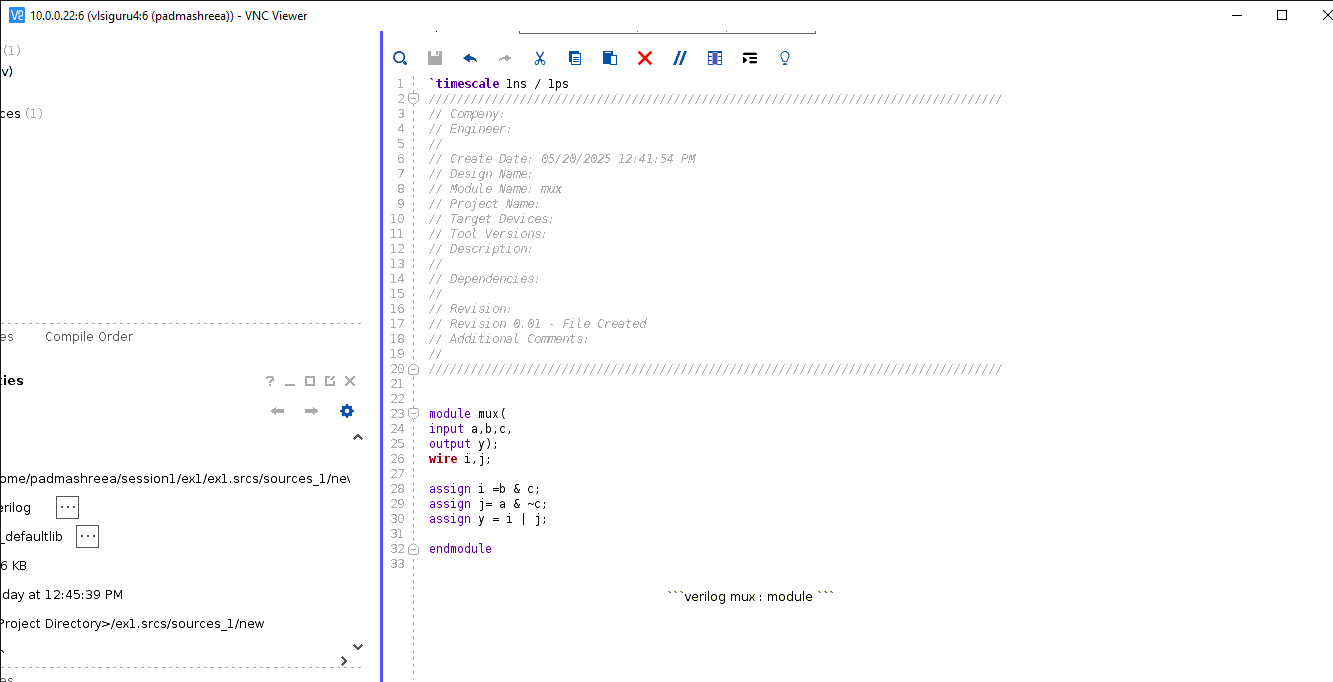
**Test circuit**

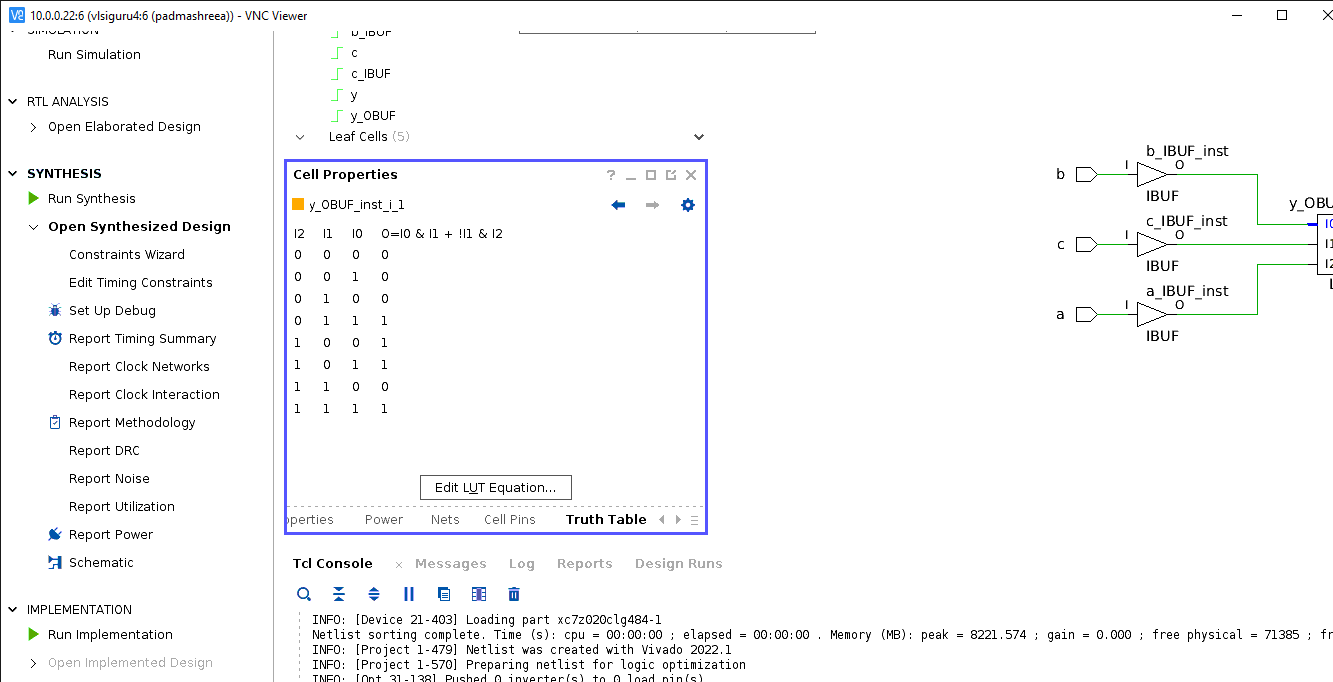
**Test circuit design code:**

In vivado software, I have created Verilog file for test circuit and written the code in it.

****

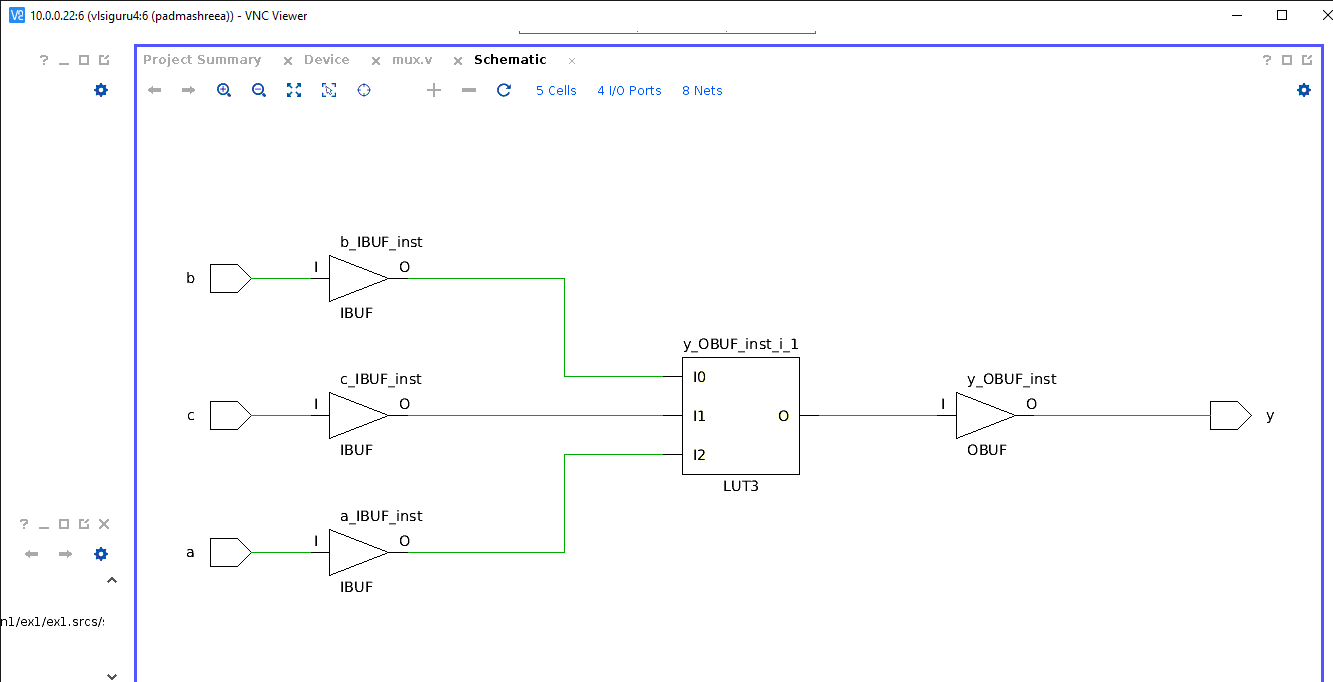
**Test circuit truth table**

From synthesis we got the truth table as it shown in bellow

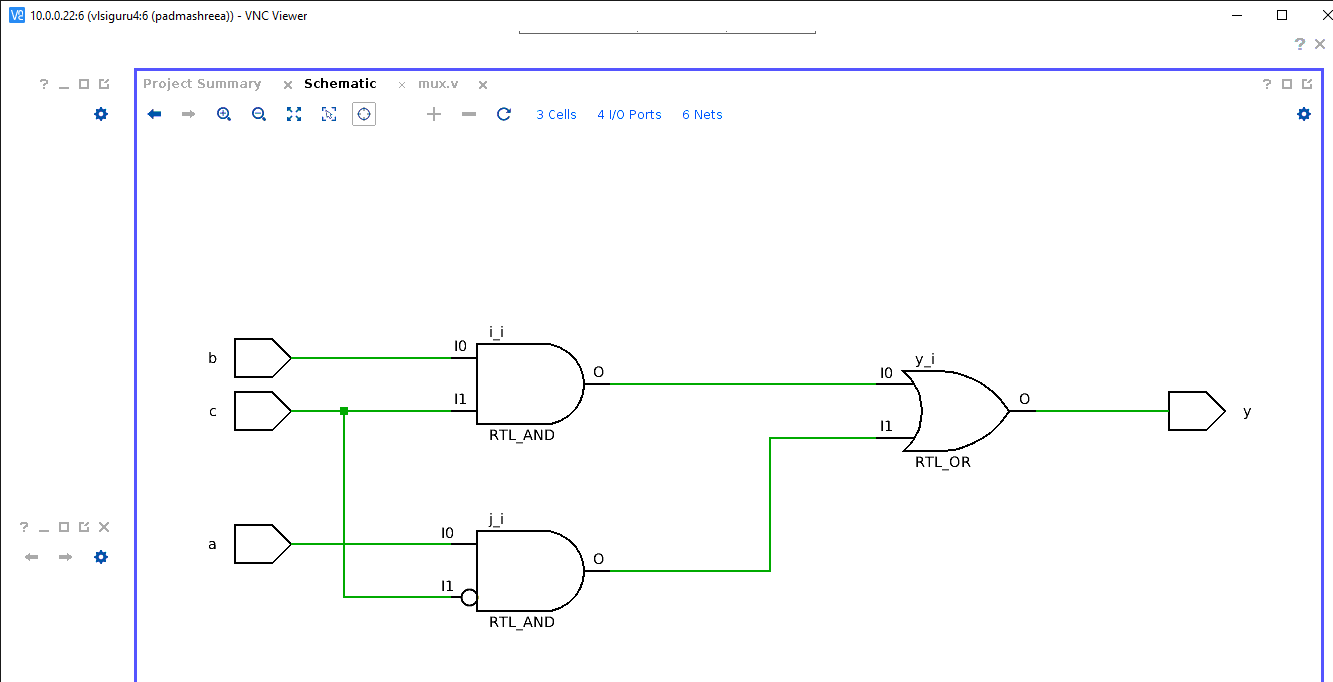


**Test circuit schematic diagram**

From synthesis we got schematic diagram as below.

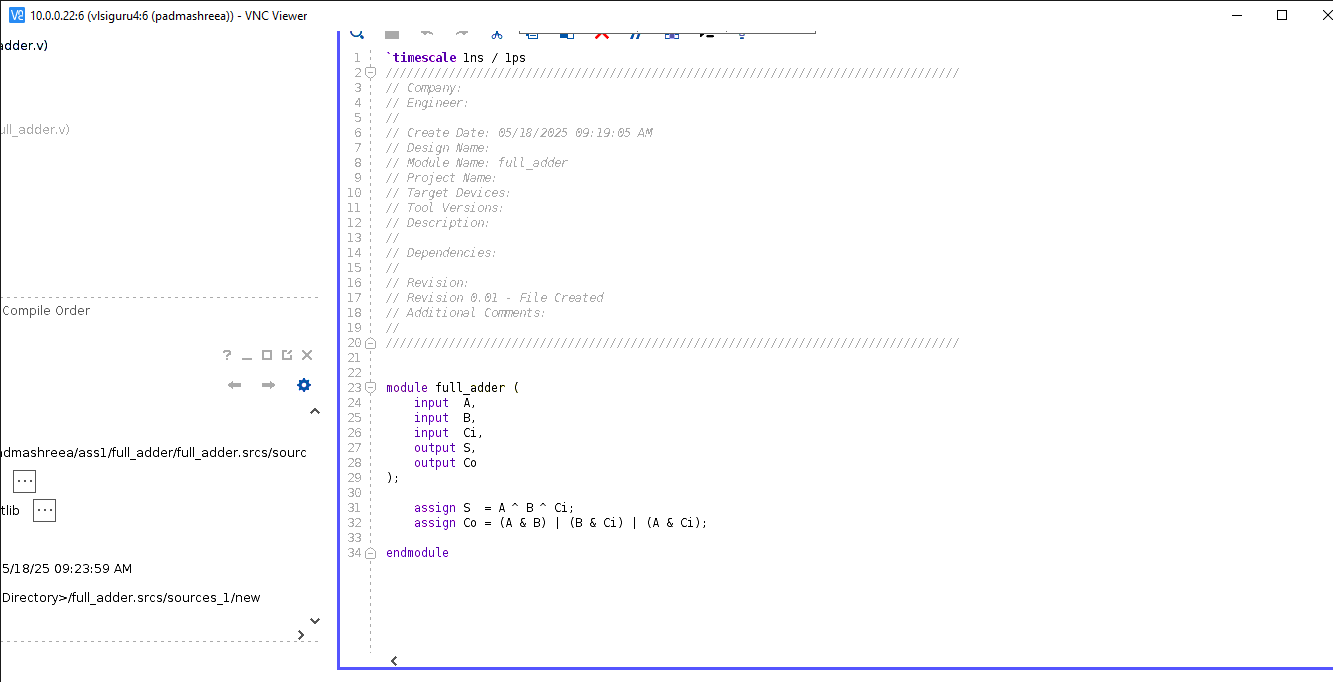
****

**Test circuit Elaborated design**

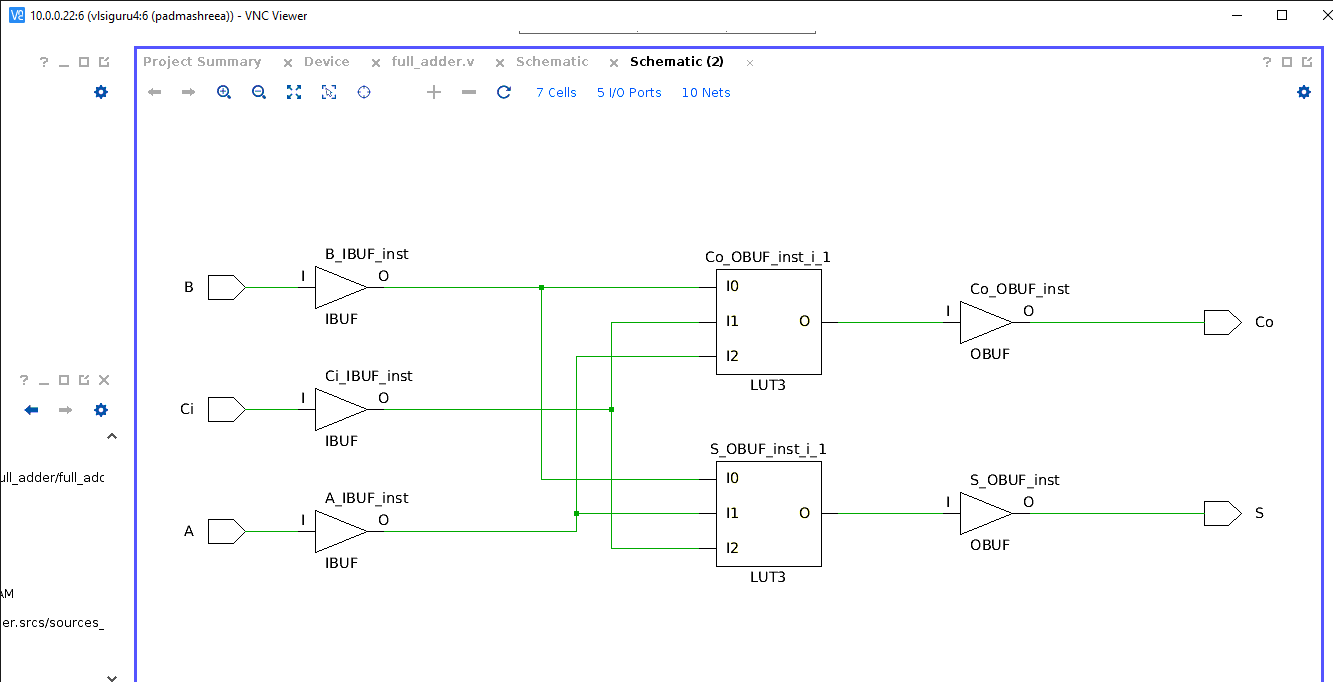
****

**Full Adder**

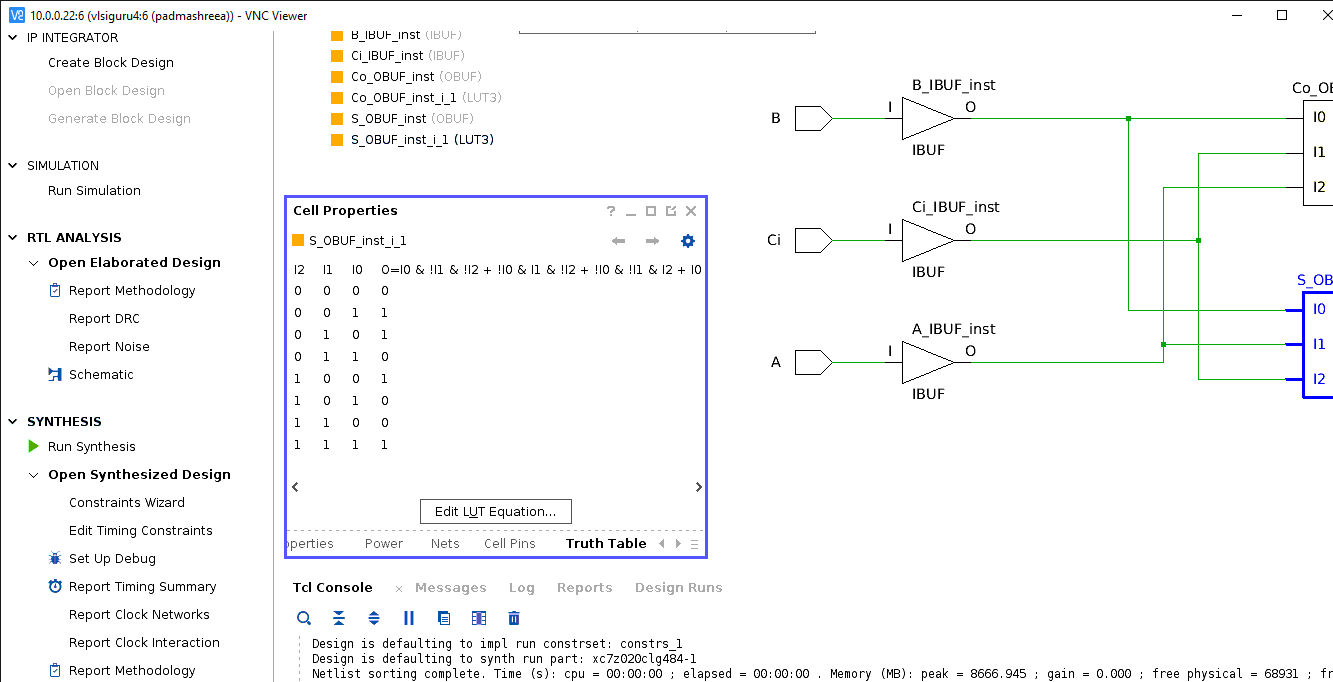
**RTL/Verilog code**

****

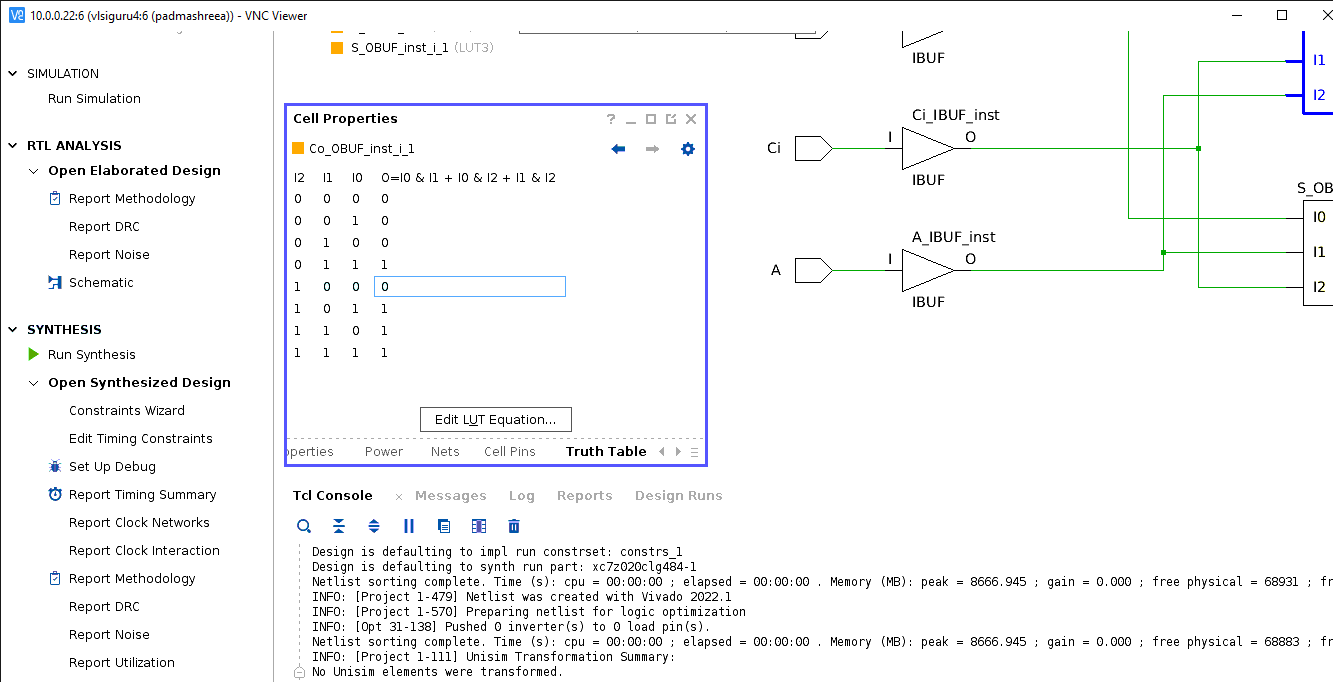
**Schematic diagram**

****

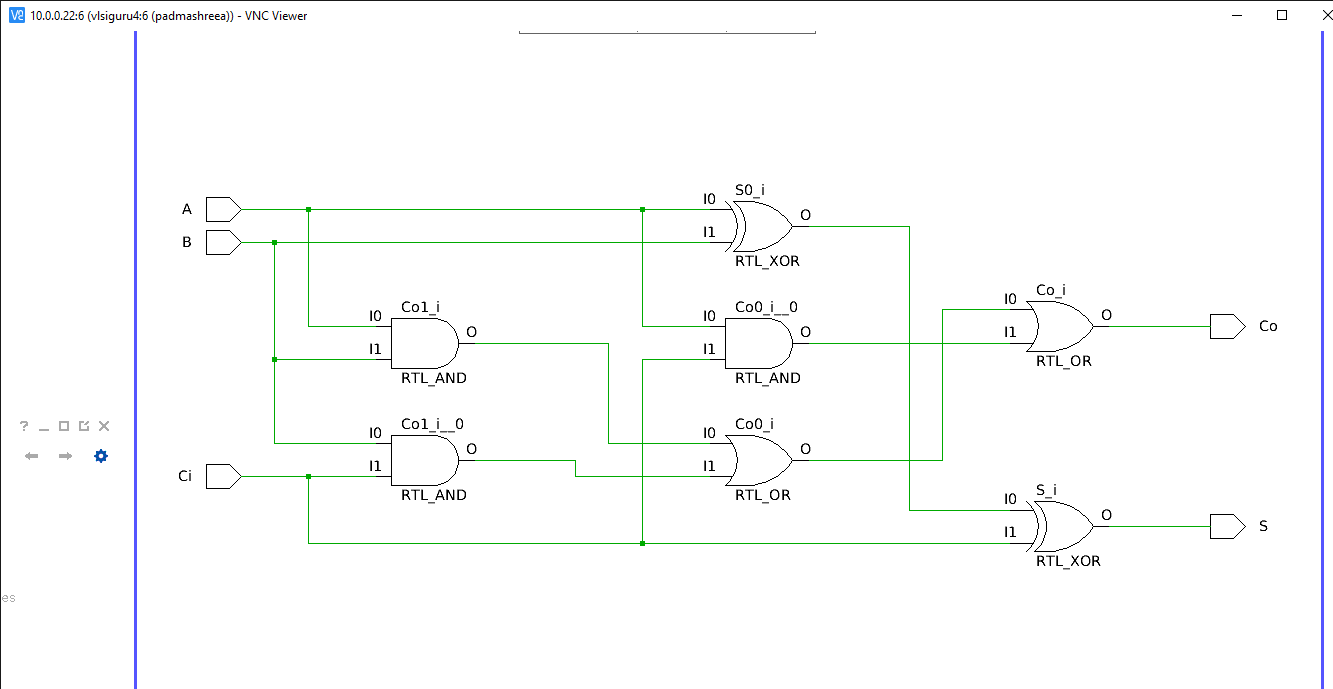
**Truth table for Sum**

****

**Truth table for carry**

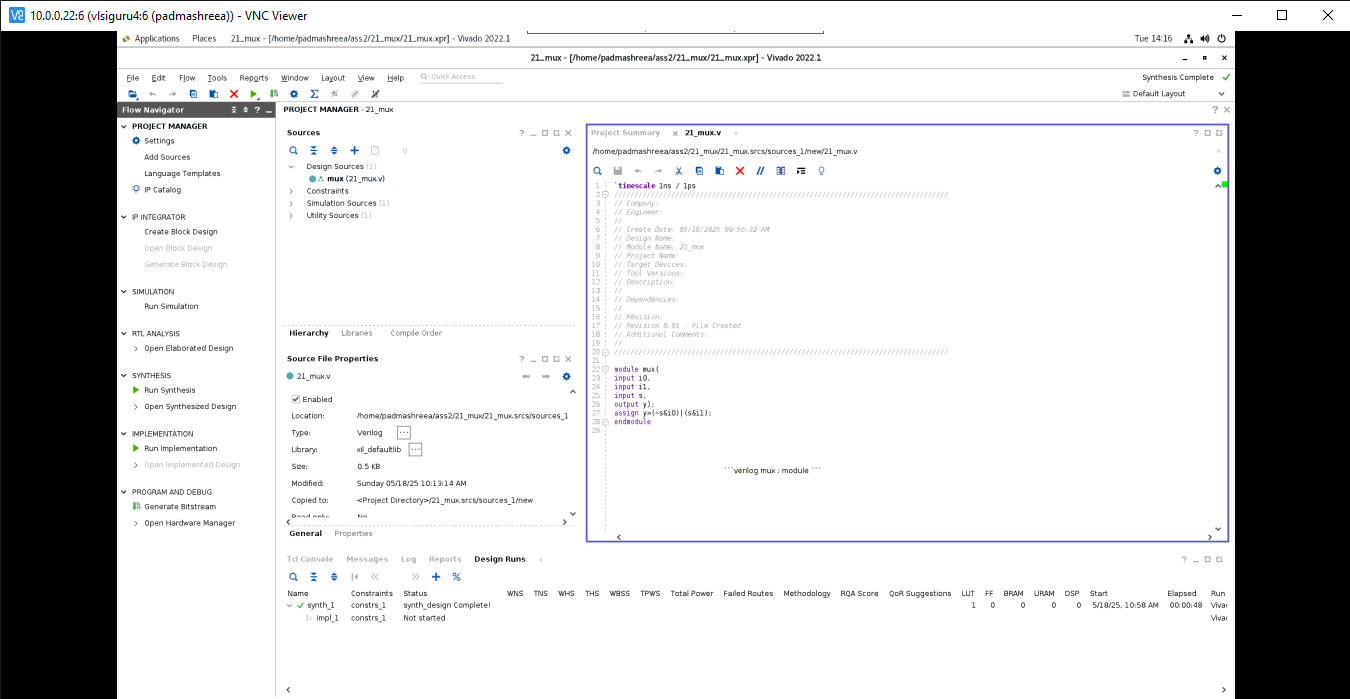
****

**Elaborated diagram**

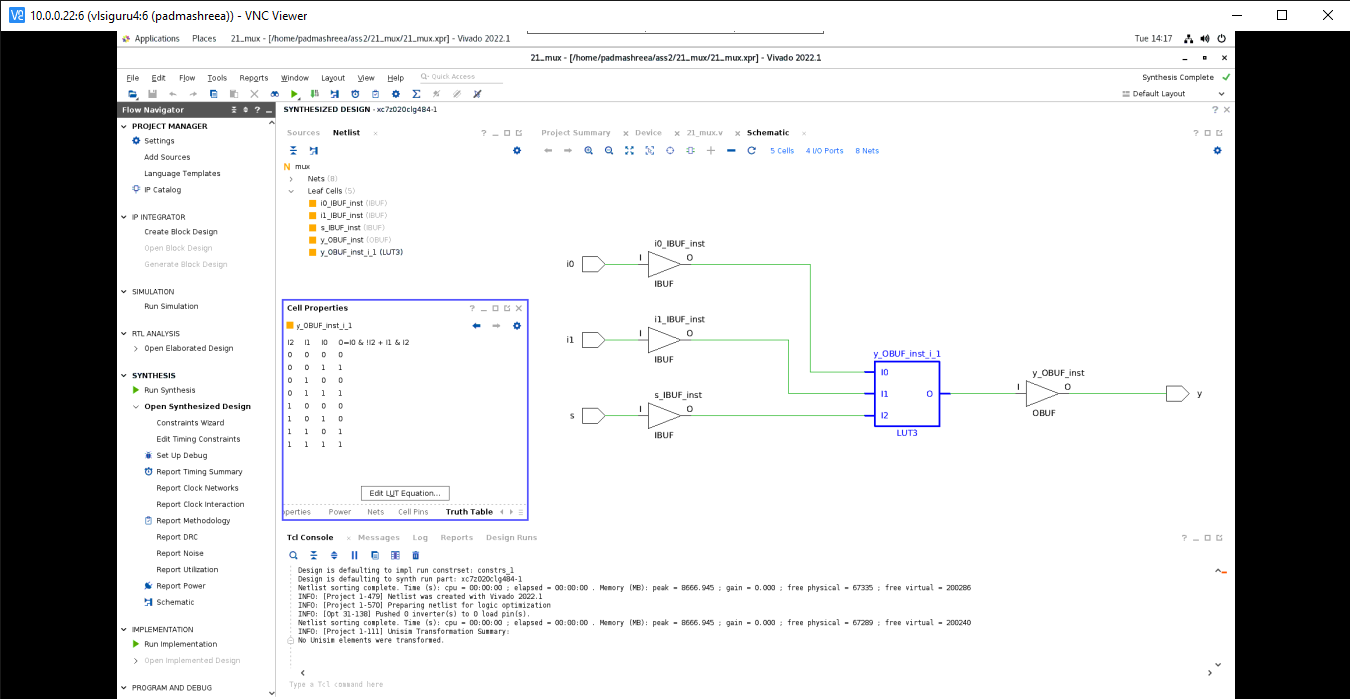
****

**2:1 Mux**

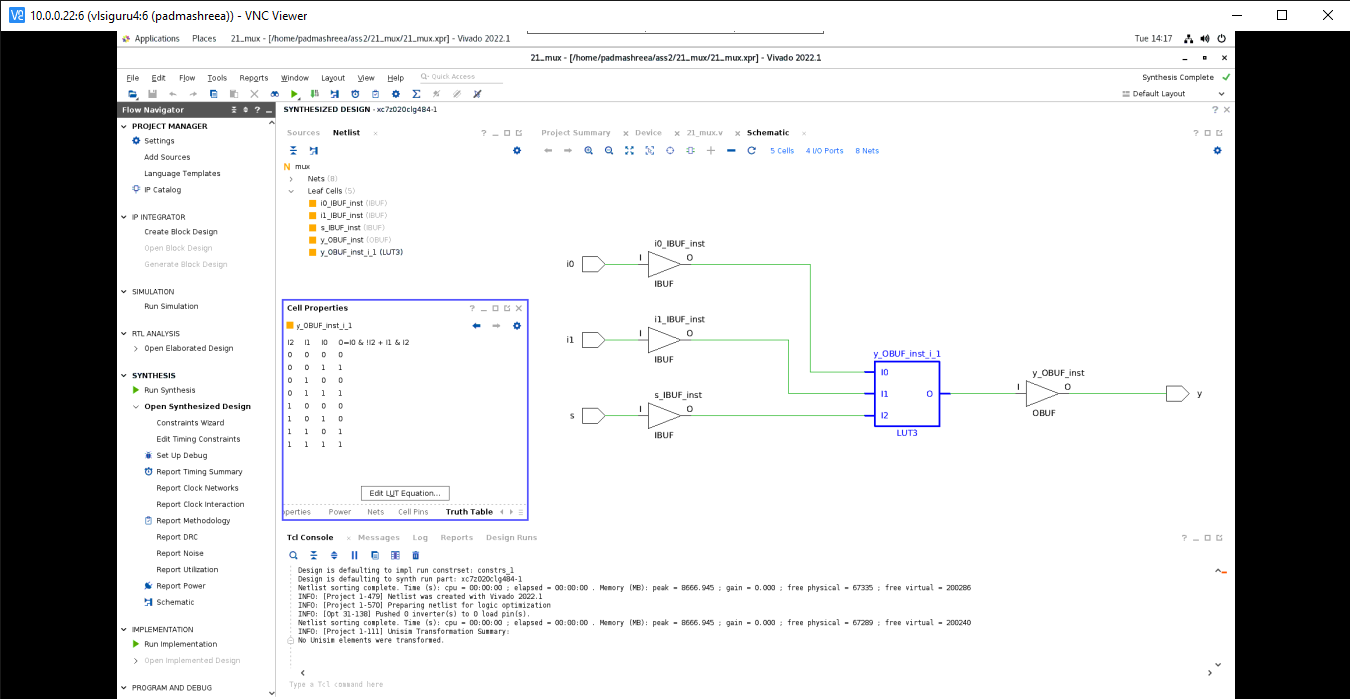
**RTL/Verilog code**

****

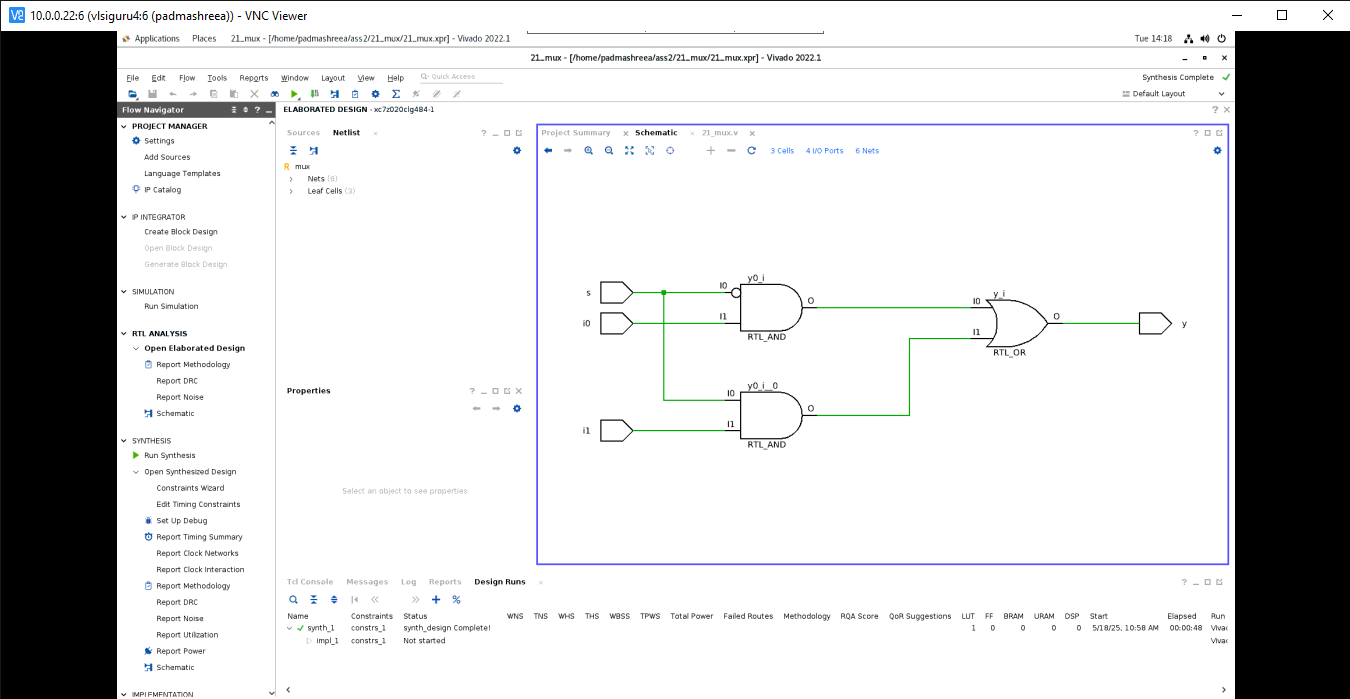
**Schematic diagram**

****

**Truth table**

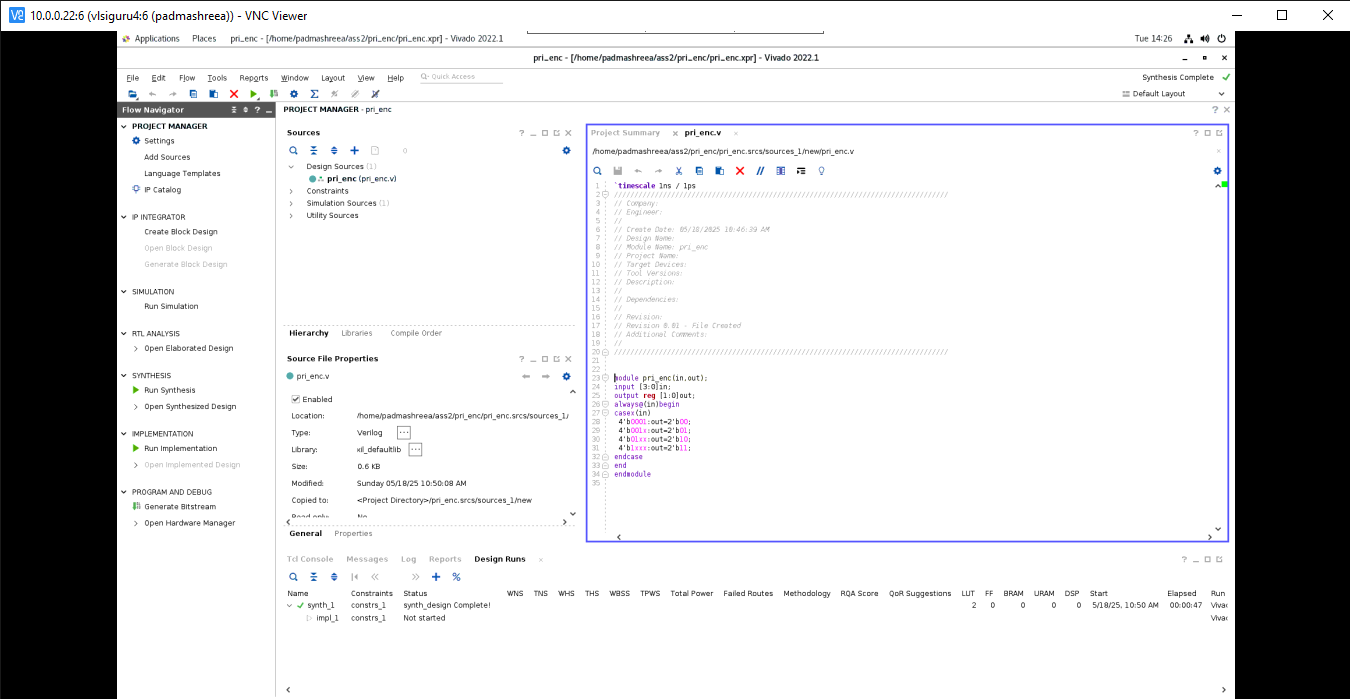
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**Elaborated diagram**

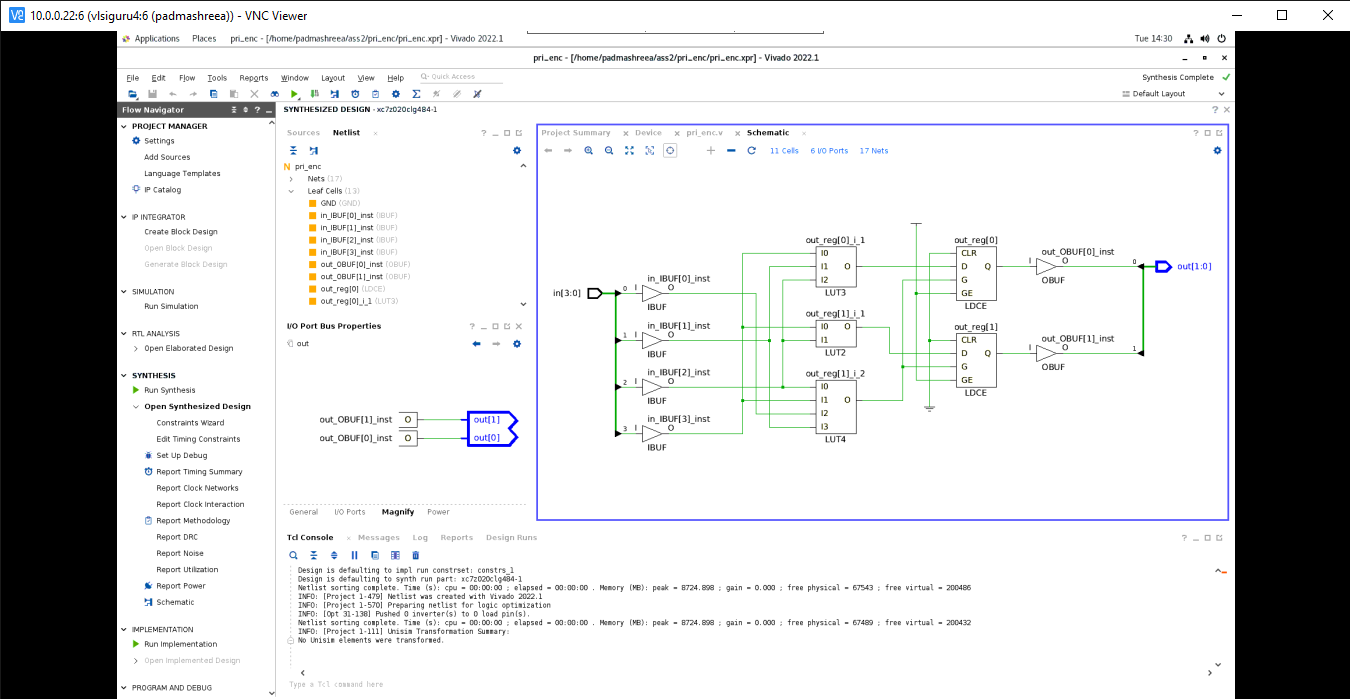
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**Priority Encoder**

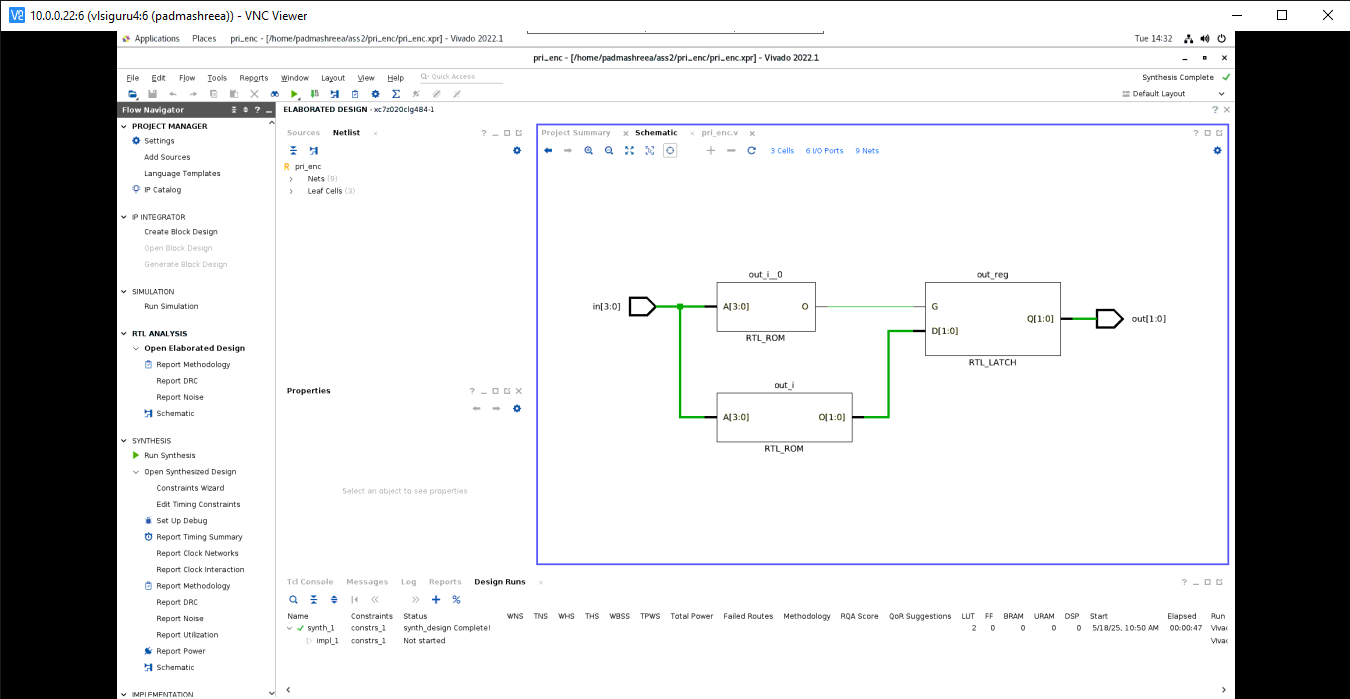
**RTL/Verilog code**

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**Schematic diagram**

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**Elaborated circuit**

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