AD-APARD32690-SL

Monday, June 30, 2025 4:54 PM

Quick Links

- MAX32690 datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/max32690.pdf
- AD-APARD32690-SL User Guide: AD-APARD32690-SL User Guide [Analog Devices Wiki] AD-APARD32690 schematic: 02-073637-01-c.pdf
- 32690 MSDK Peripheral Driver API: MAX32690 Peripheral Driver API: Main Page

USER LEDs

- schematic: <u>02-073637-01-c.pdf</u> LED1

 - o P2.1
- DS2
- LED2
- o index 1
- o P0.11
- D5
- LED3
 - o index 2 o P0.12 o D5

Processors

- Cortex-M4 (CM4)

 o 12 MHz
- o general purpose o with FPU RISC-V (RV32)

- o 32-bit
- coprocessor
 ultra-low-power
- o offload data processing

Timers and Clocks

- MAX32690 Diagrams
- - Simplified Block Diagram
 - **Electrical Characteristics** Clocking Scheme Diagram
- SYS_CLK is system clock
 SYS_TICK is system timer
- o clock vs. timer

Clock Source

Pick one of the following 7 as SYS_CLK (system clock)

- IPO
 Internal Primary Oscillator
 I20MHz
 - o ISO
 - Internal Secondary Oscillator 60 MHz
 - used for exiting power-on reset o IBRO Internal Baud Rate Oscillator
 - 7.3728 MHz
 - optimize active power consumption allow UART communications to meet 2% baud rate tolerance
 - o INRO
 - Internal Nanoring Oscillator
 8 kHz
 - ultra low power
 - o ERFO External RF Oscillator
 - external crystal required
 32 MHz
 - o ERTCO
 - 32.768 kHz
 - External RTC Oscillator
 RTC: Real-Time Clock
 - external crystal required ■ Y3 in schematic
 - CLKEXT
 - external clock (P0.23)
- does not have exposed connector for probing on APARD
 another name: ADIN1110_LINK_ST

 SYS_CLK is primary clock source for digital logic and peripherals

- Wakeup
 IBRO or IPO
- Clock Source in MSDK

 - Clock Source in MSDK

 MXC_TMR_APB_CLK = 0, // PCLK, peripheral clock, SYS_CLK/2

 MXC_TMR_EXT_CLK = 1, // external clock from P0.23

 MXC_TMR_EXT_CLK = 1, // external secondary oscillator, 60 MHz

 MXC_TMR_ISD_CLK = 3, // internal baud rate oscillator, 7.3728 MHz

 MXC_TMR_ISRD_CLK = 3, // external RF oscillator, 32 MHz

 MXC_TMR_ERTO_CLK = 5, // external RF oscillator, 32 MHz

 MXC_TMR_INRO_CLK = 6, // internal nanoring oscillator, 8 kHz

 MXC_TMR_INRO_CLK = 6, // internal nanoring oscillator, 8 kHz

 MXC_TMR_INRO_DIVS_CLK = 7, //(7.3728/8) = 0.9216 MHz

 O Why no IPO when IPO is part of the mux in Clocking Scheme Diagram?

 Paraltime (Lock)

RTC (Real-Time Clock)

- datasheet: MAX32690
 32-bit seconds register
 2^32 seconds ~= 136 years
- · provide 2 time-of-day alarms

 - 1 st alarm
 1 alarm from 1 second to 12 days
 can be used as a power-saving timer for low-power mode
 - 32-bit 1/4096 sub-second alarm
 tick resolution of 244us
- clock source
- 32.768 kHz crystal
 or external clock
- calibration
- o user software can compensate for minor variations in RTC enable SQWOUT alternate function to output RTC timing signal adjust RTC frequency through external hardware

Programmable Timers

32-Bit Timer / Counter / PWM (TMR, LPTMR)

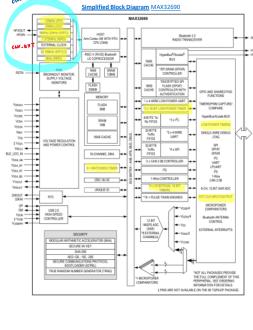
- general purpose

Electrical Characteristics MAX32690

поска					
SLOCKS Sellen Clack	_				
requency	firs_cux		120	MHz	
System Clack Period	fers,cux		18svs_c	85	
nternal Primary Dscillator (IPO)	feo		120	Mile	
nternal Secondary Seelfator (197)	fso		80	MHz	
nternal Baud Rate Dscillator (IERO)	Neo		7.3728	Mile	
nternal Nanoring Dscillator (INRO)	Neo.			HHe	
PARAMETER	SYMBOL	conprisons	MIN TYP MAX	UMTS	
Oxformal RTC Oscillator ERTCO)	Чентоо	STANE water crystal, C _L _{NTML} = 6pF, 5SF = 906C, C _S > 3pF, trystal power designation rating minimum 0.5µW, no minimal leaf opportunity.			
Osserna RF Oscillator Iraquency (ERF Q)	torro	32Mintrogenial, C _{L, NYAL} = 12pF, CSR's 500, C _S 3 TpF, withpressions aboliny scholing scho	12	Mes	
RTC Operating Current	Parc	All power modes, RTC enabled	0.3	- PAL	
ROC Power-Up Time	Sec. or		.263	1100	
External IPS Clock Injust Vaguercy	fixe_as_car	Q5_CLPEXT solected	20	Mile	
Oxformal System Clock Sput Frequency	fort, suc	EXT_CLK switched	80	Mrs	
Internal Low-Power Inner1 Clock Input Integration	fext_LPTMVI_ CLK	LPTMR1_CLK selected		Meg	
Internal Low-Power Inner2 Clock Input	fecturing.	LPTMR2_OLK selected P3-6		Mrs	

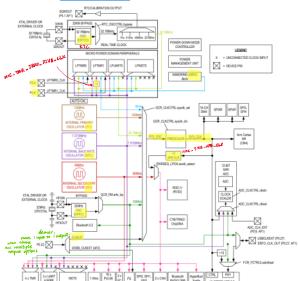


LOCKS				
lysteni Clack Tequency	fers_cux		120	MHz
System Clack Period	ters,cux		15ys_c LK	115
nternal Primary Dscillator (IPO)	feo		120	Mile
nternal Secondary Secillator (197)	160		60	MHz
nternal Baud Rate Decilator (IERO)	1seo		7.9728	Mile
nternal Nanoring Oscillator (INRCI)	feeto		8	HHe
PARAMETER	SYMBOL	covertions	MIN TYP MAX	UMITS
Oxformal RTC Oscillator ERTGO)	ferrico	329Hz waitch crystal, Cl., yrai, = 6pF., E.SR = 90kCl. C ₂ S 2pF. trystal power designation rating minimum 0.5uW. no enternal load objections.	32,768	Me
Cotemas RF Deciliator Vacquency (ERFQ)	tomo	32Miniz cryotei. C _{L, NYAL} = 12pF, CSR's 500. C _S 3 TpF, withperature aboving vidippin, solid tolerance addispon, crystal privar (dosponius relating intermediate). Tolera to the 550/22500 User (dosponius on carculating the load appendix.	п	Mes
RTC Operating Current	laro	All power modes, RTC enabled	0.3	- PAL
RDC Power-Lip Time	Sec. or		263	1100
External IPS Clock triput Vaguetrcy	feet_as_car	Q5_CLADKT solected	20	Mile
Oxformal System Clock Sput Frequency	fort, suc	EXT_CLK selected	80	MHz
Ixlemal Low-Power Inter1 Clock Input Integratory	fact untimet.	LPTMR1_CLK selected		Meg
Internal Lew Power Inver2 Clock fepal Inquency	fext_urrura_ CLK	LPTMR2_CLK selected P3-6		Mile



clocking schoune diagram

Clocking Scheme Diagram MAX32690



32-bit Timer Instances MAX32690

Table 4.	MAX32690	Timer	Instances

INSTANCE	REGISTER	SINGLE 32-BIT	DUAL 16-BIT	SINGLE 16-BIT	POWER MODE	CLOCK SOURCE						
	ACCESS NAME					PCLK	ISO	IBRO	INRO	ERTCO	LPTMR0_ CLK	LPTMR1
TMRO	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	Yes	No
LPTMR1*	TMR5	No	No	Yes	ACTIVE, SLEEP, LPM	No	No	Yes	Yes	Yes	No	Yes

WDT Timer Instances MAX32690

- adjust RTC frequency through external hardware

Programmable Timers 32-Bit Timer / Counter / PWM (TMR, LPTMR) • general purpose • 32-bit timers

- features 32-bit up/down auto reload
- programmable prescaler PWM
- capture & compare timer input, clock gating, capture timer output dual 16-bit timer
- interrupts
 six 32-bit timers
 operate in SLEEP, LPM, UPM modes

- ouerate in SLEEP, LPM, UPM mode
 Modes
 32-bit Timer Instances
 Watchdong Timer (WDT)
 compensate for electrical noise and EMI
 detects system unresnonsiveners.
- detects system unresponsiveness
 32-bit, free-running counter
 configurable prescaler
 must be periodically reset

- WDT timeout can trigger interrupt and system reset
 force the instruction pointer to a known good location
 WDT timer instances
 Pulse Train Engine (PT)

- periodic signals
 can read more from datasheet MAX32690

- ERTCO as clock source
- prescaler from 1 to 4096 support one-shot and continuous independent interrupt handler

Power Management

user-configurable system clock

Modes

ACTIVE Mode

- RV32: 256KB flash and 128KB SRAM8
 can execute from internal flash simultaneously
 all peripherals are on
 dynamic clocking disable peripherals not in use
 high performance while low-power consumption

 SLEEP Mode

- less power than ACTIVE mode wakes faster then LPM mode
- clocks can optionally be enabled
- CM4 & RV32 are asleep peripherals are on

- LOW POWER Mode (LPM)

 CM4, SRAM0 SRAM7 are in state retention
 RV32 can access several peripherals

- clocks

 IPO can optionally be powered down
 INRO is on IBRO, ERTCO, ISO and ERFO are optionally enabled

MICRO POWER M

- ICRO POWER Mode (UPM)

 CM4 & RV32 are state retained
 all non-MICRO Power downstrained
- all non-MICRO Power domain peripherals are state retained clocks
 - IPO, ISO, ERFO are powered down
- INRO is on
 IBRO, ERTCO are optionally enabled STANDRY Mode

- maintain system operation while keeping RTC
 CM4 & RV32 are state retained
- clocks
- RTC, wakeup timers, ERTCO optionally enabled
 INRO is on
- **BACKUP Mode**
- CM4 & RV32 are powered off
 all peripherals are powered down
- clocks
 ERTCO, RTC, wakeup timers are optionally enabled INRO is on IPO, ISO, IBRO, ERFO are powered down



WDT Timer Instances MAX32690

			CLOCK SOURCE					
INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE						
	100001011111111111111111111111111111111		PCLK	IBRO	INRO	ERTCO		
WDTO	WDTO	ACTIVE, SLEEP, LPM	Yes	Yes	No	No		
LPW0T0	WDT1	ACTIVE, SLEEP, LPM,	No	Yes	Yes	Yes		