AD-APARD32690-SL

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Quick Links

- MAX32690 datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/max32690.pdf
- AD-APARD32690-SL User Guide: AD-APARD32690-SL User Guide [Analog Devices Wiki]
- AD-APARD32690 schematic: 02-073637-01-c.pdf
- 32690 MSDK Peripheral Driver API: MAX32690 Peripheral Driver API: Main Page

Pins

USER LEDs

- schematic: 02-073637-01-c.pdf
- LED1
  - index 0
  - P2.1
  - DS2
- LED2
  - index 1
  - P0.11
  - D5
- LED3
  - index 2
  - P0.12
  - D5

Processors

- Cortex-M4 (CM4)
  - 12 MHz
  - general purpose
  - with FPU
- RISC-V (RV32)
  - 32-bit
  - coprocessor
  - ultra-low-power
  - offload data processing

Timers and Clocks

- MAX32690
- Diagrams
  - Simplified Block Diagram
  - Electrical Characteristics
  - Clocking Scheme Diagram
- **SYS_CLK** is system clock
- **SYS_TICK** is system timer
  - clock vs. timer

Clock Source

- Pick one of the following 7 as **SYS_CLK** (system clock)
  - **IPO**
    - Internal Primary Oscillator
    - 120MHz
  - **ISO**
    - Internal Secondary Oscillator
    - 60 MHz
    - used for exiting power-on reset
  - **IBRO**
    - Internal Baud Rate Oscillator
    - 7.3728 MHz
    - optimize active power consumption
    - allow UART communications to meet 2% baud rate tolerance
  - **INRO**
    - Internal Nanoring Oscillator
    - 8 kHz
    - ultra low power
  - **ERFO**
    - External RF Oscillator
      - external crystal required
    - 32 MHz
  - **ERTCO**
    - 32.768 kHz
    - External RTC Oscillator
      - RTC: Real-Time Clock
      - external crystal required
    - Y3 in schematic
  - **CLKEXT**
    - external clock (P0.23)
      - does not have exposed connector for probing on APARD
      - another name: ADIN1110_LINK_ST
- **SYS_CLK** is primary clock source for digital logic and peripherals
- Wakeup
  - IBRO or IPO
- Exit Power-on reset
  - ISO
- Clock Source in MSDK

```
MXC_TMR_APB_CLK = 0, // PCLK, peripheral clock, SYS_CLK/2
MXC_TMR_EXT_CLK = 1, // external clock from P0.23
MXC_TMR_ISO_CLK = 2, // internal secondary oscillator, 60 MHz
MXC_TMR_IBRO_CLK = 3, // Internal baud rate oscillator, 7.3728 MHz
MXC_TMR_ERFO_CLK = 4, // external RF oscillator, 32 MHz
MXC_TMR_ERTCO_CLK = 5, // external RTC oscillator, 32.768 kHz
MXC_TMR_INRO_CLK = 6, // internal nanoring oscillator, 8 kHz
MXC_TMR_IBRO_DIV8_CLK = 7, //(7.3728/8) = 0.9216 MHz
```

  - Why no IPO when IPO is part of the mux in Clocking Scheme Diagram?
  - External Low-power Timer (LPTMR0,1), what are they used for?

RTC (Real-Time Clock)

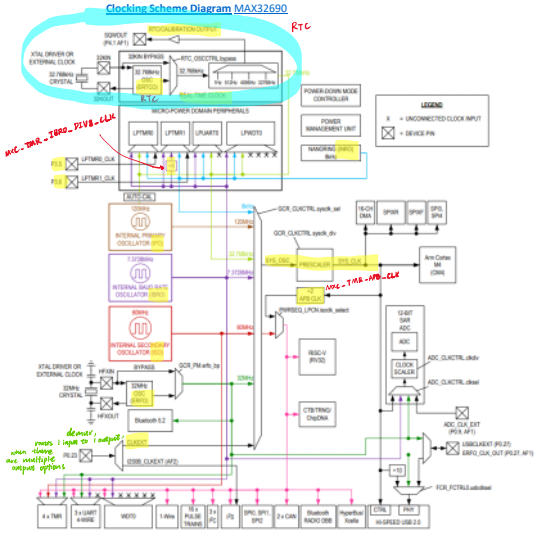
- datasheet: MAX32690
- real-time clock (RTC)
- 32-bit seconds register
  - 2^32 seconds ~= 136 years
- keep time of day in absolute seconds
- provide 2 independent **time-of-day alarms**
  - 1st alarm
    - can be programmed to any future time value from 1 second to 12 days
    - can be used as a power-saving timer for low-power mode when:
      - configured for long intervals
      - allow periodic wakeups to perform tasks
  - 2nd alarm
    - 32-bit 1/4096 sub-second alarm
    - tick resolution of 244us = 1/4096
  - both alarms could repeat
- clock source
  - 32.768 kHz crystal
  - or external clock
- calibration
  - user software can compensate for minor variations in RTC
  - enable SQWOUT alternate function to output RTC timing signal
  - adjust RTC frequency through external hardware
- some thoughts related to MAX32690 RTC

Programmable Timers

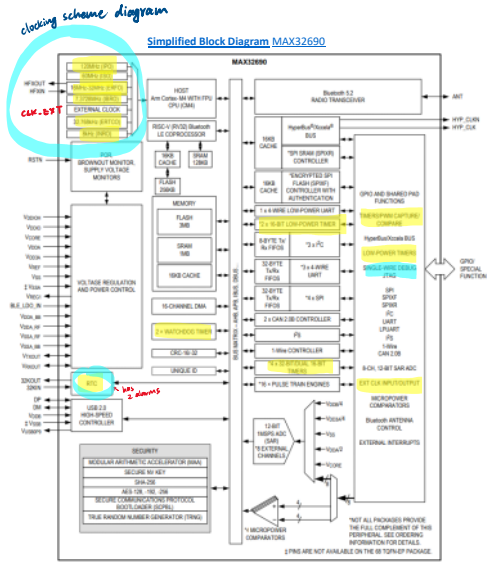
32-Bit Timer / Counter / PWM (TMR, LPTMR)

- general purpose
- 32-bit timers
- for timing, capture/compare, PWM generation
  - timer modes
- features
  - 32-bit up/down auto reload
  - programmable prescaler
  - PWM
  - capture & compare

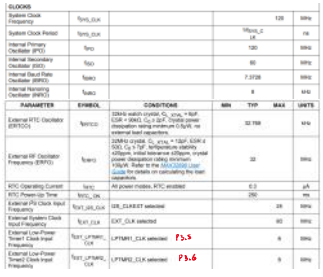
Clocking Scheme Diagram MAX32690



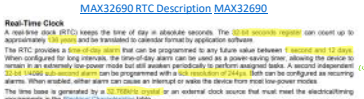
Simplified Block Diagram MAX32690

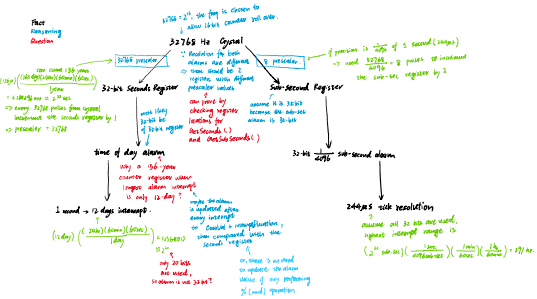


Electrical Characteristics MAX32690



MAX32690 RTC Description MAX32690





32-bit Timer Instances MAX32690

Table 4. MAX32690 Timer Instances

INSTANCE	REGISTER ACCESS NAME	SINGLE 32-BIT	DUAL 16-BIT	SINGLE 16-BIT	POWER MODE	CLOCK SOURCE						
						PCLK	ISO	IBRO	INRO	ERTCO	LPTMRx_CLK	LPTMRy_CLK
TMR0	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	Yes	No

- for timing, capture/compare, PWM generation
  - timer modes
- features
  - 32-bit up/down auto reload
  - programmable prescaler
  - PWM
  - capture & compare
  - timer input, clock gating, capture
  - timer output
  - dual 16-bit timer
  - interrupts
- six 32-bit timers
  - operate in SLEEP, LPM, UPM modes
    - Modes
- 32-bit Timer Instances table

Watchdog Timer (WDT)
- compensate for electrical noise and EMI
- detects system unresponsiveness
- 32-bit, free-running counter
  - configurable prescaler
- must be periodically reset
- WDT timeout can trigger interrupt and system reset
  - force the instruction pointer to a known good location
- WDT timer instances

Pulse Train Engine (PT)
- periodic signals
- can read more from datasheet MAX32690

Wakeup Timer
- ERTCO as clock source
- prescaler from 1 to 4096
- support one-shot and continuous
- independent interrupt handler

TMR1	TMR1	Yes	Yes	No	SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	Yes	No
LPTMR1*	TMR5	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	No	Yes

*Available as an internal timer only on the 68-pin TQFN-EP package. There is no external connection to this timer on the 68-pin TQFN-EP package.

WDT Timer Instances MAX32690

Table 5. MAX32690 Watchdog Timer Instances

INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE	CLOCK SOURCE			
			PCLK	ISRO	INRO	ERTCO
WDT0	WDT0	ACTIVE, SLEEP, LPM	Yes	Yes	No	No
LPWDT0	WDT1	ACTIVE, SLEEP, LPM, UPM	No	Yes	Yes	Yes

Power Management
- user-configurable system clock

Modes
ACTIVE Mode
- both CM4 and RV32 can execute software
  - CM4: all system SRAM
  - RV32: 256KB flash and 128KB SRAM8
  - can execute from internal flash simultaneously
- all peripherals are on
- dynamic clocking disable peripherals not in use
- high performance while low-power consumption

SLEEP Mode
- less power than ACTIVE mode
- wakes faster then LPM mode
- clocks can optionally be enabled
- CM4 & RV32 are asleep
- peripherals are on
- clocks
  - all oscillators are available

LOW POWER Mode (LPM)
- CM4, SRAM0 - SRAM7 are in state retention
- RV32 can access several peripherals
- clocks
  - IPO can optionally be powered down
  - INRO is on
  - IBRO, ERTCO, ISO and ERFO are optionally enabled

MICRO POWER Mode (UPM)
- CM4 & RV32 are state retained
- all non-MICRO Power domain peripherals are state retained
- clocks
  - IPO, ISO, ERFO are powered down
  - INRO is on
  - IBRO, ERTCO are optionally enabled

STANDBY Mode
- maintain system operation while keeping RTC
- CM4 & RV32 are state retained
- clocks
  - RTC, wakeup timers, ERTCO optionally enabled
  - INRO is on

BACKUP Mode
- CM4 & RV32 are powered off
- all peripherals are powered down
- clocks
  - ERTCO, RTC, wakeup timers are optionally enabled
  - INRO is on
  - IPO, ISO, IBRO, ERFO are powered down