HDL-Lab Introduction

Alex Schönberger

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TU Darmstadt
Integrated Electronic Systems Lab
Prof. Dr.-Ing. Klaus Hofmann
Merckstr. 25, 64283 Darmstadt, Germany

Organisational

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- Supported time period:
  - 03.08 – 14.08.2015, 9:00 am – 5:30 pm
- Room: S3|06/67
- Supervisor: Alex Schönberger,
  - Alex-Schoenberger@ies.tu-darmstadt.de
  - room: S3|06/345b
- HiWi: Xiang Ding

Goal

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- Design, implemention, synthesis and test of a MIPS-I specified processor core on FPGA

- Description language: VHDL
- Target technology: Virtex5 (Xilinx)
- Frequency constraint: 50 – 200 MHz

- Core constraints:
  - Pipeline stages: 2 – 6
  - Following subcomponents are mandatory:
    - ALU, datapath, controlpath

Evaluation

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- Simulative tests
  - **ModelSIM** for simulation
  - reference signal waves created on a core with 4-staged pipeline (generic memory and FPGA memory)

- Synthesis test
  - **Synplify** for pre-synthesis (netlist generation)
  - **Xilinx ISE** for bitfile generation

Minimum requirements to pass

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- Simulative execution of reference program on a core, netlist is synthesized for at least 50 MHz
- Successfully generated bitfile tested with on reference FPGA-testbench
- Report (12 pages)
  - Short introduction (1 page)
  - Design
    - ALU (1 page)
    - datapath (3 pages) – block diagram mandatory
    - controlpath (4 pages)
  - Evaluation (1 page)
  - Synthesis (1 page) – timing and resource reports mandatory
  - Conclusion(1 page)

Bonus

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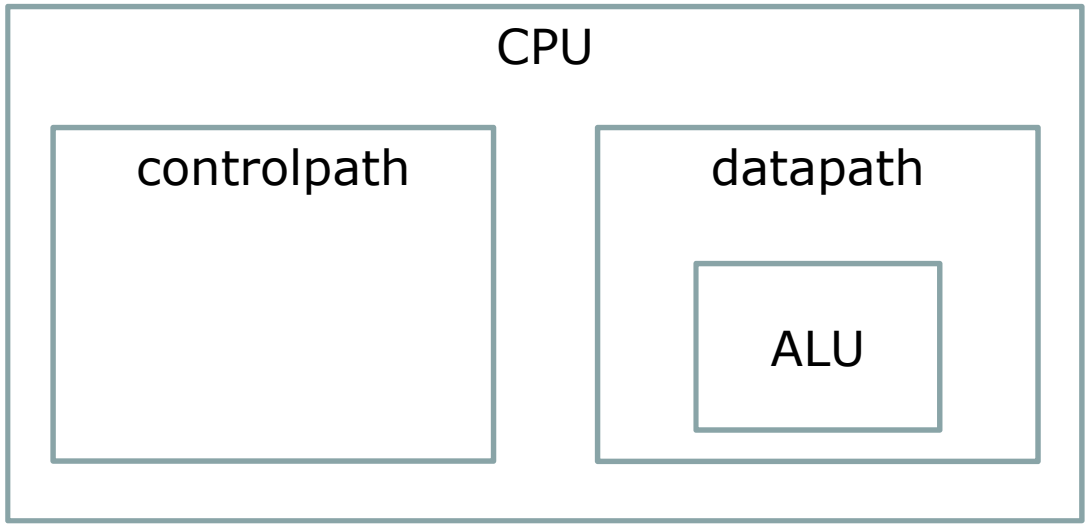
- 1. Full implementation of MIPS-I specification **or**
- 2. Design is synthesizedable for more than 200 MHz (+0.3 grade improvement)
- 1. and 2. together, tested with openJPEG algorithm and reference FPGA-testbench

Milestones

- 1 (after 4 days): ALU is implemented and tested
- 2 (after 8 days): The core executes reference programs as expected
- 3 (after 10 days): FPGA-Testbench is synthesized and works without errors.



Deadlines

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- 13.08.2015, 0:00 am: ALU with simulative testbench
- 14.08.2015, 5:30 pm: designs for grade improvements
- 24.08.2015, 8:00 am: Final deadline

Support

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- 3.08 – 14.08.2015
  - 9:00 am – 5:30 pm: Xiang Ding
  - 2 pm – 4 pm: Alex Schönberger
  - 4.08, 13.08-14.08: 11 am: Alex Schönberger
- Support list:
  - Group number, kind of question (organisational, tool usage, script usage, VHDL syntax, design structure, synthesis reports, FPGA availability …)

Project files

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- complete scr-, test- and report-folders
  - each source file should contain revision history
    - when (03.08.2015), who (Alex Schönberger), did what (created)
  - source files without revision history are going to be excluded from grading process

Starting point (I)

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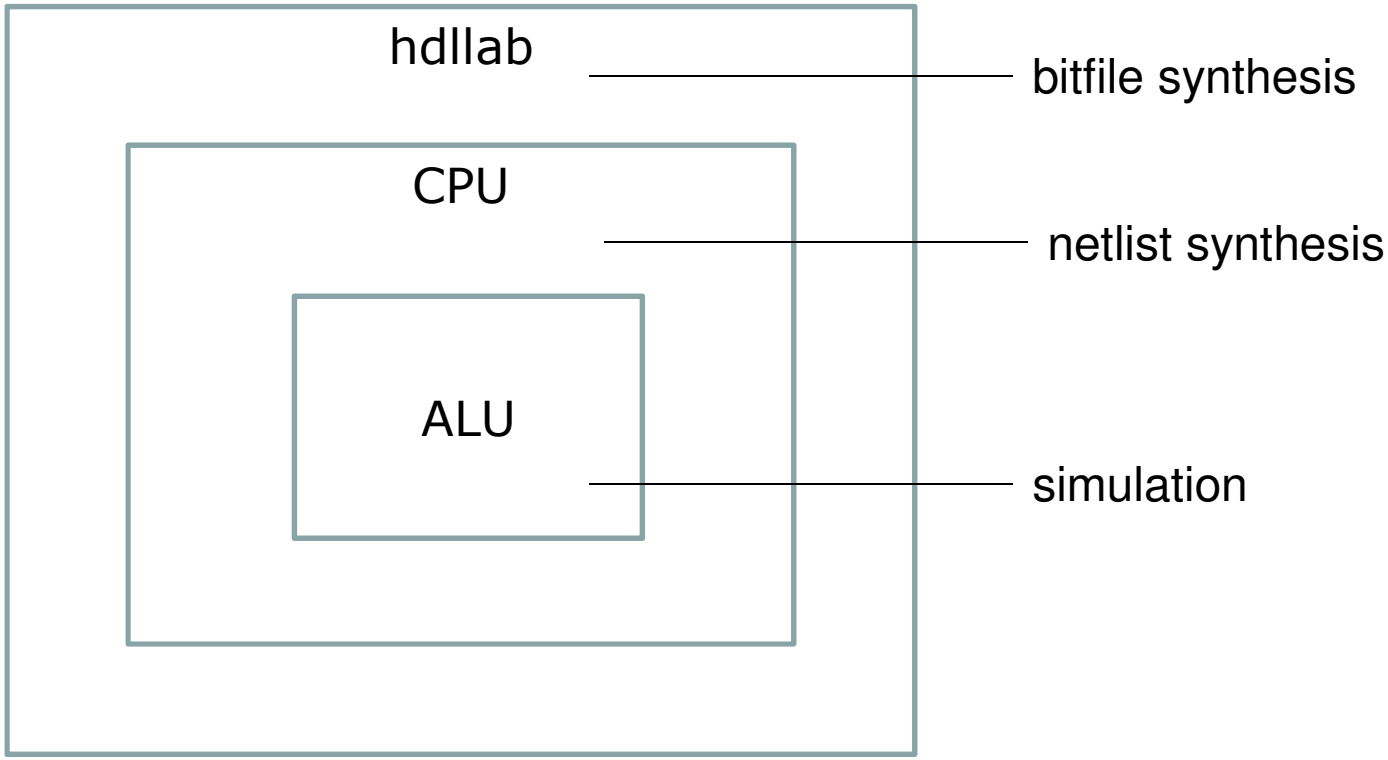
- hdllab
  - doc
    - MIPS I specification
    - ModelSIM User Quide
    - Synplify User Quide
    - Xilinx (ML507) User Quide
  - src
    - vhdl
      - mips_instruction_set.vhd, cpu_pack.vhd
      - cpu.vhd, cpu_control.vhd, cpu_datapath.vhd, alu.vhd
    - c
      - counter.c
  - test
    - vhdl
      - tb_alu.vhd, tb_cpu.vhd, tb_hdllab.vhd, hdllab.vhd, uart.vhd, memory.vhd

Testbenches



Starting point (II)

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- sim
  - counter
  - build
  - openJPEG
- syn
  - hdllab
- scripts
  - memory.tcl
- conf
  - alu.conf, cpu.conf, cpu_full.conf, lab.conf

first steps

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```
hdllab/test/scripts/create_env.sh

module load modelsim
sim cpu lc
sim cpu



sim alu lc
```

simulation

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- `module load modelsim` - load ModelSIM
- `sim cpu lc` - compile sources
- `sim cpu` - start simulation

- `sim <testname> lc` - compile sources
- `sim <testname>` - start GUI

- **ModelSIM** command line
  - `open_counter` - opens reference signal waves

netlist synthesis

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- `module load synplify`
- `syn lab lc`
- (optional) `syn lab`

bitfile synthesis

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- `cd hdllab/test/syn/hdllab`
- `module load xilinx/14.5`
- `ise &`