MIPS 1 in VHDL

HDL Lab - SS 2015

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1 Introduction

In the HDL Lab is a practical exercise of a hdl language implementation. This semester the task is the implementation of a MIPS I microcontroller in vhdl. A requirement to this laboratory is the lecture HDL: Verilog and VHDL from Prof. Dr.-Ing. Klaus Hofmann.
The MIPS instruction set is a reduced instruction set computer (RISC). There are available references for 32 and 64-bit with many revisions. This microcontroller reference is often used as an hdl first project.

1.1 Task

Each group shall design, implement, synthesise and test a MIPS-I specified processor core on FPGA. The hardware description langugage is VHDL and the target technology is a Virtex5 from Xilinx. The synthesised microcontroller must be able to run at 50 MHz with a desirable frequency of 200 MHz. The microcontroller must use a pipeline of a minimum of 2 and maximum of 6 stages. The following subcomponents are mandatory: ALU, datapath and controlpath.

2 Design

This chapter describes the design of a MIPS 1 microcontroller. The microcontroller design is shown Abbildung 2.1.

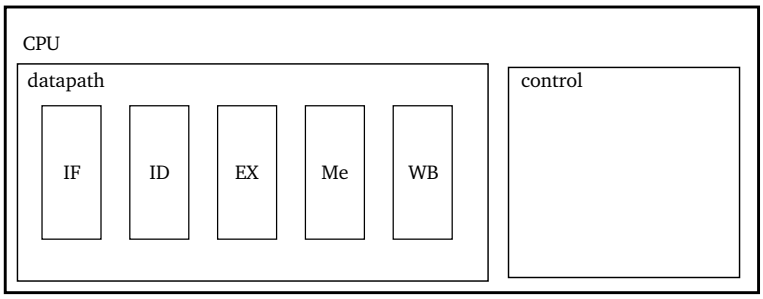

Abbildung 2.1: CPU overview

The CPU is divided in a control and a datapath blocks. In the datapath there is the pipeline made of five blocks:

- IF: Instruction fetch
- ID: Instruction decode
- Ex: Execution
- Me: Memory stage
- WB: Writeback

The CPU interacts with two external memories and has also a clock and a reset input.

2.1 ALU

2.2 Datapath

2.3 Controlpath

3 Evaluation

4 Synthesis

5 Conclusion