MIPS 1 in VHDL

HDL Lab - SS 2015

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1 Introduction

In the HDL Lab is a practical exercise of a hdl language implementation. This semester the task is the implementation of a MIPS I microcontroller in vhdl. A requirement to this laboratory is the lecture HDL: Verilog and VHDL from Prof. Dr.-Ing. Klaus Hofmann.
The MIPS instruction set is a reduced instruction set computer (RISC). There are available references for 32 and 64-bit with many revisions. This microcontroller reference is often used as an hdl first project.

1.1 Task

The objective is to design, implement, synthesise and test a MIPS-I specified processor core on FPGA. The hardware description langugage is VHDL and the target technology is a Virtex5 from Xilinx. The synthesised microcontroller must be able to run at 50 MHz with a desirable frequency of 200 MHz. The microcontroller must use a pipeline of a minimum of 2 and maximum of 6 stages. The following subcomponents are mandatory: ALU, datapath and controlpath.

2 Design

This chapter describes the design of a MIPS 1 microcontroller. A microcontroller consists mostly of a processor core, memory and programmable inputs/outputs peripherals. This design implementation focus only on the processor core design.

This laboratory requires a microcontroller structure of at least a CPU containing a controlpath, datapath and an ALU. The created design uses this base with a 5-staged pipeline. The CPU interacts with two external memories and has also a clock and a reset input. All of which are considered external to this design. The CPU is divided in two base components: a control and a datapath block, as shown in Figure 2.1.

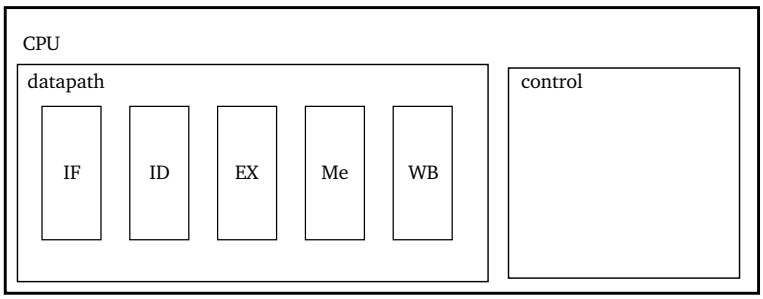

Figure 2.1: CPU overview

In the datapath there is the pipeline made of five blocks:

- IF: Instruction fetch
- ID: Instruction decode
- Ex: Execution
- Me: Memory stage
- WB: Writeback

The following sections describe the central component ALU and the two base components: datapath and controlpath.

2.1 ALU

2.2 Datapath

This chapter describes the datapath and its internal elements. The datapath is the component that connects the pipeline components within itself as well as with cpu inputs and outputs and the controlpath.

This MIPS implementation works with a 5 stage pipeline in order to achieve a fast clock. The datapath consists of instruction fetch, instructino decode, execution, memory stage and writeback. The datapath controls the information flow from one pipeline stage to the next with registers. These writing process occurs on the positive edge of the clock when the pipeline stage input from the controlpath allows it. That is, the registers forwards information synchronously.

2.3 Controlpath

3 Evaluation

4 Synthesis

5 Conclusion