राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान (रा.इ.सू.प्रौ.सं)

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय, भारत सरकार

Ministry of Electronics & Information Technology (MeitY), Govt. of India

रा.इ.सू.प्रौ.सं NIELIT

Certificate No.: NIELIT/NOI/OL/B67/25192

प्रमाणपत्र
CERTIFICATE

नाम **Name**	:	**PALAK VERMA**
माता का नाम **Mother's Name**	:	**BABITA VERMA**
पिता का नाम **Father's Name**	:	**RAJEEV VERMA**
रजिस्ट्रेशन संख्या **Registration No.**	:	**NIELIT/NOI/OL/B67/25192**

This is to certify that the above mentioned candidate has successfully completed program Internship Program on VLSI Design flow (RTL to GDS-II) of 06 Weeks / 90 hour(s) duration from 15.07.2025 to 25.08.2025 conducted by National Institute of Electronics and Information Technology (NIELIT), CoE Noida in Online mode with S grade.

Curriculum of the Course

Overview of VLSI Design Flow , Hardware Modeling, Introduction to Verilog using Icarus Verilog, RTL Synthesis with YOSYS tool, Static Timing Analysis using Open STA, Basic Concepts for Physical Design, Floor planning, Clock Tree Synthesis, Routing , Layout Design using Magic Tool.

श्रेणियों का आख्यान GRADE LEGENDS	80% and above	70% to <80%	60% to <70%	50% to <60%
	एस S	ए A	बी B	सी C

Digitally signed by DHARMENDRA KUMAR MISHRA (1)
Date:Thu Aug 28 10:51:18 IST 2025

Program Coordinator **Director**

Issued Date: 26.08.2025

Issued by
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