King Mongkut's University of Technology Thonburi
Faculty of Engineering, Department of Computer Engineering
CPE 223 Computer Architecture

PROBLEM SESSION 4: Hardware Description Language

1. Write a Verilog module for a branch predictor that has the following characteristics:
   - The module has 2 unsigned 32-bit registers. One is for the number of times branchesare taken, and another is for the number of time branch not taken.
   - The module will receive inputs:
     a. Clock(if necessary)
     b. Reset: if the reset is 1, then the module should reset all of its internal register values to 0.
     c. Branch Taken: If this is equal to 1, it indicates that the branch has been taken.
     d. Branch Not Taken: If this is equal to 1, it indicates that the branch has not been taken.
     e. You can assume that Branch Taken and Branch Not Taken will not be 1 at the same time.

   - The module will give the outputs:
     a. Branch Prediction. For example, you may have one wire, and if that wire is 1, then the prediction is branch will be taken; otherwise, the branch will not be taken.

   - The module will have the following mechanics:
     a. Upon receiving the input of the branch taken, the internal register would add 1 to the register number of the time branch taken. The same applies to the input of the branch not taken, input too, where it would be stored in another register.
     b. Branch Prediction should be based on those two registers and on which one is greater than the other. For Example if the number of times branches taken is greater than the number of times branches not taken, then the prediction should be branch will be taken.

2. Write a testbench that could demonstrate the given characteristics.

3. Create a report that briefly describes the output signal, along with briefly explanation of the module behavior.

Submission

Submit the source code, including both module code and testbench along with report into LEB2. Be sure to comment(explain) your code.

This is the problem session for the group of 2-3 students.