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ECE 4250: VLSI

Introduction to Layout and Simulation

During this lab, we designed hardware implementations of 5 simple circuit components. Green represents n-diffusion substrate, blue and purple represents metal wire contact, brown represents p-diffusion substrate, and red is polysilicon. The verification for the logic used for the hardware implementations is included in *Addendum*.

Our team faced challenges in setting up the necessary Docker container and magic software to complete the laboratory exercise; additionally, one member modeled the layout in the wrong tech file. Nevertheless, our finished layouts are depicted in *Figure 1*.

Figure 1: ACT Hardware Representations of Logic Gates

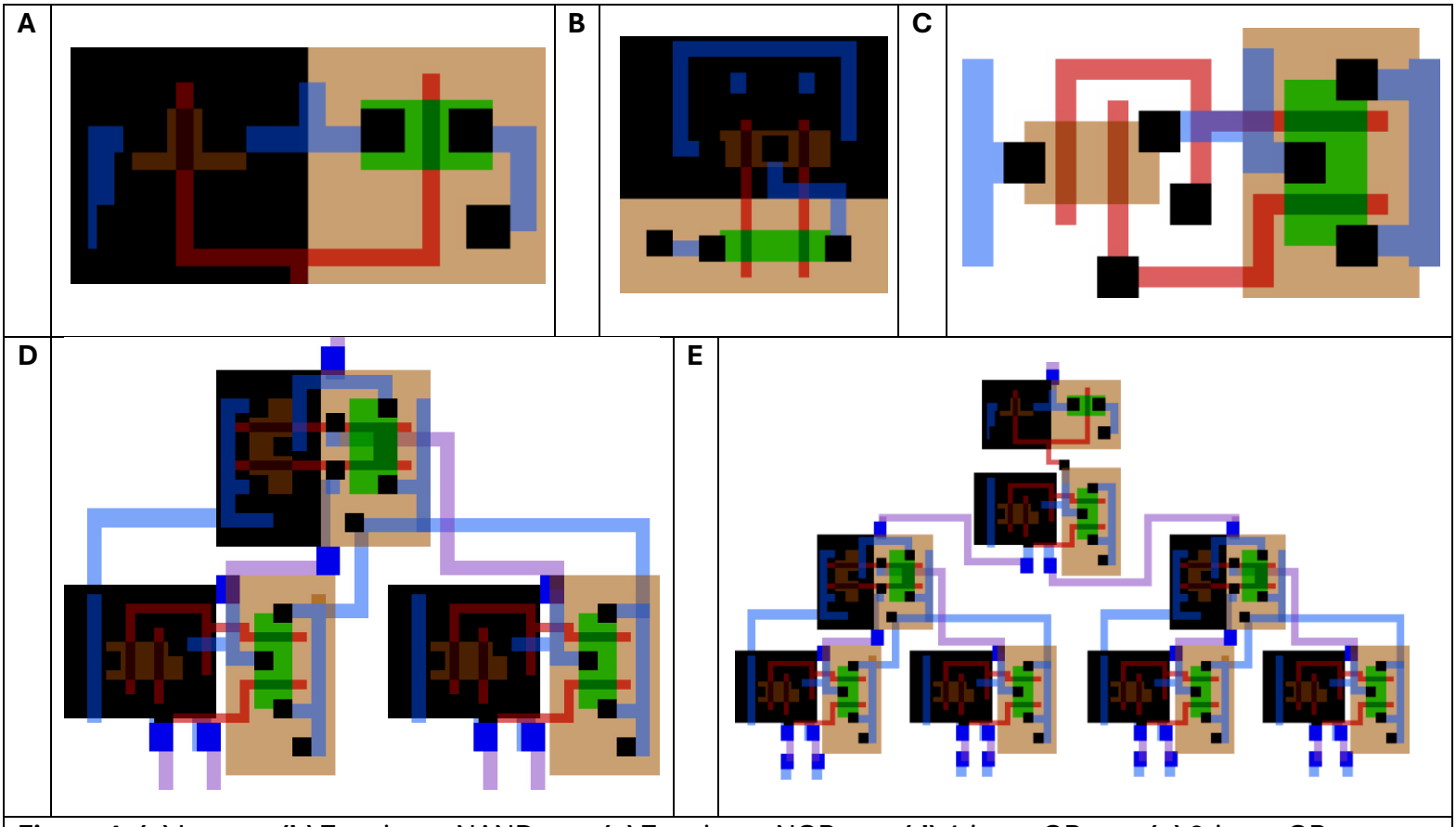

Figure 1: (a) Inverter **(b)** Two-input NAND gate **(c)** Two-input NOR gate **(d)** 4-input OR gate **(e)** 8-input OR gate.

Part III. Simulation Results

The simulation results for the assigned gates (Fig. 1a-e) were mostly as expected. The simulation of the inverter (Fig. 1a) provided expected results; the output was high when the input was low, and vice versa. The simulation of the two-input NAND gate (Fig. 1b) provided results as expected for the most part. However, when b = 1 and a – 0, the signal was pulled slightly lower than V_{dd}. We suspect this is due to the accumulation of charge between capacitors or leakage current in the transistors. The simulation for the

4-input NOR (Fig. 1d) gate provided the expected output. With a small variation both when pulling the out signal to low, and a small dip in the middle. This might be from interference when two input signals change in opposite directions simultaneously. The 8 input OR gate was similar to the 4 input OR gate.

Lambda^2 values of each gate:

Inverter	27 * 54 = 1458
NAND	37 * 59 = 2183
NOR	42 * 57 = 2394
4 Input OR	92 * 125 = 11500
8 Input OR	162 * 262 = 42444