RISC-V on FPGA in 90 minutes

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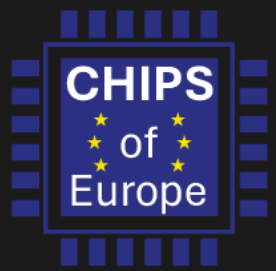

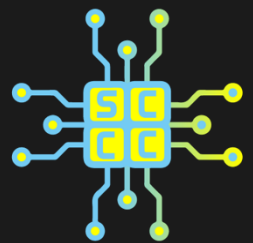

Background; Intro to Digital Design

- 240+ students, 9 credits (hp), 2nd year
- From: What is a gate / Why do we do Digital?
- To: Build a RISC-V Core in an FPGA!
- Historically, most lab hours spent on:
  - Debugging rats-nests
  - Understanding FPGA tools

Challenge

- Spend lab time on actual course content
- Enable off-site labs / BYOC
- Ease of use & Zero install
- Enable tool use during examination

Solution

- All tools via Web
- No back-end, run locally in Browser
- Compile tools to WebAssembly
- Integrate using browser-local Storage

Integrated tools

- Front end: Web converted version of IceStudio
- Synthesis: Yosys
- PnR: nextpnr
- FPGA programming: openFPGALoader
- Simulator: verilator
- Waveform display: surfer
- Compile & run in Browser: Emscripten

Let’s Do It!

https://github.com/PalePrime/single_cycle