HPC LAB - Matrix Addition CUDA

Name: Paleti Krishnasai Roll No: CED18l039

Programming Environment: CUDA (collab)

Problem: Matrix Addition

Hardware Configuration:

PU NAME: Intel(R) Core(TM) i5-8300H CPU @ 2.30GHz

Number of Sockets: 1 Cores per Socket: 4 Threads per core: 2 L1d cache: 128 KiB L1i cache: 128 KiB L2 cache: 1 MiB L3 cache: 8 MiB

| paleti@paleti-L | enovo-idea _l | oad-330-15I | CH:~\$ likwi | d-topology | | | | |
|---|--|---|--------------|---|---|--|--|--|
| | Intel(R) Core(TM) 15-8300H CPU @ 2.30GHz Intel Coffeelake processor 10 | | | | | | | |
| Hardware Thread Topology | | | | | | | | |
| ************************************** | t: 4 | **** | **** | ***** | ****** | | | |
| HWThread 0 1 2 3 4 5 6 7 | Thread 0 0 0 0 1 1 1 | Core 0 1 2 3 0 1 2 | | Socket 0 0 0 0 0 0 0 | Available * * * * * * * * * * | | | |
| Socket 0: | | 0 4 1 5 2 (| 5 3 7) | | | | | |
| ************************************** | | | | | | | | |
| Level: Size: Cache groups: | | 2 kB 0 4) (1 ! | 5)(26) | | | | | |
| Level: Size: Cache groups: Level: Size: Cache groups: | 3 8 | 56 kB 0 4) (1 ! | | | | | | |
| NUMA Topology | | | | | | | | |
| NUMA domains: | | | | | | | | |
| Domain: Processors: Distances: Free memory: Total memory: | 1) 3: | 0 1 2 3 4 5 546.2 MB 331.84 MB | 5 6 7) | | | | | |

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| Graphical Topology | | | | | | |
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CUDA code:

```
//Mat Add
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#include <stdio.h>
#include <stdlib.h>
#include<stdlib.h>
#include<time.h>
#include<math.h>
#include<unistd.h>
//#define Threads 2
#define n size 100000
__global__ void mul(float *a, float *b, float *c) {
int index=threadIdx.x+blockIdx.x*blockDim.x;
c[index] = a[index] *b[index];
void random init(float a[], int ch)
  srand(time(NULL));
 if(ch==0)
      for(int i=0;i<n size;i++)</pre>
      {
          a[i] = ((float) rand() / (float) (RAND MAX)) * 5.0;
  }
  else
  {
      for(int i=0;i<n size;i++)</pre>
            a[i] = (i+1);
      }
  }
int main() {
float a[n_size], b[n_size],c[n_size];
cudaEvent t start, end;
// host copies of variables a, b & c
float *d a, *d b, *d c;
// device copies of variables a, b & c
```

```
int size = n size*sizeof(float);
// Allocate space for device copies of a, b, c
cudaMalloc((void **)&d a, size);
cudaMalloc((void **)&d b, size);
cudaMalloc((void **)&d_c, size);
// Create Event for time
cudaEventCreate(&start);
cudaEventCreate(&end);
// Setup input values
random init(a,0);
random init(b,0);
// Copy inputs to device
cudaMemcpy(d a, &a, size, cudaMemcpyHostToDevice);
cudaMemcpy(d b, &b, size, cudaMemcpyHostToDevice);
int Thread[]=\{1, 2, 4, 6, 8, 10, 12, 16, 20, 32, 64, 128, 150\};
int thread arr size=13;
for(int i=0;i<thread arr size;i++)</pre>
        sleep(1);
      int Threads=Thread[i];
      cudaEventRecord(start);
      // Launch add() kernel on GPU
      mul<<<n size/Threads, Threads>>>(d_a, d_b, d_c);
      cudaEventRecord(end);
      cudaEventSynchronize(end);
      float time = 0;
      cudaEventElapsedTime(&time, start, end);
      // Copy result back to host
      cudaError err = cudaMemcpy(&c, d c, size, cudaMemcpyDeviceToHost);
      if(err!=cudaSuccess) {
          printf("CUDA error copying to Host: %s\n",
cudaGetErrorString(err));
      }
          int flag=0;
      for(int i=0;i<n size;i++)</pre>
      {    //printf("Result[%d]=%f\n",i+1,c[i]);
          if(c[i]!=(a[i]*b[i]))
              flag=1;
          break;
```

```
}
     if(flag==0)
      {
          printf("Program Executed as Expected\n");
          printf("Time Taken by the program for %d
Threads=%f\n", Threads, time);
          //printf("%f\n",time);
     }
     else
     {
          printf("Vector Addition hasnt been done properly, Mismatch in
Values!!!\n");
      }
}
// Cleanup
cudaFree(d a);
cudaFree(d_b);
cudaFree(d c);
return 0;
}
```

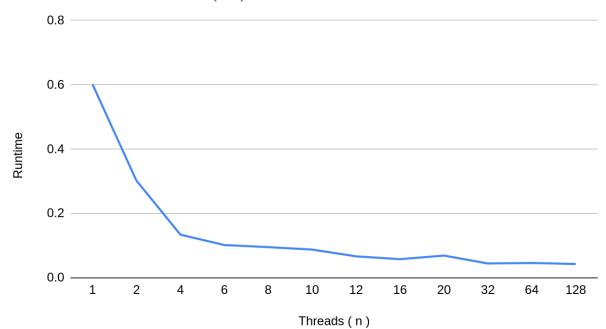
Observations:

The function add() is executed for an array of size 'N' on GPU for "N/T" times for 'T' Threads.

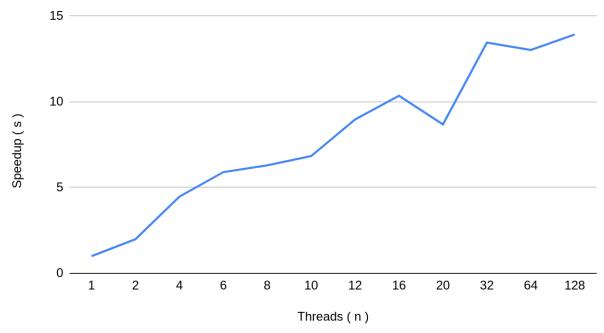
| Blocks | Threads (n) | Runtime | Speedup (s) | Parallelization Fraction |
|--------|---------------|----------|-------------|--------------------------|
| N | 1 | 0.60192 | 1 | |
| N/2 | 2 | 0.302368 | 1.990686845 | 0.9953216374 |
| N/4 | 4 | 0.13456 | 4.473246136 | 1.03526493 |
| N/6 | 6 | 0.101984 | 5.902102291 | 0.9966826156 |
| N/8 | 8 | 0.095584 | 6.297288249 | 0.9613731298 |
| N/10 | 10 | 0.088032 | 6.837513631 | 0.948608896 |
| N/12 | 12 | 0.067072 | 8.974236641 | 0.9693489923 |
| N/16 | 16 | 0.058112 | 10.35792952 | 0.9636859826 |
| N/20 | 20 | 0.069312 | 8.684210526 | 0.9314194577 |
| N/32 | 32 | 0.044736 | 13.45493562 | 0.9555384061 |
| N/64 | 64 | 0.046208 | 13.02631579 | 0.9378868046 |
| N/128 | 128 | 0.0432 | 13.93333333 | 0.9355385601 |

Graphical Inference:

Runtime vs. Threads (n)



Speedup(s) vs. Threads(n)



Inference:

From the Graph, it is observed that the speedup increases steadily in an up and down manner till 16 threads, and the highest Speedup is for 128 threads.

Runtime Decreases drastically from 1 to 4 threads and steadily decreases from then on till 128, with a minor rise at threads = 20.