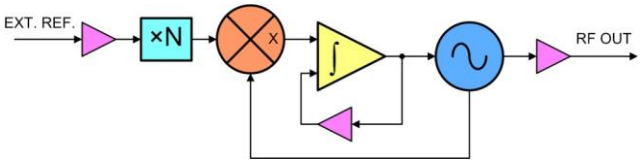
# Model PLCRO: Phase-Locked Ceramic Resonator Oscillator

## Features

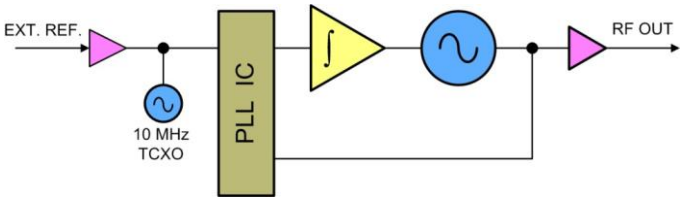
- Output Frequencies from 0.5 to 7 GHz
- Input Reference:
  - Internal TCXO Reference
  - External Reference
- Very Low Phase Noise
- +5.0 VDC Operation/Low Power Design
- Full Industrial Temp. Range -45°C to +85°C
- Low Cost


## Block Diagram

### Analog PLL




### Digital PLL




## Description

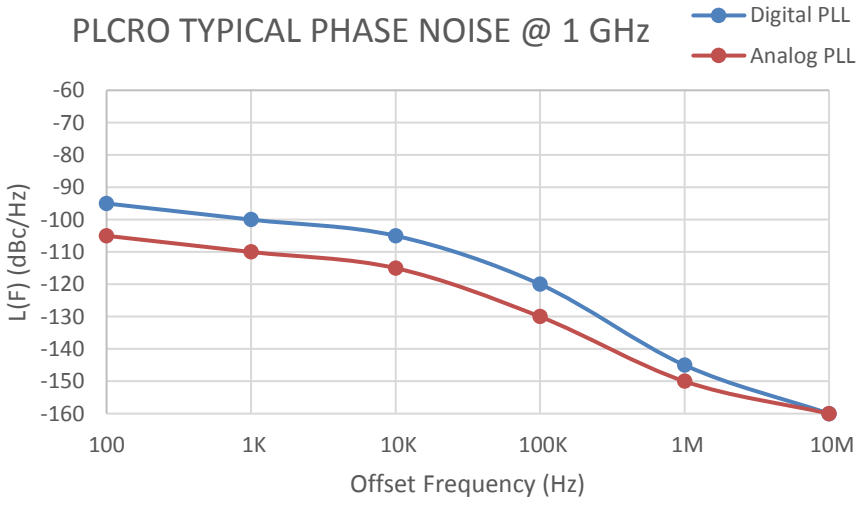
Our PLCRO line features a high-Q Ceramic Resonating Oscillator with either an Analog or Digital Sampling Phase Detector technique to establish a Phase Locked Loop (PLL).

The Analog PLL configuration is used to establish the best possible spectral quality. However, this configuration requires the output frequency to be an integer factor of the input frequency.

The Digital PLL configuration trades the Analog PLL's spectral quality for a wider range of output frequencies.

## PLCRO Key Specifications

| | |
|---|---|
| Output Frequency: | 0.5 – 7 GHz |
| Spurious: | -70 dBc |
| Harmonics (typ.): | -40 dBc |
| Output Power (min.): | +13 dBm |
| Output Power Variation: | ±3 dB |
| External Reference: | 1 – 200 MHz |
| Internal Reference: | ±0.5 PPM |
| Alarm: | Open Collector/TTL |
| Power Requirements: | +5.0 VDC @ 250 mA |
| Temp. Range: | -10°C to +70°C |

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