

COL-215

Hardware Assignment - 2 Report

Shreeraj Jambhale 2023CS50048	Pallav Kamad 2023CS51067
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1 Build Seven Segment Decoder

1.1 Aim

The aim is to design and implement a VHDL module that decodes a 4-bit input from the Basys 3 board switches into signals to control a 7-segment display, accounting for the board's active-low anode and cathode pins.

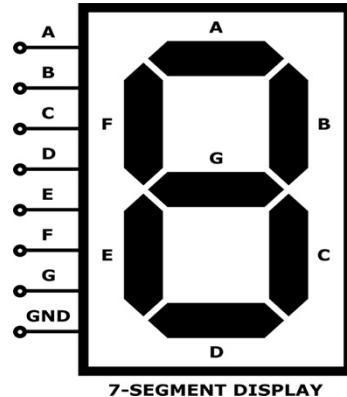
1.2 Approach

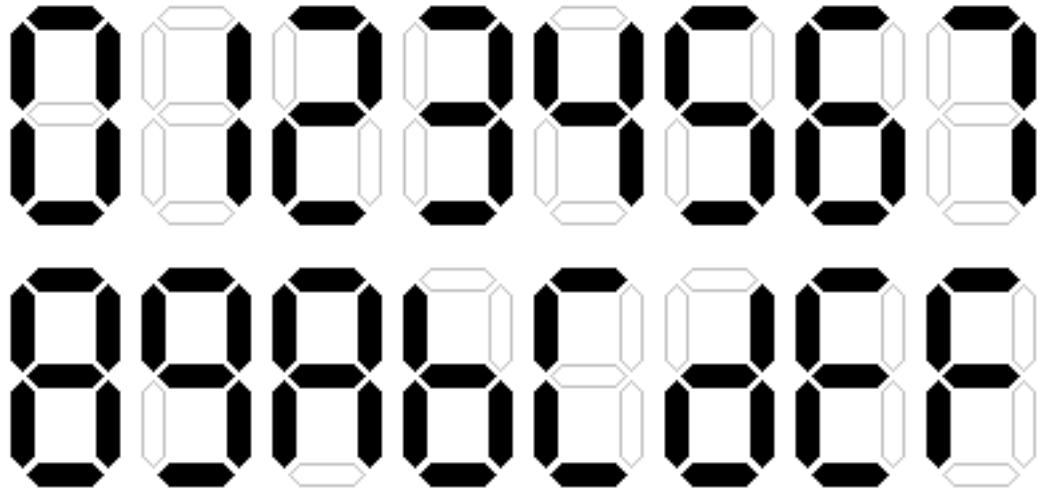
The approach involves creating a truth table with 4-bit inputs and 7-segment display outputs, followed by using Karnaugh maps (K-maps) to minimize the Boolean expressions for each segment control signal. These minimized expressions are implemented in VHDL using basic logic gates to decode the input binary number into signals that drive the active-low cathode and anode pins of the 7-segment display on the Basys 3 board. The result is an optimized combinational circuit that correctly displays the input number.

1.3 Truth Table and Logic Simplification

1.3.1 Boolean Table

Digit	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1
A	1	1	1	0	1	1	1
b	0	0	1	1	1	1	1
C	1	0	0	1	1	1	0
d	0	1	1	1	1	0	1
E	1	0	0	1	1	1	1
F	1	0	0	0	1	1	1





1.3.2 K-maps

AB/CD	00	01	10	11
00	0	1	0	0
01	1	0	0	0
10	0	0	0	1
11	0	1	0	0

$$a = A'B'C'D + A'BC'D' + ABC'D + AB'CD$$

segment a

AB/CD	00	01	10	11
00	0	0	0	0
01	0	1	1	0
10	0	0	0	1
11	1	0	1	1

$$b = A'BC'D + ABC'D' + BCD' + ACD$$

segment b

AB/CD	00	01	10	11
00	0	0	1	0
01	0	0	0	0
10	0	0	0	0
11	1	0	1	1

$$c = A'B'CD' + ABC'D' + ABC$$

segment c

AB/CD	00	01	10	11
00	0	1	0	0
01	1	0	0	1
10	0	0	1	0
11	0	0	0	1

$$d = A'B'CD' + A'BCD' + BCD + AB'CD'$$

segment d

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AB/CD	00	01	10	11
00	0	1	0	1
01	1	1	0	1
10	0	1	0	0
11	0	0	0	0

$$e = A'D + A'BC' + B'C'D$$

segment e

AB/CD	00	01	10	11
00	0	1	1	1
01	0	0	0	1
10	0	0	0	0
11	1	0	1	1

$$f = A'B'C + A'B'D + A'CD + ABC'D$$

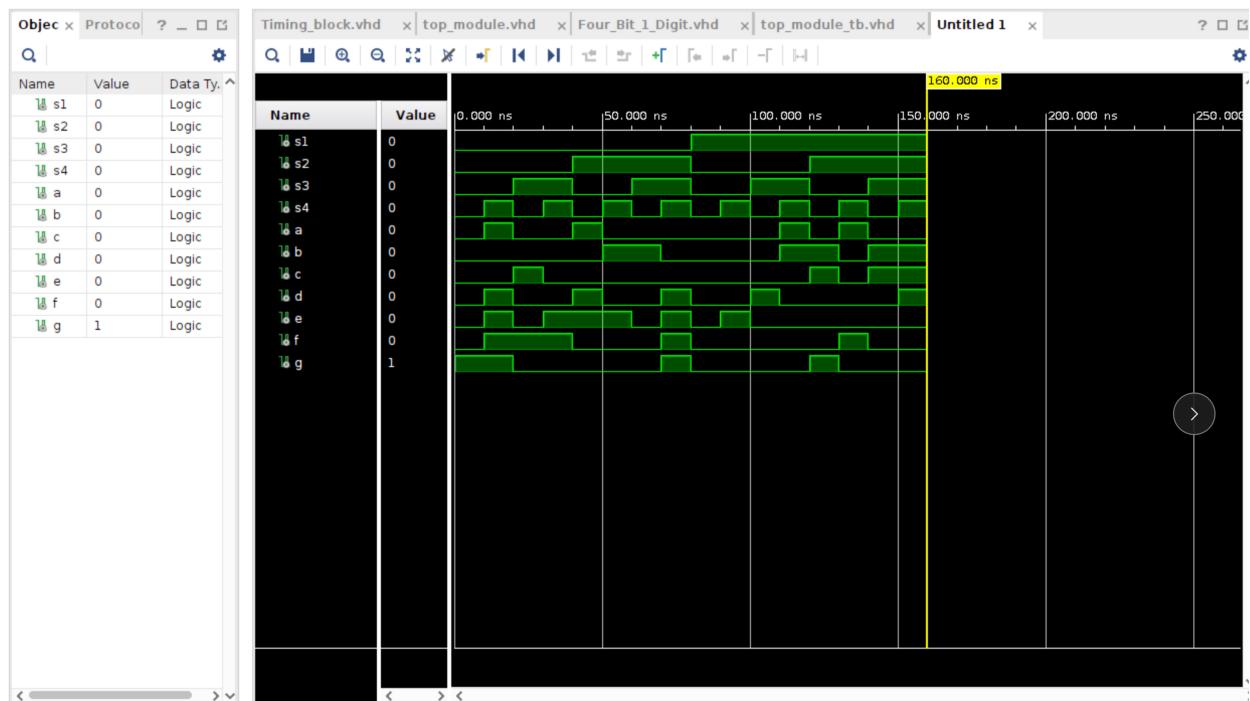
segment f

AB/CD	00	01	10	11
00	1	1	0	0
01	0	0	0	1
10	0	0	0	0
11	0	0	0	0

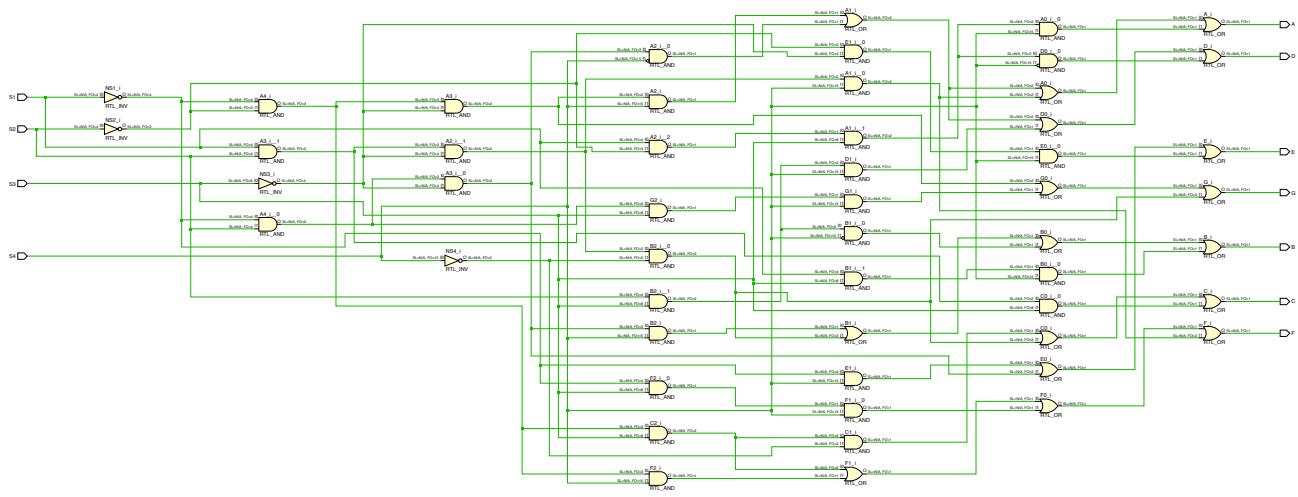
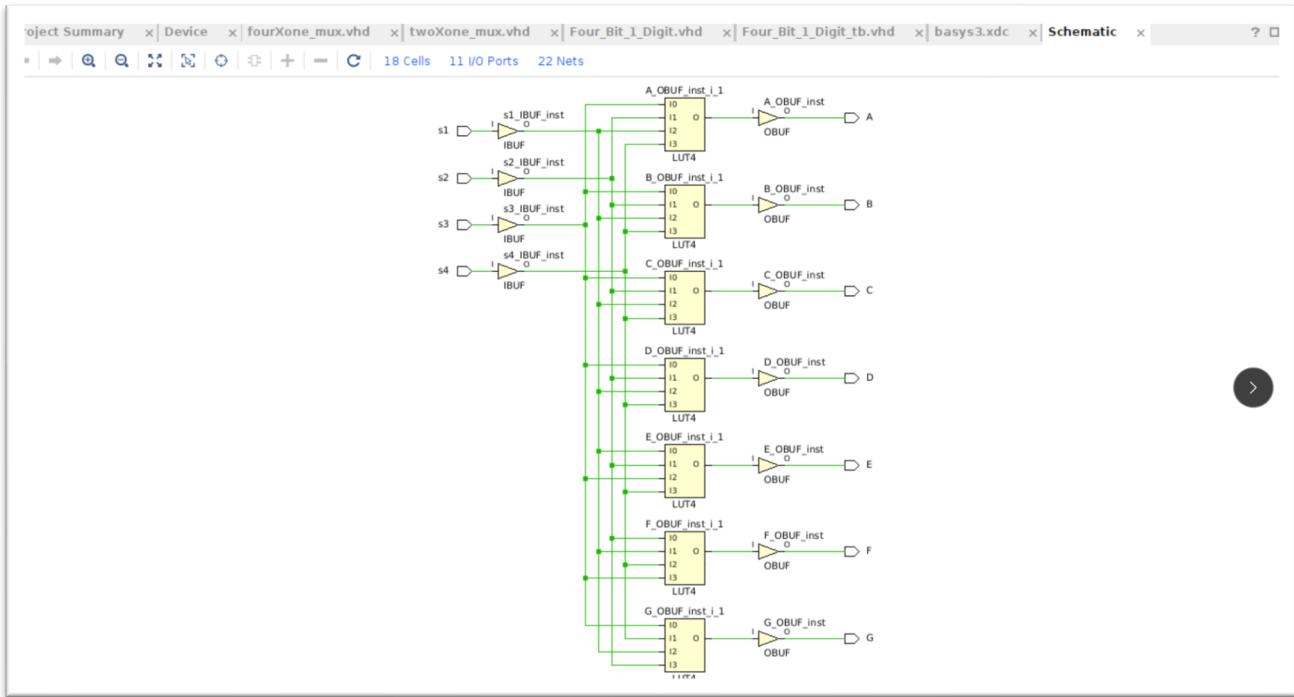
$$g = A'B'C' + A'BCD + ABC'D'$$

segment g

1.4 Simulation



1.5 Schematic Diagram



2 Driving all four LED displays

2.1 Aim

The aim is to design a system that drives four 7-segment displays using a 4:1 multiplexer and a timing circuit, ensuring proper refresh rates by dividing the 100 MHz clock signal on the Basys 3 board.

2.2 Approach

The design involves creating a 4:1 multiplexer to select one of the four 4-bit inputs (representing the digits) from the slider switches. The output of the multiplexer is fed into a 7-bit decoder, which drives the cathode signals of the 7-segment display. A timing circuit is used to control the anode signals, activating each display one at a time in a cyclic manner. To achieve the desired refresh rate, the onboard 100 MHz clock is divided using a timing circuit, ensuring a smooth display of each digit without flickering. The process is implemented using VHDL, where the timing signals are synchronized with the rising edge of the clock

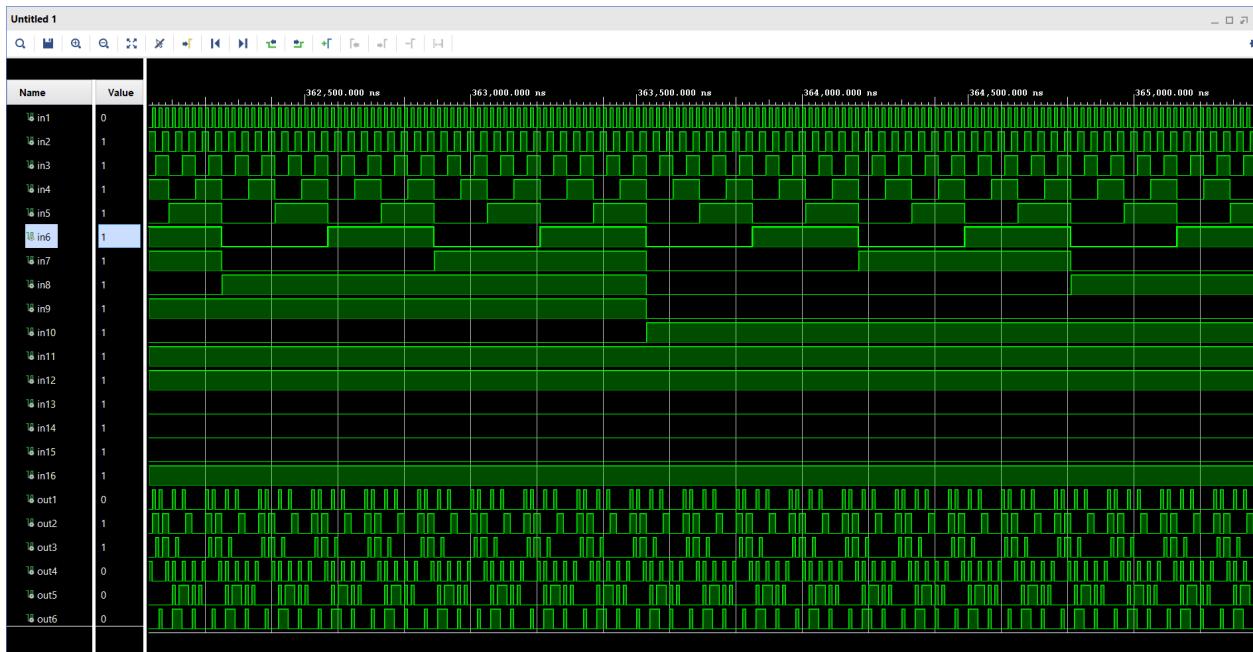
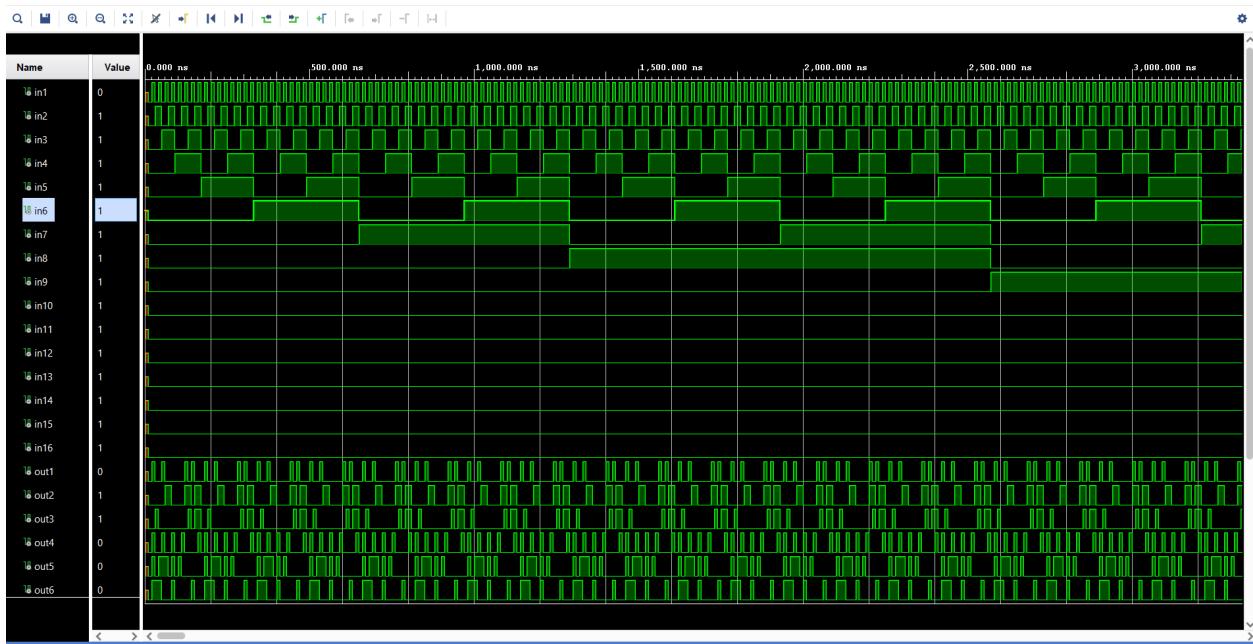
2.3 Simulation

2.3.1 Timing Circuit Test Bench Simulation

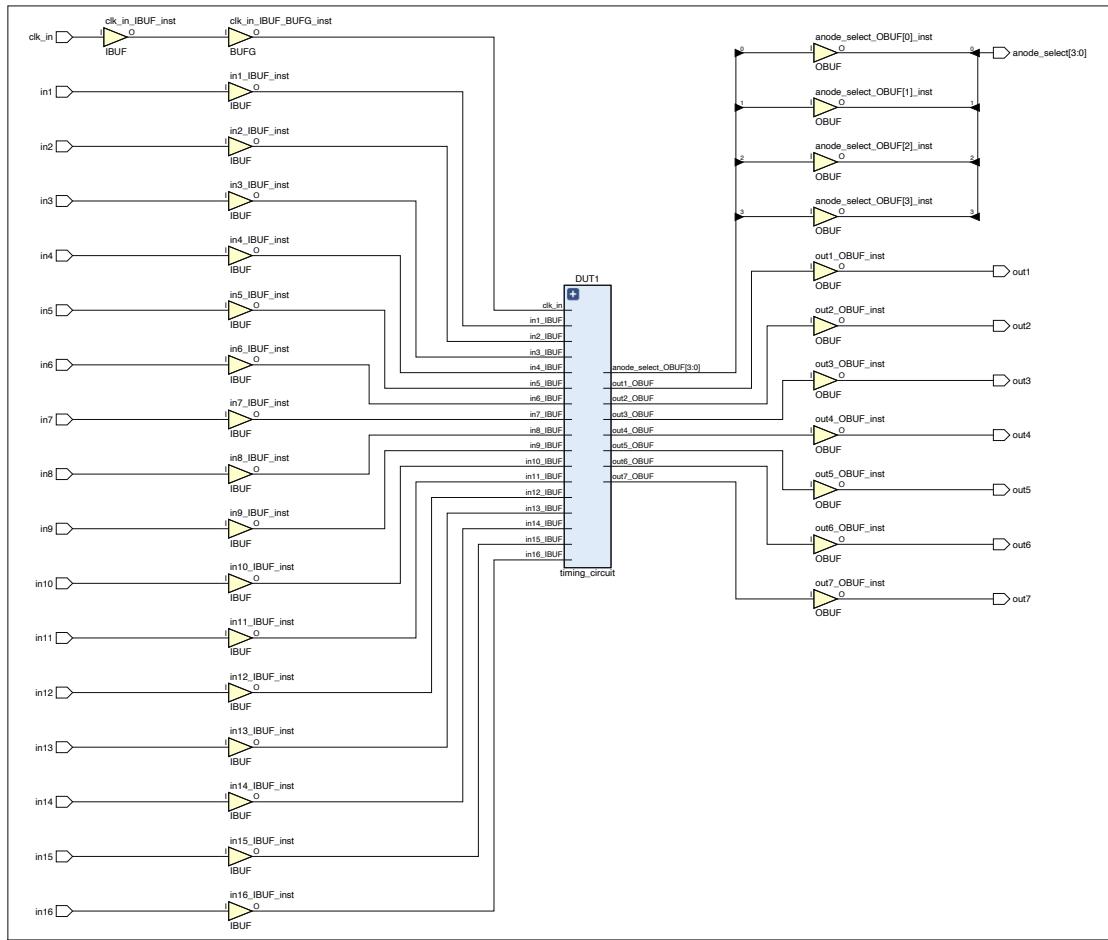
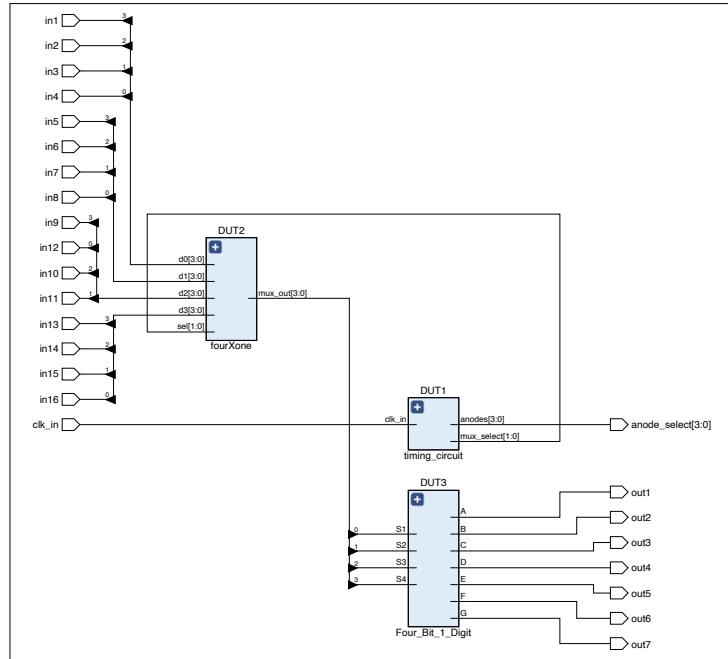


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2.3.2 Top Module Test Bench Simulation



2.4 Schematics



2.5 Utilization Report Statistics

2.5.1 Resource count of Flip-flops, LUTs, BRAMs, and DSPs

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	29	0	0	20800	0.14
LUT as Logic	29	0	0	20800	0.14
LUT as Memory	0	0	0	9600	0.00
Slice Registers	35	0	0	41600	0.08
Register as Flip Flop	35	0	0	41600	0.08
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
35	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	15	0	0	8150	0.18
SLICEL	6	0			
SLICEM	9	0			
LUT as Logic	29	0	0	20800	0.14
using 05 output only	0				
using 06 output only	11				
using 05 and 06	18				
LUT as Memory	0	0	0	9600	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	35	0	0	41600	0.08
Register driven from within the Slice	35				
Register driven from outside the Slice	0				
Unique Control Sets	3		0	8150	0.04

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

3 Extra's

3.1 Devices

