SCHOOL
OF
INFORMATION AND COMMUNICATION TECHNOLOGY

COURSE STURCTURE AND DETAILED SYLLABUS

3 YEARS M. TECH. ICT FOR SCIENCE GRADUATES

SPECIALIZATION:

VLSI

GAUTAM BUDDHA UNIVERSITY
GAUTAM BUDH NAGAR, GREATER NOIDA
2011-2012

SEMESTER – I

S. No.	Course Code	Courses	L	T	P	Credits
1	MA431	Engineering Mathematics	3	1	0	4
2	EC431	Digital Electronics	3	0	0	3
3	CS431/CS203	Operating System	3	0	0	3
4	CS433/CS202	Software Engineering	3	0	0	3
5	CS435	Problem Solving using C	3	1	0	4
6	SS431	Technical Communication	2	0	0	2
7	EC483/EC281	Digital Electronics Lab	0	0	2	2
8	CS483	Programming Lab	0	0	2	2
9	GP431	General Proficiency	-	-	-	1
		Total	**17**	**2**	**4**	**24**
		Total Contact Hours	**23**			

SEMESTER – II

S. No.	Course Code	Courses	L	T	P	Credits
1	EC442	Communication Engineering	3	0	0	3
2	CS434	Object- Oriented Programming with Java	3	0	0	3
3	CS436/CS206	Data Base Management System	3	0	0	3
4	CS438/CS309	Computer Organization and Architecture	3	0	0	3
5	EC444/EC205	Signal and Systems	3	1	0	4
6	EC446/EC306	Microelectronics Engineering	3	0	0	3
7	CS484/CS283	Object Oriented Programming with Java Lab	0	0	2	2
8	EC480	Design Lab	0	0	2	2
9	GP432	General Proficiency	-	-	-	1
		Total	**18**	**1**	**4**	**24**
		Total Contact Hours	**23**			

SEMESTER – III

S. No.	Course Code	Courses	L	T	P	Credits
1	CS531	Data Structures and Algorithms Design	3	1	0	4
2	CS533	Principles of Compiler Design	3	0	0	3
3	EC553	Data Communication	3	0	0	3
4	EC555/EC465	Principles of VLSI Design	3	0	0	3
5	EC557	Cellular Mobile communication	3	0	0	3
6	EC559/EC304	Microprocessors and Interfacing	3	0	0	3
7	CS583	Data Structures and Algorithms Design Lab	0	0	2	2
8	EC587/EC384	Microprocessors and Interfacing Lab	0	0	2	2
9	GP531	General Proficiency	-	-	-	1
		Total	**18**	**1**	**4**	**24**
		Total Contact Hours	**23**			

SEMESTER-IV

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	MA402	Simulation and Modeling	3-1-0	4
2	EC536	VLSI Technology	3-0-0	3
3	EC538	Advanced Analog VLSI Design	3-0-0	3
4		Elective-3	3-0-0	3
5		Elective-4	3-0-0	3
		PRACTICALS		
6	EC560	Design Lab II	0-0-2	2
7	EC592	Major Project	0-0-10	5
8	GP532	General Proficiency	---	1
		Total	**15-1-12**	**24**
		Total Contact Hours	28	

Electives (3 & 4)

Sr.No	Course Code	Courses
1.	EC566	VLSI for Wireless Communication
2.	EC542	Quality of Services in Networks
3.	CS447/CS547	Multimedia Techniques
4.	CS449/CS561	Soft Computing
5.	EC534	Wireless System Design
6.	CS404/CS534	Open Source Software System
7.	EC568	Design of Semiconductor Memories
8.	EC570	Principles of MEMS Design
9.	EC572	Solid State Electronics Devices
10.	EC574	Integrated Circuit Physical Design
11.	EC576	CMOS RF Circuit Design
12.	EC578	CMOS VLSI Design
13.	EC580	VLSI Design Techniques
14.	EC544	Advanced RF Engineering
15.	EC548	Probability and Stochastic Processes
16.	EC550	Advanced Microwave Communication
17.	EC556	Image Processing and Biometrics
18.	EC532	Advanced Communication Networks

SEMESTER – V

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC633	Low Power VLSI Design	3-0-0	3
2	CS633	Research Techniques in ICT	3-0-0	3
3		Elective- 5	3-0-0	3
4		Elective- 6	3-0-0	3
		PRACTICALS		
5	EC683	Design Lab III	0-0-2	2
6	EC691	Dissertation Part-I	0-0-14	7
7	GP631	General Proficiency	---	1
		Total	**12-0-16**	**22**
		Total Contact Hours	28	

Electives (5 & 6)

Sr.No	Course Code	Courses
1.	EC665	VLSI ASIC Design
2.	EC667	Micro and Smart System Technology
3.	EC669	Advances in VLSI Design
4.	EC671	Modern Optimization Techniques
5.	EC673	VLSI-Reliability Engineering
6.	EC647	Sensor Network
7.	EC675	Mixed-Signal VLSI Design
8.	EC677	DSP Integrated Circuits
9.	EC679	Advanced Digital VLSI Design
10.	EC659	Test and Verification of VLSI Circuits
11.	EC661	EM Interference and Capabilities in System Design
12.	EC663	Algorithm for VLSI Design Automation
13.	EC643	Smart Antenna System

SEMESTER-VI

Sr. No	Course Code	Courses	L-T-P	Credits
1	EC690	Dissertation Part-II	---	21
2	GP632	General Proficiency	---	1
		Total	**---**	**22**

Total Credits-140

DIGITAL ELECTRONICS			
Course Code:	**EC431**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exams Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exams Hours:**	**3**

Unit I: Review of Number systems and Binary codes, Binary arithmetic: addition, subtraction, multiplication and division algorithms. Boolean algebra: theorems and functions, Simplification of Boolean functions, minimization techniques, Karnaugh's map method,Quine and McCluskey's method, realization of various binary functions using AND ,OR,NOT,XOR logic gates.

Unit II: Universal gates: NAND, NOR, realization of boolean function using universal gates. Half and full adder, half and full subtractor, Series and parallel adder, BCD adders, look-ahead Carry adder. Decoders, Encoders, multiplexers and de-multiplexers. Analysis and design of combination circuits, realization of various Boolean functions using NAND,NOR gates and multiplexers.

Unit III: Flip-Flops: R-S, Clocked R-S, T, D, J-K, race around problem, Master-slave J-K., State and Excitation Tables Multivibrators- Astable, Monostable and bistable multivibrators, 555 timer chip and its application in multivibrators

Unit IV: Shift registers and counters, synchronous and asynchronous counters, Binary ripple counter, up-down counter, Johnson and ring counter, Analysis and Design of Sequential Circuits.

Unit V: Logic families: RTL, DTL, TTL, ECL, IIL, PMOS, NMOS and CMOS logic

Text Books:

[1] M. Mano :Digital Logic and Computer Design, Pearson Education
[2] William I. Fletcher :An Engineering Approach to Digital Design, Pearson Education
[3] R.P. Jain: Digital Electronics

References:

[1] M. Mano : Digital Design, Pearson Education
[2] W.H. Gothman : Digital Electronics, PHI.
[3] Millman and Taub : Pulse, Digital and Switching Waveforms, MGH
[4] Anand Kumar : Pulse and Digital Circuits , PHI
[5] Leach and Malvino : Digital Principles and Applications, TMH

DIGITAL ELECTRONICS LAB			
Course Code:	**EC483/EC281**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Verify the truth table of AND Gate
2. Verify the truth table of OR and NOT gates.
3. Verify the truth table of NAND , NOR Gates.
4. Verify the truth table of and EX-OR Gate.
5. Design a combinational circuit to realize the function f(ABC)=A(B+C) using NAND gates only.
6. Design a half adder using NOR gates only
7. Design full adder
8. Design a given size of Mux using gates.
9. Verify RS and JK flip flops
10. Verify D and T Flip flops
11. Design a up/down 3-bit counter
12. Design a 3 bit shift register.

OPERATING SYSTEM			
Course Code:	**CS431/CS203**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to Operating System

Importance of operating systems, basic concepts and terminology about operating system, memory management functions, processor management functions, device management functions, information management functions.

Unit II: Process Management

Elementary concept of process, job scheduler, process scheduling, operation on process, threads, overview, scheduling criteria, scheduling algorithms, algorithm evaluation process synchronization, synchronization hardware, semaphores, classical problem of synchronization, monitors and atomic transaction deadlocks: system model, deadlock characterization, deadlocks prevention, deadlocks avoidance, deadlocks detection, recovery from deadlock.

Unit III: Memory Management

Memory management, logical versus physical address space, swapping, contiguous allocation, paging, segmentation, demand paging, page replacement, page replacement algorithms, allocation of frames, thrashing, demand segmentation.

Unit IV: Storage Management

File concept, directory structure, protection, file-system structure, allocation method, free-space management, directory implementation.

Unit V: I/O Systems

I/O hardware, Application of I/O interface, Overview of Kernel I/O subsystem, three types of I/O systems, memory based I/O, I/O based I/O, Peripheral based I/O.

Text Books:

Reference Books:

[1] Galvin, Wiley, Operating Systems Concepts, 8th edition, 2009.
[2] James L Peterson, Operating Systems Concept, John Wiley & Sons Inc, the 6Rev edition, 2007.
[3] Deitel H. M., An Introduction to Operating Systems, Addison-Wesley, 1990.
[4] Stallings William, Operating Systems, PHI, New Delhi, 1997.
[5] Madnick and Donavon, Operating Systems, McGraw Hill, International edition, 1978.
[6] S. Tanenbaum Modern Operating Systems, , Pearson Education, 3rd edition, 2007.
[7] Nutt, Operating System, Pearson Education, 2009.
[8] S. Tanenbaum, Distributed Operating Systems, Prentice Hall, 2nd edition, 2007.
[9] M. Singhal & N. Shivaratri, Advanced Concepts in Operating Systems, McGraw Hill, 2003.

SOFTWARE ENGINEERING			
Course Code:	**CS433/CS202**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Software Engineering

Introduction to software engineering: definitions, Role of Software Engineering, planning a software project, defining the problem, developing a solution strategy, planning the development process, software engineering process paradigms, principles of software engineering, Software Engineering activities.

Unit II:Requirement Analysis and Design

Software Requirement Specification(SRS): Introduction, need of SRS, significance, characterstics of SRS, Structure of SRS, IEEE standards for SRS design, functional and non-functional requirements, Requirement gathering and analysis, requirement engineering and management.

Unit III: Software Design Process

Software Design: Introduction, Design Process Activities: Architectural design, Abstract specification, Interface design, Component design, Data structure design, Algorithm design Modular approach, Top-down design, Bottom-up design, Design methods: Data-flow model: Data Flow diagram, Entity-relation-attribute model: E-R diagram, Structural model: structure charts, context diagrams, Object models: use case modeling, use case diagrams, sequence diagrams, cohesion and coupling.

Unit IV: Software Life Cycle Models

Software Development Life Cycle (SDLC), SDLC models, waterfall model and its variations, prototype model, iterative enhancement model, spiral model, RAD model, comparison of these models, software development teams, software development environments, validation and traceability, maintenance, prototyping requirements, Software project management.

Unit V:Software Testing and Maintenance

Testing Methods: unit testing, integration testing, system testing, acceptance testing, testing techniques: white box testing, black box testing, thread testing, regression testing, alpha testing, beta testing, static testing, dynamic testing,

Evolution of software products, economics of maintenance, category of software maintenance, Role of product development life cycle, deployment model, adaptive maintenance, corrective maintenance, perfective maintenance, enhancement request, proactive defect prevention, problem reporting, problem resolution, software maintenance from customers' perspective, maintenance standard: IEEE-1219, ISO-12207.

Text Books:

[1] Pressman Roger S., Software Engineering: Practitioner's Approach, McGraw-Hill Inc., 2004.

Reference Books:

[1] Pankaj Jalote, An Integrated Approach to Software Engineering, Narosa Publishing House, New Delhi 1997.
[2] Ian Sommerville, Software Engineering, Pearson Education, 2009.

PROBLEM SOLVING USING C			
Course Code:	**CS435**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45+15**	**End Sem Exam Hours:**	**3**

Unit I: Introduction

Definition of Algorithms- Writing algorithms- top down design- Program verification- The efficiency of algorithms- Concept of Recursion- some simple example to illustrate these concepts like finding the GCD of two numbers. Swapping two variables- Summation of n given numbers- generation of Fibonocci sequence-Reversing a given number-Base conversion.

Unit II: Introduction to C

C character set- Delimiters-The C Keywords-Identifiers- Constants-Variables-Rules – Type Conversion-Priority of Operators and their Clubbing-Comma and Conditional Operator-Arithmetic Operators-Relational Operators-Logical Operators-Bitwise Operators-Input in C-Formatted and Unformatted Functions-Library Functions.

Unit III: More about C

if statement- if--- else statement-various forms of if-nested if-break statement-continue statement-go to statement- switch statement- nested switch statement – for statement –while statement do while statement to while statement – arrays – working with string and standard functions.

Unit IV: ADVANCED CONCEPTS OF C

Introduction to pointers – pointer declaration Arithmetic Operations with pointers- pointers and arrays-pointers and two-dimensional arrays-array of pointers – pointers to pointers- pointers and strings – void pointers – function definition and declaration – proto types of functions – call by value and reference – functions returning more values – function as an argument – function with operators – function and decision statements – function and loop statements – function with arrays and pointers – recursion – pointer to function –storage classes.

Unit V: Problem Solving

Reversal of an Array-Removal of duplicates in an ordered array-Partitioning of an array-Finding the Kth smallest of an element of an array-Finding the longest monotone subsequence of an array-Linear search-Binary search- Hash searching- Bubble sort – Merge sort – Quick sort-Insertion sort-selection sort-Text processing- Towers of Hanoi problem using recursion.

ADDITIONALS IN C: preprocessor directives – structures and unions – bit wise operators- files-command line arguments – dynamic memory allegation – graphics in C.

Text Books:

[1] Ashok N.Kamthane, Programming with ANSI and Turbo C, Pearson Education, New Delhi.
[2] R.G. Dromey, How to Solve it by computer, Prentice Hall of India Ltd, New Delhi.

Reference Books:

[1] N.G. Venkateshmurthy, Programming techniques through C, Pearson Education, New Delhi.
[2] Byron s Gottfried, Programming with C, Schaum's Outline series, Tata McGraw Hill Pub. Company, New Delhi.
[3]Jacqueline A.Jones & Keith Harrow, C programming with problem solving, Dreamtech publications, New Delhi.

PROGRAMMING LAB			
Course Code:	**CS483**	**Credits:**	**2**
No. of Practical (Hrs/Week):	**2**		
Total No. of Lab Sessions:	**15**	**End Sem. Exam Hours:**	**2**

Programs/Experiments List:

1. Write a C Code to implement each of the following:
   Variable, constant, arithmetic operator, relational operator, logical operator, assignment operator, increment & decrement operator, conditional operator, bitwise operator.
2. Write a C Code to implement each of the following:
   Decision statement, loops statement and branch statements
3. Write a C Code to implement each of the following:
   Array: Single and Two dimensional arrays
4. Write C Code to generate the following output with the help of two dimensional array.

   7 14 21 28 35 42 49 56 63 70 Sum = 385
   5 10 15 20 25 30 35 40 45 50 Sum = 275
   3 6 9 12 15 18 21 24 27 30 Sum = 165

5. Write C Code to implement each of the following.
   Matrix Multiplication, Matrix Addition
6. Write a C Code to implement each of the following:
   Strings, Standard library string functions and array of pointers to strings
7. Write a C Code to implement each of the following sorting:
   Bubble Sort, Selection Sort, Insertion Sort, Merge Sort
8. Write a C Code to implement each of the following searching:
   Linear search, Binary search and Hash searching
9. Write a C Code to implement each of the following:
   Function: Implementation of function with call by values and call by reference
10. Write a C Code to implement each of the following:
    Pointers: Pointers declaration, array of pointers, pointers to pointers, pointers and strings
11. Write a C Code to implement recursion and tower of Hanoi problem using recursion.
12. Write a C Code to implement each of the following:
    Structure, Array of structure
13. Write a C Code to implement each of the following:
    Pre-processor, Macro Expansion and File Inclusion
14. Write a C Code to implement the following:
    File Handling
15. Develop a mini projects in C.

COMMUNICATION ENGINEERING			
Course Code:	**EC442**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exams Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exams Hours:**	**3**

Unit I: Signals and its Representation
Review of Fourier transform, Convention, Signal transmission though linear systems, signal distortion in transmission, poley wiener criteria, Bandwidth and rise time, energy and power signals, spectral density and persevall's theorem for energy of power signals, Hilbert transform.

Unit II: Linear Modulation and Exponential Modulation
Linear Modulation: Definition, Necessity of modulation, Principle of amplitude modulation, Generation and detection of AM, Side bands, The generation and detection of side bands, Comparison of various AM systems, FDM, Synchronous detection.
Exponential Modulation: Definitions and relationship between PM and FM frequency deviation, Bessells function, spectrum and transmission BW of FM signals, NBFM, WBFM, phaser diagram of FM signal, multi tone FM, Generation and detection of FM Non linear effects in FM systems, comparison of AM and FM systems, TDM.

Unit III: Radio Transmitter and Receivers
Different types of AM and FM transmitters and receivers, AM and FM standard broadcast transmitter and receivers, image rejection, mixer.**Noise:**Classification and sources of noise, Noise calculations for single and cascaded stages, SNR, SNR in DSB, SSB, VSB, AM and FM systems, pre-emphasis and De-emphasis Sampling theorem, quantization, PCM, Companding intesymbol interface, Eye patterns, Delta modulation, Adaptive delta modulation, DPCM, SIN performance of PCM and delta modulation, bandwidth of PCM and delta modulation.

Unit IV: Digital Modulation Techniques
ASK, BPSK, QPSK, M-ray PSK, DPSK, BFSK, M-ray FSK, Duobinary signalling baseband signal receiver, Probability of error, Optimum filter, Matched filter, Coherent and non-coherent detection, bit error rate.Random signals, random variables and processes, cumnlative distribution function, probability density function, average value, variance, standard deviation moment and moment,] generating function, characteristics function, Tchebycheffs inequality, Binary, Poisson and Gaussian distributions, other distributions, central limit theorem.

Unit V: Information Theory and Coding
Unit of information, average information, joint and conditional entropy, mutual information, channel capacity efficiency, BBS and BEC, Shannon's Theorem, Shannon-Hartely theorem, bandwidth - SIN ratio trade-off. Coding separable codes, Prefix property, Coding efficiency, Source coding, Shannon - Fano code, Huffman code, Error connection codes, FEC and ARQ, Hamming distance, Minimum distance, Channel coding, Block code, Cyclic code, Convolutional code.

Text Books:
[1] S Haykin, Communication System, John Willey and Sons.
[2] Taub Schilling, Principle of Communication, TMH.
[3] B.P. Lathi, Modern Digital and Analog Communication System, Oxford Press.

References:

OBJECT ORIENTED PROGRAMMING WITH JAVA			
Course Code:	**CS534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Object-Oriented Programming

Concept of object-oriented programming (OOP), benefits of OOP, application of OOP, Java history, Java features, Java streaming, Java and Internet, Java contribution to Internet: Java applets, security, portability; Java environment, Java library, Java program structure, Java program, Java Virtual Machine (JVM) architecture, Just In Time compiler (JIT), data type, variables and arrays, operators, control statements, object-oriented paradigms; abstraction, encapsulation, inheritance, polymorphism, Java class and OOP implementation, packages and interfaces, multithreading.

Unit II:Distributed Computing

Collection framework, custom sockets, Remote Method Invocation (RMI), activation, object serialization, distributed garbage collection, RMI-IIOP (Internet Inter ORB (Object Request Broker) Protocol), interface definition language, JINI, Common Object Request Broker Architecture (CORBA), Java Data Base Connectivity (JDBC), database programming using JDBC, Servlets.

Unit III: Java Beans and Swing

Bean concepts, bean writing process, bean to build application: packaging beans in Java Archive (JAR) file, composing beans in a builder environment; naming patterns for bean properties and events, bean property types, files events in bean box, bean customization, persistence, application, origin of swing, swing and Abstract Window Toolkit (AWT), deployment using swing, advanced swing techniques, JAR file handling, exploring swings, advanced swing.

Unit IV: Java Enterprise Applications

Java Native Interface (JNI) technology, Java Servlet, Java Server Pages (JSP), JDBC, session beans, entity beans, Enterprise Java Beans (EJB), programming and deploying EJB, Java transactions, Java 2 Enterprise Editions (J2EE), J2EE design pattern, J2EE architecture, J2EE components and containers, J2EE services, Unified Modeling Language (UML), Extensible Markup Language (XML).

Unit V:Struts, Hibernate and Spring

Struts 2 frameworks, working with struts 2 actions, adding workflow with interceptors, data transfer, struts tags, user interface tags, integration with spring and hibernate, exploring the validation framework, internationalization, hibernate, hibernate architecture, hibernate configuration, creating persistent classes, mapping inheritance with Java classes, working with collections, persistent objects, scalar queries and hibernate query language, hibernate caching, hibernate transactions and locking, hibernate and XDOCLET, hibernate and eclipse, spring, basic bean wiring, advanced bean wiring, spring and EJB, spring with JDBC.

Text Books:

Reference Books:

[1] Hortsmann, Cornell, Core JAVA: Advance Features, Pearson Education, 2009.
[2] E. Balagurusawamy, Programming with JAVA, Tata McGraw Hill, 1998.
[3] Herbert Schildt, JAVA Beginner's guide, Tata McGraw Hill, 2007.
[4] Deitel & Deitel, Java How to Program, Prentice-Hall, 1999.

[5] Herbert Schildt, The Complete Reference JAVA 2, 7th Edition, Tata McGraw Hill, 2009.
[6] James Keogh, The Complete Reference J2EE, Tata McGraw Hill, 2002
[7] James Holmes, The Complete Reference Struts, Tata McGraw Hill, 2007.
[8] Herbert Schildt ,"Swings: A Beginners' Guide", Tata McGraw Hill, 2006.
[9] James Elliott, "Hibernate: A Developer's Notebook", O'Reily Media Inc, 2004.
[10] Ken Arnold, James Gosling," The Java Programming Language", Addison-Wesley, 1996.
[11] Rod Johnson, Jorgen Hoeller, Alef Arendsen, Thomas Risberg, Colin Sampaleanu, Wrox, "Professional Java Development with the Spring Framework", 2005.

DATABASE MANAGEMENT SYSTEM			
Course Code:	**CS436/CS206**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Data Base System
Data base system vs. file system, view of data, data abstraction, instances and schemas, data models, ER model, relational model, database languages, DDL, DML, database access for applications programs, data base users and administrator, transaction management, data base system structure, storage manager, query processor, history of data base systems, data base design and ER diagrams, beyond ER design entities, attributes and entity sets, relationships and relationship sets, additional features of ER model, concept design with the ER model, and conceptual design for large enterprises.

Unit II:Relational Model
Introduction to the relational model, integrity constraint over relations, enforcing integrity constraints, querying relational data, and logical data base design, destroying /altering tables and views. relational algebra and calculus: relational algebra, selection and projection set operations, renaming, joins, division, relational calculus, tuple relational calculus, domain relational calculus, expressive power of algebra and calculus.

Unit III: Basic SQL Query
Examples of basic SQL queries, nested queries, correlated nested queries set, comparison operators, aggregative operators, NULL values, comparison using null values, logical connectivity's, AND, OR and NOTR, impact on SQL constructs, outer joins, disallowing NULL values, complex integrity constraints in SQL triggers and active data bases.

Unit IV: Schema Refinement
Problems caused by redundancy, decompositions, problem related to decomposition, reasoning about FDS, FIRST, SECOND, THIRD normal form, BCNF, forth normal form, lossless join decomposition, dependency preserving decomposition, schema refinement in data base design, multi valued dependencies.

Unit V:Overview of Transaction Management
ACID properties, transactions and schedules, concurrent execution of transaction, lock based concurrency control, performance locking, and transaction support in SQL, crash recovery, concurrency control, Serializability and recoverability, lock management, lock conversions, dealing with dead locks, specialized locking techniques, concurrency without locking, crash recovery: ARIES, log, other recovery related structures, the write, ahead log protocol, check pointing, recovering from a system crash, media recovery, other approaches and interaction with concurrency control.

Text Books:

References:
[1] Elmasri Navrate, Data Base Management System, Pearson Education, 2008.
[2] Raghurama Krishnan, Johannes Gehrke, Data Base Management Systems, TMH, 3rd edition, 2008.
[3] C. J. Date, Introduction to Database Systems, Pearson Education, 2009.
[4] Silberschatz, Korth, Database System Concepts, McGraw hill, 5^{th} edition, 2005.
[5] Rob, Coronel & Thomson, Database Systems Design: Implementation and Management, 5th edition, 2009.

COMPUTER ORGANIZATION AND ARCHITECTURE			
Course Code:	**CS438/CS309**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Computer Arithmetic and Number System
Number representation, Number System, fixed and floating point number representation, Arithmetic Algorithms (addition, subtraction, Booth Multiplication).

Unit II: Register Transfer and Microoperation
Register Transfer Language, Bus and Memory Transfers, Bus Architecture, Bus Arbitration, Arithmetic Logic, Shift Microoperation, Arithmetic Logic Shift Unit, Design of Fast address

Unit III: Processor Design
Processor Organization: General register organization, Stack organization, Addressing mode, Instruction format, Data transfer & manipulations, Program Control, Reduced Instruction Set Computer.

Unit IV: Input-Output Organization
I/O Interface, Synchronous and Asynchronous Data Transfer, strobe, handshaking scheems Modes of transfer, Interrupts & Interrupt handling, Direct Memory access, Input-Output processor.

Unit V:Memory Organization
Memory Hierarchy, Main Memory (RAM and ROM Chips), organization of 2D and 21/2D, Auxiliary memory, Cache memory, Virtual Memory, Memory management hardware.

Text Books:
[1] Patterson, Computer Organisation and Design, Elsevier Pub. 2009
[2] John P Hays, " Computer Organization", McGraw Hill

References:
[3] William Stalling, " Computer Organization", PHI
[4] Vravice,Hamacher & Zaky, "Computer Organization", TMH
[5] Mano," Computer System Architecture", PHI
[6] Tannenbaum," Structured Computer Organization', PHI
[7] P Pal chaudhry, ' Computer Organization & Design', PHI

SIGNAL AND SYSTEMS			
Course Code:	**EC444/EC205**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: LTI Systems

Continuous time and discrete time signals, Even and Odd signals. Elementary continuous time and discrete time signals, Classification of signals, causality; stability, time invariance, linearity, Continuous time and Discrete time LTI Systems, convolution Integral and convolution sum, Properties of LTI Systems, Differential and Difference equations. Singularity functions.

Unit II: Analysis of Periodic Signals

Fourier series representation of CTPS, convergence of FS, Properties of CTFS, Fourier series representation of DTFS. Fourier series and LTI Systems, Filtering, RC low pass and high pass filters. Recursive and Non recursive Discrete Time filters.Sampling theorem, sampling of continuous time signal with impulse train and zero order hold Reconstruction, Aliasing, Discrete-time processing of continuous time signals, Digital differentiator, Sampling of discrete time signals, decimation and Interpolation

Unit III: Analysis of Aperiodic Signals

Continuous Time Fourier Transform (CTFT), Convergence of FT. Properties of CTFT, Discrete time Fourier Transform (DTFT), Properties of DTFT. System characterized by linear constant co-efficient differential equations. Magnitude and phase spectrum, group delay, Time domain and frequency domain aspects of ideal Non-ideal filters. First order and second order continuous time and discrete time systems

Unit IV: Laplace Transform

The Laplace transform, Region of convergence, Inverse Laplace transform. Geometric evaluation of Fourier transform from pole zero plot, First order, second order and all pass systems. Properties of Laplace transform Analysis and characterization of LTI systems using the Laplace transform. Causality, stability, Differential equations, Butterworth and Chebychev filters. Unilateral Laplace transform its properties and uses.

Unit V: Convolution and Correlation of Signals

concept of convolution in time domain and frequency domain, graphical representation of convolution, convolution property of Fourier Transform, cross-correlation and auto-correlation of functions, properties of correlation function, energy density spectrum, Parseval's Theorem, power density spectrum, detection of periodic signals in the presence of noise by correlation

Text Books:

[1] Oppenheim Willsky and Nawab,:Signals and Systems, PHI.
[2] Simon Haykin: Signals and Systems, John Wiley.
[3] Taub and Schilling: Principles of Communication Systems, TMH.
[4] Dungan F R: Electronic Communication Systems, Thomas-Delmar.

References:

MICROELECTRONICS ENGINEERING			
Course Code:	**EC446/EC306**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: MOSFETS

Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation. MOSFET internal capacitances and high frequency mode, CMOS digital logic inverter, detection type MOSFET.

Unit II: Single Stage IC Amplifier

IC Design philosophy, comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response, CS and CF amplifiers, CG and CB amplifiers, Cascade amplifiers, CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance.

Unit III: Differential and Multistage Amplifiers

MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers, Multistage amplifier.

Unit IV: Feedback and Operational Amplifiers

General Feedback structure, properties of negative feedback, basic feedback topologies, loop gain, Stability problem, effect of feedback on amplifier poles, stability analysis by Bode plots, frequency compensation. Two stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amps. Data Converters, A-D and D-A converters.

Unit V: Digital CMOS circuits

Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits.

Text Books:

[1] Adel Sedra and K.C. Smith, Microelectronic Circuits, 5th Edition, Oxford Uni. Press, 2004.
[2] Richard C. Jaeger and Blalock, Microelectronic Circuit Design,3rd Edition, TMH 2007

References:

[1] Behzad Razavi, Fundamentals of Microelectronics, John Wiley, 2008

OBJECT-ORIENTED PROGRAMMING WITH JAVA LAB			
Course Code:	**CS484**	**Credits:**	**2**
No. of Practical (Hrs/Week):	**2**		
Total No. of Lab Sessions:	**15**	**End Sem. Exam Hours:**	**2**

Programs/Experiments List:

1. Write a separate Java Code to implement each of the following:
   Class, Command Line Argument, how to enter value through keyboard

2. Write a separate Java Code to implement each of the following data types:
   Variable, Constant, Arrays, Strings, Vectors, Wrappers Classes, Type Casting

3. Write a separate Java Code to implement each of the following operators:
   Arithmetic operator, Relational operator, Logical operator, Assignment operator, Increment & Decrement operator, Conditional operator, Bitwise operator, ?: operator

4. Write a separate Java Code to implement each of the following control statements:
   Decision statement, Loops statement and Branch statements

5. Write a separate Java Code to implement each of the following sorting:
   Bubble Sort, Selection Sort, Insertion Sort, Merge Sort

6. Write a separate Java Code to implement each of the following:
   Class, Object, Constructors, Method, Method Overloading and Method Overriding

7. Write a separate Java Code to implement each of the following:
   Final variable, final class, final method, abstract class, abstract method and concrete method

8. Write a separate Java Code to implement each of the following OOPs concepts:
   Abstraction, Polymorphism, Encapsulation, Inheritance
9. Write a separate Java Code to implement each of the following:
   Exception handling with Try, Catch, Throw, Throws, Finally
   Multiple catch statement with the following exceptions :
   ArithmeticException, ArrayOutOfBoundsException and ArrayStoreException

10. Write a separate Java Code to implement each of the following:
    Visibility Controls: Private, Public and Protected

11. Write a separate Java Code to implement each of the following:
    Interface, extending and implementing interface

12. Write a separate Java Code to implement each of the following:
    Multithreading: Create thread with thread class and runnable interface, thread priorities, synchronization

13. Write a separate Java Code to implement each of the following:
    Packages : Create package A with following methods and import this package A into another Java program to show the result of methods of package A.
    i) First method: Factorial number with the help of recursion.
    ii) Second method: Fibonacci Series
    iii) Third Method: Generate first 10 prime numbers and show the sum of first 10 prime numbers.

14. Write Java Code to generate the following output on applet with the help of two dimensional array and show the result with the help of HTML file.

7 14 21 28 35 42 49 56 63 70	Sum = 385
5 10 15 20 25 30 35 40 45 50	Sum = 275
3 6 9 12 15 18 21 24 27 30	Sum = 165

15. Write a Java Code to design the following web page with the help of applet and HTML.

School of Information and Communication Technology
GAUTAM BUDDHA UNIVERSITY
GREATER NOIDA

- **Student Name:**
- **Enrollment Number:**
- **Programme Name:**
- **Semester:**
- **Course Name:**
- **E-Mail ID:**
- **Mobile Number:**
- **Blood Group:**

DESIGN LAB			
Course Code:	**CS484**	**Credits:**	**2**
No. of Practical (Hrs/Week):	**2**		
Total No. of Lab Sessions:	**10**	**End Sem. Exam Hours:**	**2**

1. Characterization of JFET.
2. Characterization of MOSFET
3. Design of Inverter Using MOSFET.
4. Design of an Inverting Amplifier using OP-AMP.
5. Design of noninverting Amplifier using OP-Amp.
6. Design of an integrater using Op-Amp.
7. Design of Astable Multivibrator using 555 Timer.
8. Design of Schmitt trigger using 555 timer
9. Design an 8-bit A/D Converter.
10. Design an 8-bit D/A Converter.
11. Verify the truth table of AND, OR and NOT gates.
12. Verify the truth table of NAND , NOR and EX-OR Gate.
13. Design a combinational circuit to realize the function f(ABC)=A(B+C) using NAND gates only.
14. Design a half adder using NOR gates only
15. Design full adder
16. Design a given size of Mux using gates.
17. Verify RS and JK flip flops
18. Verify D and T Flip flops
19. Design a up/down 3-bit counter
20. Design a 3 bit shift register.

DATA STRUCTURES AND ALGORITHMS DESIGN			
Course Code:	**CS531**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to Data Structures

Abstract data types - Sequences as value definitions - Data types in C -Pointers in C -Data structures and C - Arrays in C - Array as ADT – One dimensional array -Implementing one dimensional array - Array as parameters- Two dimensional array -Structures in C - Implementing structures – Unions in C - Implementation of unions -Structure parameters - Allocation of storage and scope of variables. Recursive definition and processes: Factorial function - Fibonacci sequence - Recursion in C - Efficiency of recursion. Hashing: Hash function, open hashing, closed hashing: Linear probing, quadratic probing, double hashing – Rehashing – extendible hashing.

Unit II: Stack, Queue and Linked List

Stack definition and examples – Primitive operations – Example -Representing stacks in C - Push and pop operation implementation. Queue as ADT - C Implementation of queues - Insert operation – Priority queue – Array implementation of priority queue. Inserting and removing nodes from a list-linked implementation of stack, queue and priority queue - Other list structures - Circular lists: Stack and queue as circular list -Primitive operations on circular lists. Header nodes - Doubly linked lists - Addition of long positive integers on circular and doubly linked list.

Unit III: Trees

Binary trees: Operations on binary trees - Applications of binary trees - Binary tree representation - Node representation of binary trees – Implicit array representation of binary tree – Binary tree traversal in C – Threaded binary tree - Representing list as binary tree – Finding the Kth element – Deleting an element. Trees and their applications: C representation of trees - Tree traversals - Evaluating an expression tree - Constructing a tree.

Unit IV: Sorting and Searching

General background of sorting: Efficiency considerations, Notations, Efficiency of sorting. Exchange sorts: Bubble sort; Quick sort; Selection sort; Binary tree sort; Heap sort. Heap as a priority queue - Sorting using a heap-heap sort procedure - Insertion sorts: Simple insertion - Shell sort - Address calculation sort - Merge sort -Radix sort. Sequential search: Indexed sequential search - Binary search – Interpolation search.

Unit V: Graphs

Application of graph - C representation of graphs - Transitive closure - Warshall's algorithm – Shortest path algorithm - Linked representation of graphs - Dijkstra's algorithm - Graph traversal - Traversal methods for graphs - Spanning forests - Undirected graph and their traversals – Depth first traversal - Application of depth first traversal - Efficiency of depth first traversal - Breadth first traversal - Minimum spanning tree - Kruskal's algorithm - Round robin algorithm.

Text Books:

[1] Aaron M. Tenenbaum, Yeedidyah Langsam, Moshe J. Augenstein, 'Data structures using C', Pearson Education, 2004 / PHI.

References:

[1] E. Balagurusamy, 'Programming in Ansi C', Second Edition, Tata McGraw Hill Publication, 2003.
[2] Robert L. Kruse, Bruce P. Leung Clovis L.Tondo, 'Data Structures and Program Design in C', Pearson Education, 2000 / PHI.

DATA COMMUNICATION			
Course Code:	**EC553**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to Data Communication and Networks

Data Communication, Networks – Physical structures; different topologies, Categories of Networks: LAN, MAN, WAN, Interconnection of networks, The Internet, Protocols and Standards, Standards Organizations. Network Models, Layered tasks, The OSI model, different layers in OSI model. TCP/IP protocol suite ; different layers, addressing, - physical, logical, port and specific addresses, Analog and digital, digital signals-Bit Length, Digital Signal as a Composite Analog Signal, Transmission of Digital Signals, Data Rate Limits-Noiseless Channel, Noisy Channel.

Unit II:Physical Layer

Digital-to-Digital Conversion-Line Coding, Line Coding Scheme, Block Coding, Scrambling. Multiplexing – Frequency Division, Wavelength Division, Synchronous Time Division, Statistical Time Division Multiplexing. Circuit-Switched Networks – Three Phases, Efficiency, Delay. Datagram Networks - Routing Table, Efficiency, Delay, Datagram Networks in the Internet. Virtual Circuit Networks - Addressing, Three Phases, Efficiency, Delay, Circuit Switched Technology in WANs. Structure of Circuit and Packet switches, Dial-up Modems, Digital Subscriber Line - ADSL, ADSL Lite, HDSL, SDSL, VDSL, Cable TV for Data Transfer- Bandwidth, Sharing, CM and CMTS, Data Transmission Schemes.

Unit III: Data Link Layer

Introduction - Types of Errors, Redundancy, Detection Vs Correction, Forward Error Correction Vs Retransmission, Modular Arithmetic. Block Coding - Error Detection, Error Correction, Hamming Distance, Minimum Hamming Distance. Linear Block Codes, Cyclic Codes - Cyclic Redundancy Check, Hardware Implementation, Polynomials, Cyclic Code Analysis, Advantages. Checksum, Framing - Fixed and Variable-Size. Flow and Error Control, Protocols, Noiseless Channels – Simplest and Stop-and-Wait Protocols. Noisy Channels - Stop-and-Wait Automatic Repeat Request, Go-Back-N Automatic Repeat Request, Selective Repeat Automatic Repeat Request.

Unit IV: Medium Access

Random Access- ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). Controlled Access-Reservation, Polling, Token Passing. Channelization- Frequency-Division Multiple Access (FDMA), Time-Division Multiple Access (TDMA), Code-Division Multiple Access (CDMA). IEEE Standards, Standard Ethernet, Changes in the Standard, Fast Ethernet, Gigabit Ethernet, IEEE 802.11- Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer. Bluetooth- Architecture, Radio Layer, Baseband Layer, L2CAP.

Unit V: Connecting LANs

Connecting Devices- Passive Hubs, Repeaters, Active Hubs, Bridges, Two-Layer Switches,Three-Layer Switches, Gateway. Backbone Networks-Bus, Star, Connecting Remote LANs. Virtual LANs - Membership, Configuration, Communication between Switches, Network layer – logical addressing - IPv4Addresses- Address Space, Notation, Classful Addressing, Classless Addressing, Network Address Translation (NAT). IPv6 Addresses - Structure and Address Space. Internetworking - Need for Network Layer, Internet as a Datagram Network, Internet as a Connectionless Network. IPv4- Datagram, Fragmentation, Checksum, Options. IPv6 Advantages, Packet Format, Extension Headers. Transition from IPv4 to IPv6. Address Mapping- Logical to Physical Address, Physical to Logical Address, Routing – Delivery forwarding techniques and processes, routing table,, Unicast routing protocols – Optimization, inter domain, intra domain, distance vector, link state and path vector.

routing, Multicast routing protocol - Unicast, multicast and broadcast, applications, multicast routing and routing protocols.

Text Books:

[1] B. A. Forouzan and Sophia Chung Fegan: Data Communications and Networking, 4th Ed, TMH.
[2] W. Tomasi: Introduction to Data Communications and Networking, Pearson Education.
[3] A. S. Tanenbaum: Computer Networks, Pearson Education.
[4] W. Stalling: Data and Computer Communication, Pearson Education.

References:

PRINCIPLES OF VLSI DESIGN			
Course Code:	**EC555/EC465**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Basic MOS Technology

Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks.MOS Device Design Equations, The Complementary CMOS Inverter: DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter.

Unit II: Circuit Design Processes and CMOS Logic Structures

MOS layers, Stick diagrams, Design rules and layout – lambda-based design and other rules, Layout diagram, Symbolic diagrams, Basic Physical Design of Simple logic gates, CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic.

Unit III: MOS Circuits Concepts

Sheet resistance, Area capacitances, Capacitance calculations, delay unit, Inverter delays, Driving capacitive loads, Propagation delays, Wiring capacitances, Scaling models and factors, Limits on scaling, Limits due to current density and noise.

Unit IV: CMOS Subsystem Design and Processes

Architectural issues, Switch logic, Gate logic, Design examples – combinational logic, Clocked circuits, other system considerations, Clocking Strategies, Subsystem design processes: General considerations, Process illustration, ALU subsystem, Adders. Multipliers.

Unit V: Advance Topic

Memory registers and clock: Timing considerations. Memory elements, Memory cell arrays. Testability: Performance parameters. Layout issues. I/O pads, System delays, Ground rules for design, Test and testability.

Text Books:

[1] CMOS VLSI Design – A Circuits and Systems Perspective, 3rd Edition, N.H. Weste and David Harris. Addison- Wesley, 2005.
[2] Basic VLSI Design - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition, 2005.

Reference Books:

[1] Principles of CMOS VLSI Design: A Systems Perspective, Neil H. E. Weste, K. Eshragian, Pearson Education (Asia) Pvt. Ltd.

CELLULAR MOBILE COMMUNICATION			
Course Code:	**EC557**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
Introduction to cellular mobile system A basic cellular system, Performance criteria, Uniqueness of Mobile Radio Environment, Operation of cellular systems, Planning and cellular system.

Elements of Cellular Radio System Design: General description of problem, Concept of frequency channels, Co channel interface reduction factor, Hand off, Cell splitting, Consideration of the components of cellular systems.

Unit II:
Interface: Introduction to co-channel interface, Real time Co-channel interface Co-channel measurement, Design of antenna system, Antenna parameter and their effects, Diversity receiver non co-channel interface different types.

Unit III:
Cell coverage for signal and traffic : General introduction, Obtaining the mobile point-to-point mode propagation over water or flat open area, foliage loss, propagation near in distance, long distance propagation, point-to-point prediction model-characteristics, cell site, Antenna heights and signal coverage cells, Mobile-to-mobile propagation.

Unit IV:
Cell site antennas and mobile antennas: Antennas at cell site, mobile antennas. Frequency management and Channel Assignment: Frequency management, Fixed channels assignment, Non-fixed channel assignment, Traffic and channel assignment.

Unit V:
Digital Cellular System: GSM, Architecture, Layer Modeling, Transmission, GSM channels, Multiple process, CDMA, Terms, Power limits & Control Modulation characteristics, Call processing, Hand off.

Text Books:
[1] Lee, Cellular and Mobile Communication, McGraw Hill.
[2] Faher Kamilo., Wireless Digital Communication, PHI.

References:

MICROPROCESSORS AND INTERFACING			
Course Code:	**EC559/EC304**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to 8085 microprocessor: Pin diagram, architecture, programming model, instruction set, and classification of instruction set, instruction and data format, timing diagram of instructions. Basic concept of programming, Addressing Modes of 8085 microprocessors

Unit II: Microprocessor 8086 Architecture - BIU and EU, Registers, Pin Diagram, Memory Addressing, Clock Generator 8284, Buffers and Latches, Maximum and Minimum Modes

Unit III: Addressing Modes, Instruction set of 8086, Assembly Language Programming, Assemblers, Procedures, Macros, Interrupts, 8086 Based Multiprocessor Systems

Unit IV: Interfacing Chips- IC 8155 (Static Ram with I/O Ports and Timer), 8755 (EPROM with I/O Ports), 8251A (USART), 8255A(Programmable Peripheral Interface), 8253/8254 (Programmable Interval Timer/Counter), 8257 (DMA Controller), 8259A (Programmable Interrupt Controller)

Unit V: The 8051 architecture Microprocessor and Microcontroller, Comparison of microprocessors and microcontrollers Microcontroller survey – microcontrollers of different word length, make and features, selection criteria for microcontroller ,8051 microcontroller hardware – I/O pins and internal architecture internal RAM,ROM organization , I/O port circuits ,connecting external memory, addressing modes , Instruction set and assembly language programming.

Text Books:

[1] A K Ray : Advanced Microprocessors and Interfacing, 2nd edition,TMH
[2] Mazidi and Mazidi: The 8051 Microcontroller and Embedded Systems, Pearson Education

References:

[1] B. B. Brey: The Intel Microprocessors, Architecture, Programming and Interfacing, Pearson Education.
[2] Liu Gibson: Microcomputer Systems: The 8086/8088 Family- Architecture, Programming and Design, PHI
[3] D. V. Hall: Microprocessors and Interfacing, TMH.
[4] Ayala Kenneth:The 8051 microcontroller, Third Edition, Cengage Learning
[5] A. V. Deshmukh: Microcontroller (Theory and Application), TMH.
[6] Raj Kamal: Embedded Systems- Architecture, Programming and Design, TMH, New Delhi.
[7] V. Udayashankara and M. S. Mallikarjunaswamy: 8051 Microcontroller, TMH, New Delhi.
[8] R S Gaonkar, Microprocessor, Architecture, Programming, and Applications with the 8085, Penram International Publication, 5/e
[9] P.K. Ghosh and P. R. Sridhar, 0000 to 8085 Introduction to microprocessor for Engineers and Scientists, PHI, 2/e

VLSI TECHNOLOGY			
Course Code:	**EC536**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II: Lithography and Relative Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III: Deposition, Diffusion, Ion Implantation and Metallization
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV: Process Simulation and VLSI Process Integration
Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V: Assembly Techniques and packaging of VLSI Devices
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

Text Books:
[1] S.M.Sze: VLSI Technology, Mc.Graw Hill Second Edition. 2002.
[2] Richard Jaegar, Introduction to Microelectronics Fabrication, Addison-Wesley, 2006.
[2] Douglas A. Pucknell and Kamran Eshraghian: Basic VLSI Design, Prentice Hall India, 2003.

References:
[1] Amar Mukherjee: Introduction to NMOS and CMOS VLSI System design, Prentice Hall India, 2000.
[2] Wayne Wolf : Modern VLSI Design, Prentice Hall India,1998.
[3] Plummer, Deal and Graffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Prentice Hall, 2000

ADVANCED ANALOG VLSI DESIGN			
Course Code:	**EC538**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I- Introduction
Basic building blocks in Analog ICs, Translinear networks, Video and RF/IF Amplifiers, IC negative feedback wide band amplifiers, Voltage Sources and References, IC Voltage Regulator, Characteristics and Parameters of Voltage, Protection circuitry for Voltage Regulator, Switched Mode Regulator, IC Voltage Op Amps, Transconductance Op Amps, Audio Power and Norton's Amplifier, Analog Multipliers, Voltage Controlled Oscillator, Self Tuned Filter, Phase Locked Loop, Current Mode ICs.

UNIT II – CMOS Analog Circuit Design
Submicron, Deep Submicron and Ultra-Deep Submicron CMOS Technology, BiCMOS Technology, Latchup and ESD, MOS Capacitor Model, Large Signal Model Dependence, Small Signal Models, Noise, Passive Component Models, Component Matching, Computer Models and Extraction of the Simple Large Signal Model, MOS Switch, Current Sinks and Sources.

UNIT III – High Speed Operational Amplifiers & Comparators Design
Two-stage Op Amp Design, Simulation and Measurement of Op Amps, Buffered Op Amps, High Speed Op Amps, Differential-In, Differential-Out Op Amps, Low Noise and Low Power Op Amps, Low Voltage Op Amps, Open-Loop Comparators, Improved Open-Loop Comparators and Latches, High speed comparators

UNIT IV – Design of ADCs & DACs
Characterization of DACs and Current Scaling DACs, Voltage, Charge Scaling and Serial DACs, Improved Resolution, Characterization of ADCs and Sample and Hold Circuits, Moderate Speed Nyquist ADCs, High Speed Nyquist ADCs, Oversampling ADCs.

UNIT V – Advance Topics
Analysis and optimized design of integrated analog systems and building blocks, Specific topics include operational and wide-band amplifiers, gain-bandwidth and power considerations, analysis of noise in integrated circuits, low noise design, feedback, precision passive elements, analog switches, comparators, CMOS voltage references, non-idealities such as matching and supply/IO/substrate coupling.

Text Books:
[1] Allen and Holberg, CMOS Analog Circuit Design, Oxford University Press
[2] Hurst and Meyer, Analysis and Design of Analog Integrated Circuits, Wiley
[3] Behzad Razavi, Design of Analog CMOS ICs, 2000. John Wiley
[4] Jaeger and Blalock, Microelectronics Circuit Design, McGraw Hill

References:
[1] Agarwal & Lang, Foundations of Analog and Digital Electronic Circuits, (The Morgan Kaufmann Series in Computer Architecture and Design)
[2] Behzad Razavi, Introduction to Microelectronics, 2006. John Wiley

DESIGN LAB II			
Course Code:	**EC560**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to Cadence Virtuoso tool and Full Custom IC Design cycle.
2. Realization of an Inverter.
3. Realization of Differential Amplifier.
4. Realization of Common Source Amplifier.
5. Realization of Common Drain Amplifier.
6. Realization of Operational Amplifier.
7. Realization of R-2R DAC.
8. Realization of SAR based ADC.

VLSI FOR WIRELESS COMMUNICATIONS			
Course Code:	**EC408/EC566**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Standards, Communication Systems, Overview of Modulation Scheme, QPSK, BPSK, MSK, Classical Channel, Wireless Channel Description, Path Environment, Path Loss, Friss Equation, Time Varying Channel Models, Envelope Fading, Frequency Selective Fading, Fast Fading.

Unit II: Receiver Architectures
Introduction, Receiver Front: Motivations, Heterodyne and other Architecture, Filter Design: Band Selection Filter, Image Rejection Filter, Channel Filter, Nonidealities and Design Parameters: Nonlinearity, Noise, Derivation of NF, IIP_3 of receiver Front end.

Unit III: Low Noise Amplifier (LNA)
Introduction, Matching Networks, Wideband LNA Design, DC bias, Gain and Frequency Response, Noise Figure, Narrowband LNA, Impedance Matching, Interpretation of Power Matching, Quality Factor, Core Amplifier, Noise Figure, Power Dissipation, Noise Contribution from other sources.

Unit IV: Active Mixers
Unbalanced Mixers, Single Balanced Mixers, Qualitative Description of Gilbert Mixer, Conversion Gain, Distortion analysis of Gilbert Mixer, Comparison of Sample and Hold Circuit and Sampling Mixer.

Unit V: Passive Mixers
Switching Mixers, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single Ended Sampling Mixer, Distortion in single ended sampling mixer, Intrinsic and Extrinsic noise.

Text Books:
[1] Bosco Leung, "VLSI for Wireless Communication", PHI.

References:
[1] Emad N Farag, M.I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems", Kluwer Publication.
[2] David Tsee, Pramod Viswanath," Fundamentals of Wireless Communication", Cambridge Univ Press.

QUALITY OF SERVICES IN NETWORKS			
Course Code:	**EC406/EC542**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: IP Quality Of Service
Level of QoS, IP QoS history, performance measures, QoS functions, layer 2 QoS technologies, multiprotocol label switching, end-to-end QoS.

Unit II: QOS Architectures
Intserv architecture; RSVP, reservation style, service types, RSVP media support, RSVP scalability, along with their case studies. Diffserv architecture; network boundary traffic conditioners, PHB, resource allocation policy, packet classification.

Unit III: Network Boundary Traffic Conditioners and Resource Allocation
Packet classification, packet marking, need of traffic rate management, traffic policing, traffic shaping along with their case studies. Scheduling of QoS support, sequence number computation based WFQ, flow based WFQ, flow based distributed DWFQ, class based WFQ, priority queuing, schedule mechanisms for voice traffic, MWRR, MDRR along with their case studies.

Unit IV: Congestion Avoidance
TCP slow start and congestion avoidance, TCP traffic behavior in a trial drop scenario, REDproactive queue management for congestion avoidance, WRED, flow WRED, ECN, SPD along with their case studies.

Unit V: QOS in MPLS-Based Networks
MPLS, MPLS with ATM, MPLS QoS, MPLS VPN, MPLS VPN QoS along with their case studies. traffic engineering; MPLS traffic engineering, the layer 2 overlay model, RRR, TE trunk definition, TE tunnel attributes, link resource attributes, distribution of link resource information, path selection policy, TE tunnel setup, link admission control, TE path maintenance, TE RSVP, IGP routing protocols, TE approaches along with their case studies.

Text Books:
[1] Srinivas Vegesna, “IP Quality of Service,” CISCO PRESS, 2001.
[2] Santiago alvarez, “Qos for IP/MPLS Networks,” Cisco Press, Pearson Education, 2006.

References:
1. IETF website: www.ietf.org

MULTIMEDIA TECHNIQUES			
Course Code:	**CS553/CS653**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit-I: Introduction
Introduction to Multimedia, Multimedia Information, Multimedia Objects, Multimedia in business and work. Convergence of Computer, Communication and Entertainment products.

Stages of Multimedia Projects
Multimedia hardware, Memory & storage devices, Communication devices, Multimedia software's, presentation tools, tools for object generations, video, sound, image capturing, authoring tools, card and page based authoring tools.

Unit-II: Multimedia Building Blocks
Text, Sound MIDI, Digital Audio, audio file formats, MIDI under windows environment Audio & Video Capture.

Unit-III: Data Compression
Huffman Coding, Shannon Fano Algorithm, Huffman Algorithms, Adaptive Coding, Arithmetic Coding Higher Order Modeling. Finite Context Modeling, Dictionary based Compression, Sliding Window Compression, LZ77, LZW compression, Compression, Compression ratio loss less & lossy compression.

Unit-IV: Speech Compression & Synthesis
Digital Audio concepts, Sampling Variables, Loss less compression of sound, loss compression & silence compression.

Unit-V: Images
Multiple monitors, bitmaps, Vector drawing, lossy graphic compression, image file formatting animations Images standards, JPEG Compression, Zig Zag Coding, Multimedia Database .Content based retrieval for text and images, **Video:** Video representation, Colors, Video Compression, MPEG standards, MHEG Standard Video Streaming on net, Video Conferencing, Multimedia Broadcast Services, Indexing and retrieval of Video Database, recent development in Multimedia.

Reference:
[1] Tay Vaughan: Multimedia, Making IT Work, Osborne McGraw Hill.
[2] Buford: Multimedia Systems, Addison Wesley.
[3] Agrawal & Tiwari: Multimedia Systems, Excel.
[4]Mark Nelson: Data Compression Book, BPB.
[5] David Hillman: Multimedia technology and Applications, Galgotia Publications.
[6] Rosch: Multimedia Bible, Sams Publishing.
[7] Sleinreitz: Multimedia System, Addison Wesley.
[8] James E Skuman: Multimedia in Action, Vikas.

SOFT COMPUTING			
Course Code:	**CS551/CS651**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fuzzy Logic
Introduction to fuzzy logic, classical and fuzzy sets, overview of fuzzy sets, membership function, fuzzy rule generation, operations on fuzzy sets: compliment, intersection, union, combinations on operations, aggregation operation.

UNIT II: Fuzzy Arithmetic
Fuzzy numbers, linguistic variables, arithmetic operations on intervals & numbers, uncertainty based information, information and uncertainty, no specificity of fuzzy and crisp sets, fuzziness of fuzzy sets.

UNIT III: Neural Network
Overview of biological neurons, computational neuron, mathematical model of neurons, ANN architecture, single layer and multilayer architectures, activation function, threshold value, self learning and forced learning algorithms, feed forward and feedback architectures.

UNIT IV: Learning Fundamentals
Learning paradigms, supervised and unsupervised learning, reinforced learning, ANN
training, algorithms perceptions, training rules, delta, back propagation algorithm, multilayer perception model, Hopfield networks, associative memories, applications of artificial neural networks,

UNIT V: Genetic Algorithms
History of genetic algorithm, terminology of genetic algorithm, biological background, creation of offspring, working principles of genetic algorithms, fitness function, reproduction: Roulette wheel selection, Boltzmann selection, cross over mutation, inversion, deletion, and duplication, generation cycle.
Concept of Uncertainty
Presence of uncertainty in real world problems, handling uncertain knowledge, degree of belief, degree of disbelief, uncertainty and rational decisions, decision theory, utility theory, concept of independent events, Bay's rule, using Bay's rule for combining events.

References:
[1] Peteus J. Braspenning: Artificial Neural Networks: An introduction to ANN Theory and Practice, PHI publication, 2005.
[2] Paul P. Wang: Fuzzy Logic: A spectrum of Theoretical and Practical issues, Pearson publication 2004.
[3] Lotfi Asker Zadeh, George J. Kilr, Bo Yuan Fuzzy: Sets, Fuzzy logic, and Fuzzy Systems: Selected Papers-, 2005.
[4] Foundations of Fuzzy logic and Soft Computing: 12th International Fuzzy conference proceeding, 2005.
[5] Particia Melin: Neural Networks Theory, Oxford University press, 2003
[6] Oscar Castillo: Neural Networks Theory and Application, Wiley Eastern publication 2003.

WIRELESS SYSTEM DESIGN			
Course Code:	**EC534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
RF system design procedures, methodology, link budget, propagation models, tower-top amplifiers, RF design guidelines, traffic projections, cell site design,

Unit II:
Network design- traffic forecasts, node dimensioning, interface design, placement of network nodes, topology

Unit III:
Antenna systems,-base station antenna, cross pole antenna, dual band antenna, intelligent antenna, diversity techniques-derivation of selection diversity and maximal ratio combining improvement, polarization diversity, frequency diversity, time diversity, RAKE receiver

Unit IV:
UMTS system design-design principles, coverage analysis, capacity analysis, radio access networks, overloading UMTS over GSM, CDMA system design-design methodology, deployment guidelines, traffic estimation, radio elements, fixed network d4sign requirements, traffic models, link budget, case studies-CDAM2000 1xRTT, EVDO, CDMA2000 1xRTT with EVDO overlay

Unit V:
Communication sites-types, installation, towers, stealth, in-building and tunnel systems, inter, modulation, collocation, Study of various network simulators, GloMoSim, ns-2, Opnet, designing and evaluating performance of transport and routing protocols of mobile and wireless networks.

Text Books:
[1] Clint Smith, P.E. Daniel Collins: 3G Wireless Networks" Tata McGraw-Hill, 2nd Edition
[2]Theodore S. Rappaport: Wireless Communication, Principles and Practice" Pearson

References:
IEEE Journals and proceedings

OPEN SOURCE SOFTWARE SYSTEM			
Course Code:	**CS404/CS534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Open Source Software (OSS)

History, philosophy, ethics, licensing, Pernes' principle, open source software methodology, open source vs. closed source, open source software vs. free software, open source software vs. source available, Windows and Linux, open source standards, open source development environment, OSS in e-government, OSS management, OSS management tools: taskjuggler, dotProject.net, licenses, open source content management system, project management via open source and open standard, copyright, patent, social dynamic of collaboration and legal implication of software intellectual property.

UNIT II: Open Source Technology and Infrastructure

Operating system: Linux, Berkeley Software Distribution (BSD); protocols: low level protocols, high level protocols; common open source language: presentation language, system programming languages, scripting languages; database system: MYSQL, PostgreSQL, BerkeleyDB; web services: Apache; communication servers: send mail, jabber; application and messaging server: Open3.org, Enhydra.org, JBoss, Zope, Zend, Open Source Desktop and server Applications.

UNIT III: Open Source Standards

Standards, open standards, benefits of open standards, national considerations, standard setting organization and processes, open standard organization for internet networking and application/services, computer graphics and multimedia, office documents, open standards usage, Linux standard base, Linux standard base as an ISO standard, Linux standards base certification, patents in standards.

UNIT IV: Open Source Software Applications

Rapid web application development framework: Ruby on Rail (ROR), Model-View-Controller (MVC) model, Don't Repeat Yourself (DRY) principle, convention over configuration principle, open source applications - business applications: Enterprise Resource Planning (ERP), Customer Relationship Management (CRM); educational applications: educational suites, learning support, language,; groupware: Content Management Systems (CSM), Wiki software; programming language support: bug trackers, code generators, configuration software.

UNIT V: Open Source in the Enterprise

Modern era of open source, rebranding open source, character of the community, open source community development, open source and enterprise applications, risks and benefits of using open source in the enterprise, developing an enterprise application strategy, cost, licensing and resources of OSS.

References:

[1] O'Reilly Media, Dan Woods: Open Source for the Enterprise: Managing Risks, Reaping Rewards,, 2005.
[2] James Lee, Brent Ware: Open Source Web Development with LAMP, Pearson Education, 2008.
[3] Paul Kavanagh: Open Source Software: Implementation and Management, Digital Press, 2004.
[4] Steven Weber: The Success of Open Source, Harvard University Press, 2004.

DESIGN OF SEMICONDUCTOR MEMORIES			
Course Code:	**EC568**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: RAM Technologies
Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs, DRAMs Cell Theory

UNIT II: Non Volatile Memories
Masked Read-Only Memories, High Density ROMs, PROMs, CMOS PROMs, EEPROMs, Floating-Gate EPROM Cell, Electrically Erasable PROMs, EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories, Advanced Flash Memory Architecture.

UNIT III: Memory Testing
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.

UNIT IV: Reliability and Radiation Effects
General Reliability Issues, RAM Failure Modes and Mechanics, Nonvolatile Memory Reliability, Reliability Modeling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, RAM Fault Modeling, Electrical Testing, Psuedo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling.

UNIT V: Packaging Technologies
Radiation Effects, Single Event Phenomenon, Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimeter, Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories, GaAs FRAMs, Analog Memories, Magnetoresistive Random Access Memories

Text Books:
[1] Ashok K. Sharma: Semiconductor Memories Technology, Testing and Reliability, Prentice-Hall of India Private Limited, New Delhi, 1997.
[2] Tegze P. Haraszti: CMOS Memory Circuits, Kluwer Academic publishers, 2001.

PRINCIPLES OF MEMS DESIGN			
Course Code:	**EC570**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II: Mechanics for MEMS Design
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III: Electrostatic Design
Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV: Circuit and System Issues
Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Capacitive Accelerometer, Piezoelectric pressure sensor, Modeling of MEMS systems, CAD for MEMS.

UNIT V: Introduction to Optical and RF MEMS
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

Text Books:
[1] Stephen Santuria: Microsystems Design, Kluwer publishers, 2000.
[2] Nadim Maluf: An introduction to Micro electro mechanical system design, Artech House, 2000.

References:
[1] Mohamed Gad-el-Hak: The MEMS Handbook, CRC press Baco Raton,2000.
[2] Tai Ran Hsu: MEMS & Micro systems Design and Manufacture Tata McGraw Hill, New Delhi, 2002.

SOLID STATE ELECTRONICS DEVICES			
Course Code:	**EC572**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fundamental Models
Physical models-bohr model, quantum mechanics, atomic structure, energy bands & charge carriers in semi conductors, carrier concentration, drift of carriers in electric and magnetic fields, diffusion of carriers. Continuity equation. Semi-conductor materials. Introduction to solid state electronics.

UNIT II: Diodes
Fabrication of P-N junctions, equilibrium conditions, forward and reverse biased junctions, steady state conditions, reverse bias breakdown, transient and a.c. condition, Recovery time, deviation from simple theory, metal semi-conductor junction, heterojunction. P-N junction linearly graded and step junction diodes, tunnel diode, photo diode, light emitting diodes and lasers.

UNIT III: BJTs
BJT amplification & switching: Fundamental of BJT operation, minority carier distribution & terminal currents, generalized biasing, switching, frequency limitation of transistors, ebber Molls model, Gummel Poon Model of BJTs. Heterojuction bipolar transistor.

UNIT IV: FETs
FET-metal semi-conductor (MESFETs), FET-Metal insulator semiconductor (MOSFET). Power MOSFETs, MODFETs, High Electron Mobility Transistors.

UNIT V: Integrated circuits
Monolithic device elements, charge transfers devices, very large scale integration, testing of VLSI chips, Stuck at faults and Fault diagnosis.

Text Book:
[1] Ben G Streetman, Solid State Electronic Devices PHI

References:
[1] S M Sze: Physics of semiconductor Devices, Wiley Pub.
[2] Kittel C: Introduction to Solid State Physics, Wiley Pub.

INTEGRATED CIRCUIT PHYSICAL DESIGN			
Course Code:	**EC574**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: The Well
Substrate, Parasitic Diode, N-well as a Resistor, N-well patterning and layout, Design Rules, Resistance calculation, N-well Resistor, N-well/Substrate Diode, Carrier Concentrations, Fermi Energy Level, Depletion Layer Capacitance, Storage or Diffusion Capacitance, RC Delay through the N-well, Distributed RC Delay, Distributed RC Rise Time, Twin Well Processes.

Unit II: The Metal Layers
Bonding Pad and layout, Metal-to-Substrate capacitance, Passivation, Design and Layout of Metal Layers, Metal1 and Via1, Parasitic Associated with Metal Layers, Intrinsic Propagation Delay, Current-Carrying Limitations, Design Rules for Metal Layers, Contact Resistance, Crosstalk and Ground Bounce , Crosstalk, Ground Bounce, DC Problems, AC Problems.

Unit III: The Active and Poly Layers
Layout Using Active and Poly Layers, P- and N-Select Layers, Poly Layer, Self-Aligned Gate, Poly Wire, Silicide Block, Connecting Wires to Poly and Active, Connecting P-Substrate to Ground, N-Well Resistor layout, NMOS and PMOS Device layout, Standard Cell Frame, Design Rules, Electrostatic Discharge (ESD) Protection, Diodes layout.

Unit IV: Resistors, Capacitors, MOSFETs
Resistors, Temperature Coefficient, Voltage Coefficient, Unit Elements, Guard Rings, Interdigitated Layout, Common- Centroid Layout, Dummy Elements, Poly-Poly Capacitor layout, Parasitic, MOSFETs: Lateral Diffusion, Oxide Encroachment, Source/Drain Depletion Capacitance, Source/Drain Parasitic Resistance, Long-Length MOSFETs layout, Large-Width MOSFETs layout, MOSFET Capacitances.

Unit V: MOSFET Operation
Accumulation, Depletion, Strong Inversion, Threshold Voltage, Characteristics of MOSFETs, MOSFET Operation: Triode and Saturation, Cgs Calculation, Long-Channel MOSFET Models, Model Parameters Related to the Drain Current, Modeling of the Source and Drain Implants Short-Channel MOSFETs Hot Carriers, Lightly Doped Drain, MOSFET Scaling, Short-Channel Effects, Oxide Breakdown, Drain-Induced Barrier Lowering, Gate-Induced Drain Leakage.

Text Books:
[1] R. Jacob Baker: CMOS Circuit Design, Layout, and Simulation, Second Edition.
[2] Christopher Saint, Judy Saint: IC Layout Basics: A Practical Guide

References:
[1] Dan Clein: CMOS IC Layout : Concepts, Methodologies, and Tools,.
[2] Alan Hastings, Roy Alan Hastings: The Art of Analog Layout

CMOS RF CIRCUIT DESIGN			
Course Code:	**EC576**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF design and Wireless Technology
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

UNIT II: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

UNIT III: RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT V: RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text Book:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University press 1998.

References:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce CMOS Circuit Design, layout and Simulation PHI, 1998
[3] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996

CMOS VLSI DESIGN			
Course Code:	**EC578**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor theory
nMOS / pMOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT II: CMOS Process Technology
Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT III: Basics of Digital CMOS Design
Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques.

UNIT IV: CMOS Analog Design
Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

UNIT V: Dynamic CMOS and clocking
Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking-clock generation, clock distribution, clocked storage elements.

Text Books:
[1] Neil Weste and K. Eshragian: Principles of CMOS VLSI Design: A System Perspective, 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
[2] Wayne, Wolf: Modern VLSI design: System on Silicon, Pearson Education, 2nd Edition

References:
[1] Douglas A Pucknell & Kamran Eshragian: Basic VLSI Design, PHI, 3rd Edition
[2] Sung Mo Kang & Yosuf Lederabic Law: CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 3rd Edition

VLSI DESIGN TECHNIQUES			
Course Code:	**EC580**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor Theory and Process Technology
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II: Inverters and Logic Gates
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III: Circuit Characterization and Performance Estimation
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing ,Scaling.

UNIT IV: VLSI System Components Circuits and System Level Physical Design
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V: Verilog Hardware Description Language
Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modelling, data flow modeling, behavioral modeling, task & functions, Test Bench.

Text Books:
[1] Neil H.E. Weste and Kamran Eshraghian: Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
[2] John P.Uyemura: Introduction to VLSI Circuits and Systems, John Wiley & Sons, Inc., 2002.
[3] Samir Palnitkar: Verilog HDL, Pearson Education, 2nd Edition, 2004.

References:
[1] Eugene D.Fabricius: Introduction to VLSI Design McGraw Hill International Editions, 1990.
[2] J.Bhasker, B.S.Publications: A Verilog HDL Primer, 2nd Edition, 2001.
[3] Pucknell: Basic VLSI Design, Prentice Hall of India Publication, 1995.
[4] Wayne Wolf: Modern VLSI Design System on chip, Pearson Education, 2002

ADVANCED RF ENGINEERING			
Course Code:	**EC544**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF Electronics
Introduction to RF Design and Wireless Technology: Design and Applications,

UNIT II: Complexity and Choice of Technology
Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion

UNIT III: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direct conversion and two-step transmitters. RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation Overview of RF Filter design, Active RF components & modeling,

UNIT V: RF Circuits Design
Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text books:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce: CMOS Circuit Design, layout and Simulation, PHI, 1998.

References:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University Press, 1998.
[2] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996
[3] David M. Pozar: Microwave Engineering, John Wiley & Sons, 2nd Edition, 2003.

PROBABILITY AND STOCHASTIC PROCESSES			
Course Code:	**EC548**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:

Probability models, Algebra of events, probability axioms, conditional probability, Baye's rules, Bernoulli traits. **Discrete Random Variables**: Discrete random variables, probability mass functions, discrete distribution functions-Bernoulli, Binomial, geometric, Poisson, hyper geometric & uniform distributions, probability generating function.

Unit II:

Continuous Random variable: Exponential distribution, memory less property, application to reliability, hypo exponential, Erlang, Gamma, hyper exponential & Normal distributions ,order statistics, distribution of sums.

Unit III:

Stochastic Process, Classification, Discrete and continuous time markov chain, Poisson process, renewal process, littles's formula, Erlang Loss Model, M/M/1 Queue, M/M/m Queue Multidimensional Queue.

Unit IV:

Solution Techniques: Steady-State Solutions of Markov Chains, Solution for a Birth Death Process, Matrix-Geometric Method: Quasi-Birth-Death Process, Heisenberg Matrix: Non-Markovian Queues, Transient analysis, stochastic Petri nets, Numerical Solution: Direct Methods, Numerical Solution: Iterative Methods, Comparison of Numerical Solution Methods, Performance Measures,

Unit V:

Queueing Networks. Definitions and Notation. Performance Measures. Product-Form Queueing Networks. Algorithms for Product-Form Networks, priority Networks.

Reference Books:

[1] Research Methodologies, R. Panneerselvam, Prentice Hall, 2007.
[2] Research in Education, Best John V. and James V Kahn, Wiley eastern, 2005.
[3] Elements of Educational Research, Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra, PHI publication, 2003.
[4] Methodology of Research Education, K. Setia, IEEE publication, 2004.
[5] Research methodology, Methods and Techniques, Kothari, C.R., 2000.

ADVANCED MICROWAVE COMMUNICATION			
Course Code:	**EC550**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Microwave and Millimeter Wave Devices
Overview of microwave and millimeter wave vacuum tube devices, limitations of microwave vacuum tubes, gyratron vacuum tube devices. Advances in microwave and millimeter wave solid state devices, Gunn devices, oscillator using, Gunn diode, and injection locked oscillators, IMPATT devices, and microwave and mm wave performance of IMPATT. Other solid state devices like Tunnel diode, BARITT and TRAPAT. Microwave and mm wave circuits.

UNIT II: Microwave and MM Wave Circuits
Review of scattering matrix concept in the light of vector network analyzer, impedance matching network, couplers, power dividers, resonators and filters, Detectors, mixers, attenuators, phase shifters, amplifier and oscillator, Ferrite based circuits.

UNIT III: Antennas
Hertzian dipole, loop antenna, helical antenna, frequency independent antenna: Du0Hamel principle, log spiral and log periodic dipole antenna array. Babinet principle, waveguide slot antenna, microstrip antenna, horn antenna, parabolic reflector. Antenna arrays and phased array antenna.

UNIT IV: Satellite Communication
Orbital parameters, satellite trajectory, period, geostationary satellites, non-geostationary constellations. Communication satellites – Space craft subsystems, payload – repeater, antenna, attitude and control systems, telemetry, tracking and command, power sub system and thermal control. Earth stations antenna and feed systems, satellite tracking system, amplifiers, fixed and mobile satellite service earth stations. Terrestrial: line of sight transmission, relay towers and distance considerations. Communication link design: Frequency bands used, antenna parameters, transmission equations, noise considerations, link design, propagation characteristics of fixed and mobile satellite links, channel modeling, very small aperture terminals (VSAT), VSAT design issues.

UNIT V: Microwave and MM Wave Propagation.
Overview of basic radio wave propagation mechanisms, Friis transmission formula, plane earth propagation model, troposcatter systems, ionosphere propagation, duct propagation, microwave radio link and calculation of link budget. Effect on radio wave propagation due to rain, fog, snow, ice, atmospheric gases, Earth's magnetic field.

Text Books:
[1] David M Pozar: Microwave Engineering, John Wiley & Sons
[2] R E Collin, Antenna & Radio wave Propagation, McGraw Hill Book Co.

References:
[1] M Richharia: Satellite Communication Systems,2nd Edition, Macmillan Press Ltd.
[2] Ferdo Ivanek: Terrestrial Digital Microwave Communications, Artech House
[3] E. Hund: Microwave Communications, IEEE Press
[4] Jordan & Balman: Electromagnetic waves & Radiating System
[5] R E Collin: Microwave Engineering, McGraw Hill Co.

IMAGE PROCESSING AND BIOMETRICS			
Course Code:	**EC418/EC556**	**Credits:**	**3**

No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Image Processing and Image Enhancement
Introduction, An image model, sampling & quantization, Basic relationships between Pixels, imaging geometry, Properties of 2 – D Fourier transform, FFT algorithm and other separable image transforms, Components of an image processing System., Digital Image Fundamentals- elements of visual perception, image sensing and acquisition, Basic relationships between pixels
Fundamentals of spatial filtering, smoothing spatial filters (linear and non-linear).

Unit II: Pattern Recognition
Fundamentals of Pattern Recognition, Recognition Measurement, Errors, and Statistics, Recognition measurement and testing, Identification System Errors and Performance Testing, Computer Security, Bayesian decision theory, Multilayer neural networks, Unsupervised Learning and Clustering.

Unit III: Biometrics
Introduction to Biometrics, Fingerprints: Ridges, Furrows, Types of Fingerprints, Image and Signal Processing, Biometric Signal Processing, Other Biometric Modalities, Comparing Biometrics, Passwords, and Tokens, Multimodal Biometrics, Biometric Resources and Standards, Large Scale Biometrics and Systems Case Studies.

Unit IV: Analysis in Biometrics
Large-Scale Biometric Identification: Challenges and Solutions, Issues Involving the Human Biometric Sensor Interface, Fundamentals of Biometric-Based Training System Design, Biometric Systems and Applications, Force Field Feature Extraction for Fingerprint Biometrics, Behavioral Biometrics for Online Computer User Monitoring.

Unit V: Synthesis in Biometrics:
Introduction to Synthesis in Biometrics, Local B-Spline Multiresolution with Example in Iris Synthesis and Volumetric Rendering, image smoothing filters (Butterworth and Guassian low pass filters), image sharpening filters (Butterworth and Guassian high pass filters), selective filtering, Computational Geometry and Image Processing in Biometrics: On the Path to Convergence, **,** A Statistical Model for Biometric Verification.

Text Books:
[1] Practical Algorithms for Image Analysis: Description, Examples, and Code, Seul, O'Gorman, Sammon, 2000.
[2] S. Annadurai and R. Shanmugalakshmi: Fundamentals of Digital Image Processing, Pearson Education.
[3] R. C. Gonzalez and R. E. Woods: Digital Image Processing, 3rd Edition, Pearson Education.
[4] A. K. Jain: Fundamentals of Digital Image Processing, PHI Learning.
References:
[1] M. Sonka, V. Hlavac and R. Boyle: Digital Image Processing and Computer Vision: Cengage Learning.
[2] B. Chanda and D. D. Majumder: Digital Image Processing and Analysis, PHI Learning.
[3] S. Jayaraman, S. Esakkirajan and T. Veerakumar: Digital Image Processing, TMH.

ADVANCED COMMUNCIATION NETWORKS			
Course Code:	**EC402/EC532**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Digital switching systems-analysis, hierarchy, evolution, SPC, call processing, communication and control- level 1,2,& 3 control, interface control, network control processor, central processor, control architecture, multiplexed highways, switching fabric-space division switching, time division switching, STS, TST, TTT, switching system software-architecture, OS, database management

Unit II: MPLS-label stack and label distribution, traffic engineering, design of switching systems, and routers, switching networks-crossbar switches, multistage switches, shared memory switches, optical networks, DWDM techniques, IP over optical core switches

Unit III: Congestion control: integrated services, differentiated services, congestion control, congestion control in packet switching, frame relay congestion control, flow control at link level, TCP congestion control

Unit IV: Voice over IP: basic IP telephone system, digital voice sampling, compression techniques, protocol for VoIP, session initiation protocol

Unit V: Internetworking-connection mode network service, x.75 internetworking, network through ISDN, internetworking SNA, and x.25, x.300 internetworking standards, personal computer networking, data transmission in PTN, Data network standards, voice-data integration, fast packet switches

Text books:

[1] Syed R. Ali, " Digital Switching Systems, System Reliability and analysis, Tata McGraw-Hill
[2] William Stallings, " High Speed Networks and Internet" 2nd ed. Perason edu, 2005
[3] Bellamy John, " Digital Telephony" Wiley 3rd Ed, 2000
[4] Viswanathan, T, "Telecommunications Switching Systems and Networks, " PH

References:

[1] Andrew S. Tanenbaum: Computer networks, PHI.
[2] W. Stallings: Data and computer communications, MC, Milan.
[3] Alberto Leon-Gercia, India Widjaja: Communication networks, fundamental concepts and key architecture, TATA McGraw Hill.
[4] Bertsekas D. and Gallager R.: Data Networks, PHI.
[5] Keshav S: An Engineering Approach to computer Networking, Addison Weslay.

LOW POWER VLSI DESIGN			
Course Code:	**EC633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

UNIT II: Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III: Power estimation

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT IV: Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT V: Low power Architecture & Systems

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text Books:

[1] Gary K. Yeap: Practical Low Power Digital VLSI Design, KAP, 2002
[2] Rabaey and Pedram: Low power design methodologies, Kluwer Academic, 1997

References :

[1] Kaushik Roy, Sharat Prasad: Low-Power CMOS VLSI Circuit Design, Wiley, 2000
[2] J. B. Kulo and J.H Lou: Low voltage CMOS VLSI Circuits, Wiley 1999.
[3] A.P. Chandrasekaran and R.W. Broadersen: Low power digital CMOS design, Kluwer, 1995.
[4] Abdelatif Belaouar, Mohamed.I. Elmasry, “Low power digital VLSI design, Kluwer, 1995.

DESIGN LAB III			
Course Code:	**EC683**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to simulation software ANSYS using GUI.
2. Introduction to simulation software ANSYS using Command lines.
3. Performing a Harmonic Response Analysis using ANSYS.
4. Realization of a Force Sensor using ANSYS.
5. Multiphysics Analysis of a Thermal Actuator using ANSYS.
6. Piezoelectric Analysis using ANSYS.
7. Introduction to MEMS Design using ANSYS.
8. Electromechanical Analysis of an Optical Brag Reflector using ANSYS.

RESEARCH TECHNIQUES IN ICT			
Course Code:	**CS633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I : Introduction to Research Techniques
Meaning of research, objectives of research, motivation in research, types of research-Introduction to experimental test bed, algorithmic research, simulation research, mathematical modeling approach, characteristics and prerequisites of research, significance of research, research process, Sources of research problem, criteria of identifying the problem, necessity of defining the problem, errors in selecting research problem, technique involved in defining the problem, Report and paper writing

Unit II: Data Analysis and Statistical Techniques
Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminant analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis.

Unit III: Random Numbers and Variates
Properties of random numbers, generation, tests for random numbers, random-variate generation
Inverse Transform technique, direct transformation, convolution method, acceptance-rejection Technique, Probability distributions functions, Moments, moment generating functions, joint distributions, marginal and conditional distributions, functions of two dimensional random variables Poisson process-Markovian queues, single and multi server models, Little's formula, steady state analysis

Unit IV: Algorithmic Research
Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments,

Unit V: Simulation and Soft Computing Techniques
Introduction to soft computing, Artificial neural network, Genetic algorithm, Fuzzy logic and their applications, Tools of soft computing, Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, verification of simulation models, calibration and validation of models, Output analysis, introduction to MATLAB, NS2, ANSYS, Cadence

Text Books:
[1] R. Panneerselvam: Research Methodologies, PHI
[2] Jerry Banks, John S. Carson, Barry.L. Nelson David. M. Nicol: Discrete-Event System Simulation, Prentice-Hall India
[3] Donald Gross, Carl M. Harris: Fundamentals of Queueing Theory, 2nd Ed. John Wiley and Sons, New York,

References:
[1] Best John V. and James V Kahn: Research in Education, Wiley eastern, 2005.
[2] Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra: Elements of Educational Research, PHI publication, 2003.
[3] K. Setia: Methodology of Research Education, IEEE publication, 2004.
[4] Kothari, C.R.: Research methodology, Methods and Techniques, 2000.

VLSI ASIC DESIGN			
Course Code:	**EC665**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I : Introduction to ASICs, CMOS Logic and ASIC Library Design
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II: Programmable ASICs, Programmable ASIC Logic Cells and ASICs I/O Cells.
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III: Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV: Logic Synthesis, simulation and Testing
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation- boundary scan test - fault simulation - automatic test pattern generation.

UNIT V: ASIC Construction, Floor Planning, Placement and Routing
System partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC.

Text Books:
[1] M.J.S .Smith, Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
[2] Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.

References:
[1] Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
[2] R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House, 2000.

MICRO AND SMART SYSTEM TECHNOLOGY			
Course Code:	**EC667**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT 1: Introduction to Micro and Smart Systems
Smart-material systems, Evolution of smart materials, structures and systems, Components of a smart system, Application areas, Commercial products, Microsystems, Feynman's vision, Micromachined transducers, Evolution of micro-manufacturing, Applications.

UNIT II: Micro and Smart Devices and Systems: Principles and Materials:
Microsensors, silicon capacitive accelerometer, resonant accelerometer, piezo-resistive pressure sensor, capacitive pressure sensor, inertial sensor, sensor for munitions, microresonator, tunable rf filters, actuators, , microvalve/micropumps, microactuator, microgripper, detectors, flow sensor, accelerometer, gyros sensor, enhanced jet engine, chemical sensor, biosensors, DNA chips, micro thruster, CNT.

UNIT III: Micromanufacturing and Material Processing
Materials: types, mechanical properties, electronics properties and optical properties. Processing of other materials: ceramics, polymers and metals, silicon wafer processing, lithography, nanolithography, micro contact printing lithography, thin-film deposition, etching (wet and dry), TMAH etching, LIGA, laser ECE, wafer-bonding, and metallization, Silicon micromachining: surface, bulk, moulding, bonding based process flows, Thick-film processing, Smart material processing, Emerging trends.

UNIT IV: Modeling, Design and Simulations
Scaling issues, Elastic deformation and stress analysis of beams and plates, Residual stresses and stress gradients, Thermal loading, Heat transfer issues, Basic fluids issues, Electrostatics. Coupled electromechanics. Electromagnetic actuation, Capillary electro-phoresis. Piezoresistive modeling, Piezoelectric modeling. Magnetostrictive actuators,finite element method overview.

UNIT V: Advanced Topic
Micro and smart system based switches for RF and Microwave applications, inductors and capacitors, RF filters, phase shifters, transmission lines and components, antenna, integration and packaging.

Text Books:
[1] MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill.
[2] RF MEMS and their applications, V.Varadan, K. J. Vinoy, K.A. Jose, Wiley.

References:
[1] Microsystems Design, S. D. Senturia, Kluwer Academic Publishers, 2001.
[2] Analysis and Design Principles of MEMS Devices, Minhang Bao, Elsevier
[3] Design and Development Methodologies, Smart Material Systems and MEMS: V. Varadan, K. J. Vinoy, S. Gopalakrishnan, Wiley.
[4]MEMS- Nitaigour Premchand Mahalik, TMH 2007

ADVANCES IN VLSI DESIGN			
Course Code:	**EC669**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.MESFET and MODFET operations, quantitative description of MESFETS.MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

UNIT II: Short channel effects and challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

UNIT III: Beyond CMOS
Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing.

UNIT IV : Super buffers, Bi-CMOS and Steering Logic
Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

UNIT V: Special circuit layouts & technology mapping and System Design
Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out. CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

Text Books:
[1] Kevin F Brrnnan Introduction to semi conductor device, Cambridge Publications
[2] Eugene D Fabricius Introduction to VLSI design, McGraw-Hill International Publications

References:
[1] D.A Pucknell Basic VLSI design, PHI Publication
[2] Wayne Wolf, Modern VLSI Design Pearson Education, Second Edition, 2002

MODERN OPTIMIZATION TECHNIQUES			
Course Code:	**EC671**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Artificial Neural Networks (ANN)
Objectives-History-Biological inspiration, Neuron model, Single input neuron, Multi-input neuron, Network architecture, Single layer of neurons, Multi-layers of Neurons.

UNIT II: Perceptron and Learning
Perceptron architecture, Stingle-neuron perceptron, Multi-neuron perceptron- Perceptron Learning Rule, Constructing learning rules, Training multiple neuron perceptrons. Associative Learning: Simple associative network, Unsupervised Hebbrule- Hebb rule with decay, Instar rule, Kohonen rule. Widro-Hoff Learning: Adaline Network, Single Adaline, Mean square Error, LMS algorithm, Analysis of Convergence.

UNIT III: Neural Network Roles in VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Time Series and Forecasting.

UNIT IV: Genetic Algorithms and its Mathematical Foundations
Introduction, robustness of traditional optimization and search methods, goals of optimization, difference between genetic algorithms and traditional methods, a simple genetic algorithm, hand simulation, Grist for the search mill, similarity templates, learning the lingo. Foundation theorem, schema processing, the two armed and k-armed bandit problem, schemata processing, building block hypothesis, minimal deceptive problem (MDP), extended schema analysis, MDP results, similarity templates as hyper planes.

UNIT V: Advanced Topics
Data structures, reproduction, crossover and mutation, a time to reproduce and a time to cross, main program and results, mapping objective functions to fitness form, fitness scaling, codings, a multiparameter mapped fixed point coding, discretization, constraints.

Text Books:

[1] Neural Network Design, PWS publishing company, 1995.
[2] Introduction to Artificial Neural Systems, Jaico Pub.House, Bombay, 1994.
[3] Neural Computing : Theory and practice, Van Nastrand Reinhold, 1989.

References

[1] Haykin S., Neural Networks-A Comprehensive Foundations, Prentice-Hall International, New Jersey, 1999.
[2] Freeman J.A., D.M. Skapura, Neural Networks: Algorithms, Applications and Programming Techniques, Addison-Wesley, Reading, Mass, (1992).
[3] Golden R.M., Mathematical Methods for Neural Network Analysis and Design, MIT Press, Cambridge, MA, 1996.

VLSI-RELIABILTY ENGINEERING			
Course Code:	**EC673**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Probability Plotting and Load- Strength Interference
Statistical distribution , statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II: Reliability Prediction, Modeling and Design
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III: Electronics and Software System Reliability
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV: Reliability Testing and Analysis
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V Manufacture and Reliability Management
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

Text Books:
[1] Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
[2] David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, AT & T Reliability Manual, 5th Edition, 1998.

Reference:
[1] Gregg K. Hobbs, Accelerated Reliability Engineering - HALT and HASS, John Wiley & Sons, New York, 2000.

SENSOR NETWORKS			
Course Code:	**EC647**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Sensor Network Operations
Overview of mission-oriented sensor networks, trends in sensor development, mission oriented sensor networks, dynamic systems perspective, Dense sensor networks, robust sensor positioning in wireless ad hoc sensor networks, trigonometric k clustering (TKC) for censored distance estimation, sensing coverage and breach paths in surveillance wireless sensor networks.

UNIT II: Lower Layer Issues-MAC, Scheduling, and Transmission
Medium access control for sensor networks, comprehensive performance study of IEEE 802.15.4, providing energy efficiency for wireless sensor networks, link adaptation techniques.

UNIT III: Network Routing
Load balanced query protocols for wireless sensor networks, energy efficient and MAC aware routing for data aggregation in sensor networks, ESS low energy security solution for large-scale sensor networks based on tree ripple zone routing scheme.

UNIT IV: Sensor Network Applications
Evader centric program, Pursuer centric program, hybrid pursuer evader program, efficient version of hybrid program, Implementation and simulation results

UNIT V: Embedded Soft Sensing for Anomaly Detection
Mobile robot simulation setup, software anomalies in mobile robotic networks, soft sensor, software anomaly detection architecture, anomaly detection mechanisms, test bed for software anomaly detection in mobile robot application, multisensor network-based framework; Basic model of distributed multi sensor surveillance system, super resolution imaging, optical flow computation, super resolution image reconstruction, experimental results.

Text Books:
[1] Sensor Network Operations, Shashi Phoha, Thomas F. La Porta , Chrisher Griffin, Wiley-IEEE Press March 2006.
[2] Wireless sensor networks, Jr. Edger H. Callaway, CRC Press.

References:
[1] Wireless Sensor Networks, I. F. Akyildiz and M. C. Vuran, John Wiley and Sons Publ. Company
[2] Wireless Sensor Networks: An Information Processing Approach, Feng Zho, Morgan Kaufmann

MIXED SIGNAL VLSI DESIGN			
Course Code:	**EC519/EC675**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Signals, Filters, and Tools
Sinusoidal Signals, Pendulum Analogy, Amplitude in the x-y Plane, In-Phase and Quadrature Signals, Complex (z-) Plane, Comb Filters, Digital Comb Filter, Digital Differentiator, Intuitive Discussion of the z-Plane, Comb Filters with Multiple Delay Elements, Digital Integrator, Delaying Integrator, Exponential Fourier Series, Fourier Transform, Dirac Delta Function .

Unit II: Sampling and Aliasing
Sampling, Impulse Sampling, Time Domain Description of Reconstruction, Decimation, Sample-and-Hold, S/H Spectral Response, Reconstruction Filter, Circuit Concerns for Implementing the S/H, Track-and-Hold (T/H), Interpolation, Zero Padding, Hold Register, Linear Interpolation, K-Path Sampling, Switched-Capacitor Circuits, Non-Overlapping Clock Generation, Circuits Implementing the S/H, Finite Op-Amp Gain-Bandwidth, Auto zeroing,

Unit III: Analog Filters
Integrator Building Blocks, Lowpass Filters, Active-RC Integrators, Effects of Finite Op-Amp Gain Bandwidth Product, Active-RC SNR, MOSFET-C Integrators, gm-C Integrators, Common-Mode Feedback Considerations, High-Frequency Transconductor, Discrete-Time Integrators, Frequency Response of an Ideal Discrete-Time Filter, Filtering Topologies, Bilinear Transfer Function, Active-RC Implementation, Transconductor-C Implementation.

Unit IV: Digital Filters
Models for DACs and ADCs, Ideal DAC, Modeling of Ideal DAC, Ideal ADC, Number Representation, Increasing Word Size, Adding Numbers and Overflow, Two's Complement Sinc-Shaped Digital Filters, Counter, Aliasing, Accumulate-and-Dump, Lowpass Sinc Filters, Averaging without Decimation, Cascading Sinc Filters, Finite and Infinite Impulse Response Filters, Bandpass and Highpass Sinc Filters, Frequency Sampling Filters.

Unit V: Data Converter SNR
Quantization Noise, Quantization Noise Spectrum, Bennett's Criteria, RMS Quantization Noise Voltage, Quantization Noise as a Random Variable, Quantization Noise Voltage Spectral Density, Power Spectral Density, SNR, Effective Number of Bits, Coherent Sampling, SNDR, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter.

Text Books:
[1] Jacob Baker, CMOS Mixed Signal Circuit Design, TMH

References:
[1] Yannis Tsividis ,"Mixed Analog-Digital VLSI Device and Technology", Wiley
[2] Roubik Gregorian ,"Introduction to CMOS Opamps and Comparators",TM

DSP INTEGRATED CIRCUITS			
Course Code:	**EC521/EC677**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: DSP Integrated Circuits and VLSI Circuit Technologies
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

Unit II: Digital Signal Processing
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

Unit III: Digital Filters and Finite Word length Effects
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

Unit IV: DSP Architectures and Synthesis of DSP Architectures
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Unit V: Arithmetic Units and Integrated Circuit Design
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

Text Books:
[1] Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
[2] A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.

References:
[1] Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
[2] Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

ADVANCED DIGITAL VLSI DESIGN			
Course Code:	**EC679**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Basic principle of MOSFETs, Introduction to large signal MOS models (long channel) for digital design. The MOS Inverters: Static and Dynamic characteristics: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, transition time, Propagation Delay, Power Consumption.

UNIT II: MOS Circuit Layout & Simulation
Layout design rules, MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation, Circuit Compaction; Circuit extraction and post-layout simulation.

UNIT III: Combinational MOS Logic Design
Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits, DSL, DCVSL, Transmission gate logic. Dynamic MOS design: Dynamic logic families and performances. Memory Design: ROM & RAM cells design

UNIT IV: Sequential MOS Logic Design
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Adders, Multiplier Circuits.

UNIT V: Interconnects & IO Buffers and BiCMOS Logic Circuits
Interconnect delays, Cross Talks. Introduction to low power design, Input and Output Interface circuits. BiCMOS Logic Circuits: Introduction, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits.

Text Books:
[1] Kang & Leblebigi CMOS Digital IC Circuit Analysis & Design- McGraw Hill, 2003
[2] J.M. Rabey, Digital Integrated Circuits Design, Pearson Education, Second Edition, 2003
[3] Weste and Eshraghian, Principles of CMOS VLSI design Addison-Wesley, 2002

Reference:
[1] W Wolf Modern VLSI Design.
[2] David A. Hodges, Horace G. Jackson, Resve Saleh, Analysis & Design of Digital Integrated Circuits, 3rd Edi Mc Graw Hill, 2003.

TEST AND VERIFICATION OF VLSI CIRCUITS			
Course Code:	**EC681**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Basic Concepts, Functional Modeling: Truth table and primitive cubes, Binary decision diagrams, Basic RTL constructs, Timing Modelling, Structural Modeling: External Representations Structural Properties, Internal representations, Wired Logic and bidirectionality.

UNIT II: Logic Simulation
Types of simulations, The unknown logic values, Complied simulation, Event driven simulation Delay Models for gates, Element Evaluation, Hazard Detection, Tristate Logic, MOS Logic, other delay models: Rise and Fall Delays, Inertial Delays, Ambiguous Delays, Oscillation Control.

UNIT III: Fault Modeling and Simulation
Logical Fault Models, Fault Detection and Redundancy: Combinational Circuits, Sequential Circuits, Fault Equivalence and Fault location: Combinational Circuits, Sequential Circuits, Fault Dominance, Single stuck Fault model, Multiple stuck at Fault model, General Fault Simulation Techniques: Serial Fault, Parallel Fault, Deductive Fault, Concurrent Fault, Fault Simulation for Combinational Circuits.

UNIT IV: Testing for Faults
Basic Issues, ATG for SSFs in Combinational Circuits: Fault Oriented ATG, Common Concepts, Algorithms, Selection Criteria, Fault Independent ATG, Random Test Generation, Combined Deterministic/Random Test Generation, ATG for single stuck at faults in sequential Circuits, Bridging Fault model, Detection of feedback and non feedback Bridging Faults.

UNIT V: Design for Testability
Testability: Tradeoffs, Controllability and Observability, Ad Hoc Design for Testability Techniques: Test points, Initialization, Monostable multivibarators, Oscillators and Clocks, Controllability and Observability by means of scan registers, Generic scan based designs.

Text Books:
[1] Digital Systems Testing & Testable Design, Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman.
[2] An Introduction to Logic Circuit Testing, Parag K Lala

REFERENCE BOOKS
[1] VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon), Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen.

EM INTERFERENCE AND CAPABILITIES IN SYSTEM DESIGN			
Course Code:	**EC661**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Basic EMC concepts at IC level
Introduction , Definition of EMC, EMI, EMS and EME, Sources of electromagnetic interference, Electromagnetism versus integrated circuit design, Electrical length, Near field versus far field, Radiation of a conductor , Basic EMC antenna concepts, Radiated, induced and conducted disturbances, Practical example, Intra-chip versus externally-coupled EMC, EMC in automotive applications.

UNIT II: EMC of Integrated Circuits and Distortion
Relationship between EMI resisting design and distortion , Linear distortion, Nonlinear distortion (rectification) , Weak and strong nonlinear distortion, diode connected NMOS transistor , NMOS source follower, NMOS current mirror, Capacitor decoupling the mirror node, Low-pass *R-C* filter in the mirror node , EMI resisting (4-transistor) current mirror , EMI resisting (Wilson totem pole) current mirror , Comparison of EMI susceptibility of current mirrors , EMI susceptibility in ESD protections.

UNIT III: EMI Resisting Analog output circuits
Categorization of analog output structures, Common-drain output circuits, Common-source output circuits, Comparing the electromagnetic susceptibility, Large EMI amplitudes, EMI resisting DC current regulator , EMI issues in a classic DC current regulator, EMI issues: small signal analysis large signal analysis, Decoupling capacitor *Cd* , DC current regulator with a high immunity to EMI Measurements.

UNIT IV: EMI Resisting Analog input circuits
Electromagnetic immunity of CMOS operational amplifiers, Asymmetric slew rate, Strong nonlinear behaviour of the input differential pair, Weak nonlinear behaviour of the input differential pair, EMI induced offset in a classic differential pair , Classic differential pair using source degeneration, Cross-coupled differential pair, Differential pair with low-pass *R-C* filter, Improved cross-coupled differential pair, Source-buffered differential pair, Comparison, EMI induced offset measurement setups, Measurements.

UNIT V: Advance Topics
CMOS bandgap voltage references with a high immunity to EMI, EMI injection in a bandgap reference, Small signal analysis, Large signal analysis, EMI resisting bandgap reference , Small signal analysis , Large signal analysis, EMI resisting bandgap reference, Small signal analysis, Large signal analysis, Startup circuit and biasing, Measurements.

Text Books:
[1] EMC of Analog Integrated Circuits, Jean-Michel Redoute, Michiel Steyaert

References:
[1] Electromagnetic compatibility of integrated circuits: techniques for low emissions and susceptibility, Sonia Ben Dhia, Mohamed Ramdani, Étienne Sicard.
[2] Electromagnetic Compatibility Engineering , Henry Ott.

ALGORITHM FOR VLSI DESIGN AUTOMATION			
Course Code:	**EC685**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction

Architectural Design , Logic Design, Physical Design , Full-custom Layout**,** Gate-array Layout, Standard-cell Layout Macro-cell Layout, Programmable Logic Arrays, FPGA layout**,** Difficulties in Physical Design, Problem Subdivision, Computational Complexity of Layout Subproblems, Solution Quality, Nets and Netlists, Connectivity Information, Weighted Nets, Grids, Trees, and Distances.

UNIT II: Circuit Partitioning and Floorplanning

Cost Function and Constraints: Bounded Size Partitions, Minimize External Wiring, Approaches to Partitioning Problem: Kernighan-Lin Algorithm, Variations of Kernighan-Lin Algorithm, Fiduccia Mattheyses Heuristic, Simulated Annealing, Floorplanning Model, Approaches to Floorplanning, Cluster Growth ,Simulated Annealing ,Analytical Technique , Dual Graph Technique.

UNIT III: Placement

Complexity of Placement , Problem Definition , Cost Functions and Constraints: Estimation of Wirelength, Minimize Total Wirelength , Minimize Maximum Cut , Minimize Maximum Density, Maximize Performance, Other Constraints, Approaches to Placement: Partition-Based Methods, Limitation of the Min-cut Heuristic, Simulated Annealing , Numerical Techniques.

UNIT IV: Routing

Problem Definition, Cost Functions and Constraints: Placement Constraints , Number of Routing Layers Geometrical Constraints, Maze Routing Algorithms: Lee Algorithm, Limitations of Lee Algorithm for Large Circuits ,Connecting Multi-point Nets ,Finding More Desirable Paths, Further Speed Improvements, Line Search Algorithms, Other Issues: Multi Layer Routing , Ordering of Nets , Rip-up and Rerouting, Power and Ground Routing.

UNIT V: Advanced Topics

Cost Functions and Constraints , Routing Regions: Routing Regions Definition, Routing Regions Representation, Sequential global Routing: The Steiner Bee Problem, Global Routing by Maze Running, Integer Programming ,Global Routing by Simulated Annealing : The First Stage , The Second stage, Hierarchical Global Routing.

Text Books:

[1] VLSI physical design automation: theory and practice, By Sadiq M. Sait, Habib Youssef.

[2] Algorithm for VLSI physical design automation by Naveed A. Sherwani.

References:

[1] Essential Electronic Design Automation (EDA), Mark D Birnbaum.

[2] Physical Design Automation for VLSI systems, Bryan D Ackland.

[3] Practical Problems in VLSI Physical Design Automation, Sung Ku Lim.

SMART ANTENNA SYSTEMS			
Course Code:	**EC643**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Basic Concepts of Radiation
Radiation mechanism: Basic sources of Radiation- Current distribution on antennas, Basic antenna parameters.

UNIT II- Analysis and Synthesis of Antennas
Vector potential, Antenna theorems and definitions, dipole, loop, reflector, slot antennas. Types of linear arrays, current distribution in linear arrays, Antenna array synthesis techniques.

UNIT III Smart Antennas
Spatial processing for wireless systems: Introduction, Vector channel impulse response & the spatial signature. Spatial processing receivers, fixed beam forming Networks, switched beam systems, Adaptive antenna systems, Wide band smart antennas, Digital radio receiver & software radio for smart antennas.

UNIT IV- Smart Antenna Techniques for CDMA
Non-coherent & coherent CDMA spatial processors, spatial processing rake receiver, Multi-user spatial processing, dynamic resectoring, down link beam forming for CDMA, MIMO.

UNIT V: Microstrip Antenna
Radiation Mechanism and Excitation techniques : Microstrip dipole; Patch ,Rectangular patch, Circular patch, and Ring antenna – radiation analysis from cavity model; input impedance of rectangular and circular patch antenna; Microstrip array and feed network; Application of microstrip array antenna.

Text Books:
[1] Balanis A., Antenna Theory Analysis and Design, John Wiley and Sons, New York, 1982.
[2] Joseph C. Liberti, Theodore S. Rappaport – Smart Antennas for Wireless Communications: IS95 and third generation CDMA Applications, Prentice Hall, Communications Engineering and Emerging Technologies Series.

References:
[3] I.J. Bahl and P. Bhartia, Microstrip Antennas,Artech House,Inc.,1980
[4] W.L.Stutzman and G.A.Thiele,Antenna Theory and Design, 2nd edition,John Wiley& Sons Inc.,1998.