SCHOOL
OF
INFORMATION AND COMMUNICATION TECHNOLOGY

COURSE STURCTURE AND DETAILED SYLLABUS

2 YEARS M. TECH. ICT FOR ENGINEERING GRADUATES

SPECIALIZATION:

VLSI

GAUTAM BUDDHA UNIVERSITY
GAUTAM BUDH NAGAR, GREATER NOIDA
2011-2012

2-Years M.Tech. (ICT) for Engineering Graduates
Specialization: VLSI Design

SEMESTER I

Sr.No	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC535	Digital IC Design	3-1-0	4
2	EC537	Electronic Design Automation	3-1-0	4
3	EC539	Advanced Digital Signal Processing	3-1-0	4
4		Elective-2	3-0-0	3
5	SS101	Human Values & Buddhist Ethics	2-0-0	2
		PRACTICALS		
6	EC585	Design Lab I	0-0-2	2
7	CS591	Programming Lab	0-0-2	2
8	GP531	General Proficiency	---	1
		Total	**14-3-4**	**22**
		Total Contact Hours	21	

Elective-2

Sr.No	Course Code	Courses
1	EC565	Embedded System Design
2	EC541	Advanced Computer Network
3	CS574	Principle of Artificial Intelligence
4	EC533	Wireless Network
5	CS536	Computer System Architecture
6	CS576	Data Mining
7	EC531	Advanced Digital Communication System

SEMESTER II

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	MA402	Simulation and Modeling	3-1-0	4
2	EC536	VLSI Technology	3-0-0	3
3	EC538	Advanced Analog VLSI Design	3-0-0	3
4		Elective-3	3-0-0	3
5		Elective-4	3-0-0	3
		PRACTICALS		
6	EC560	Design Lab II	0-0-2	2
7	EC592	Major Project	0-0-10	5
8	GP532	General Proficiency	---	1
		Total	**15-1-12**	**24**
		Total Contact Hours	28	

Electives (3 & 4)

2-Years M.Tech. (ICT) for Engineering Graduates
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Sr.No	Course Code	Courses
1.	EC566	VLSI for Wireless Communication
2.	EC542	Quality of Services in Networks
3.	CS447/CS547	Multimedia Techniques
4.	CS449/CS561	Soft Computing
5.	EC534	Wireless System Design
6.	CS404/CS534	Open Source Software System
7.	EC568	Design of Semiconductor Memories
8.	EC570	Principles of MEMS Design
9.	EC572	Solid State Electronics Devices
10.	EC574	Integrated Circuit Physical Design
11.	EC576	CMOS RF Circuit Design
12.	EC578	CMOS VLSI Design
13.	EC580	VLSI Design Techniques
14.	EC544	Advanced RF Engineering
15.	EC548	Probability and Stochastic Processes
16.	EC550	Advanced Microwave Communication
17.	EC556	Image Processing and Biometrics
18.	EC532	Advanced Communication Networks

SEMESTER – III

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC633	Low Power VLSI Design	3-0-0	3
2	CS633	Research Techniques in ICT	3-0-0	3
3		Elective- 5	3-0-0	3
4		Elective- 6	3-0-0	3
		PRACTICALS		
5	EC683	Design Lab III	0-0-2	2
6	EC691	Dissertation Part-I	0-0-14	7
7	GP631	General Proficiency	---	1
		Total	**12-0-16**	**22**
		Total Contact Hours	28	

Electives (5 & 6)

2-Years M.Tech. (ICT) for Engineering Graduates
Specialization: VLSI Design

Sr.No	Course Code	Courses
1.	EC665	VLSI ASIC Design
2.	EC667	Micro and Smart System Technology
3.	EC669	Advances in VLSI Design
4.	EC671	Modern Optimization Techniques
5.	EC673	VLSI-Reliability Engineering
6.	EC647	Sensor Network
7.	EC675	Mixed-Signal VLSI Design
8.	EC677	DSP Integrated Circuits
9.	EC679	Advanced Digital VLSI Design
10.	EC659	Test and Verification of VLSI Circuits
11.	EC661	EM Interference and Capabilities in System Design
12.	EC663	Algorithm for VLSI Design Automation
13.	EC643	Smart Antenna System

SEMESTER-IV

Sr. No	Course Code	Courses	L-T-P	Credits
1	EC690	Dissertation Part-II	---	21
2	GP632	General Proficiency	---	1
		Total	**---**	**22**

Grand Total Credits = 90

2-Years M.Tech. (ICT) for Engineering Graduates
Specialization: VLSI Design

DIGITAL IC DESIGN			
Course Code:	**EC535**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Digital number systems and information representation; arithmetic operations, decimal and alphanumeric codes, Binary logic, Boolean algebra (identities, functions and manipulation), standard forms, simplification, Logic gates, switch-level and logic CMOS implementation, integrated circuits.

UNIT II: Combinational Logic Design
Components of Combinational Design, Multiplexer and Decoder, Multiplexer Based Design of Combinational Circuits, Implementation of Full Adder using Multiplexer and Decoder, Types of PLD, Combinational Logic Examples, PROM - Fixed AND Array and Programmable OR Array Implementation of Functions using PROM, PLA, PAL, Comparison of PROM, PLA and PAL Implementation of a Function using PAL, Types of PAL Outputs, Device Examples

UNIT III: Sequential Logic Design
Introduction to Sequential Circuits, R-S Latch and Clocked R-S Latch, D Flip Flop, J-K Flip Flop, Master Slave Operation, Edge Triggered Operation, Clocking of Flip-flops, Setup and Hold Times, Moore Circuit, Mealy Circuit Clocking Rules, Sequential Circuits – Design Rules, Sequential Circuit Design Basics, Design of a 4-bit Full Adder using D Flip-flop, Pattern Identifier, State Graph , Transition Table, Implementation of Pattern Identifier, MUX Based Realization, ROM Based Realization, PAL Implementation

UNIT IV: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
PLD families, ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array, I/O Block, Programmable interconnect, Xilinx – 3000 series and 4000 series FPGAs, Altera CPLDs, Altera FLEX 10K series PLDs, Designing a synchronous sequential circuit using PLA/PAL, Realization of finite state machine using PLD

UNIT V: System Design using HDL
HDL operators , Arrays, concurrent and sequential statements , packages, Data flow, Behavioral – structural modeling, compilation and simulation of HDL code, Test bench, Realization of combinational and sequential circuits using HDL, Registers, counters, sequential machine, serial adder , Multiplier-Divider, System Design examples.

Text Books:
[1] Charles H.Roth Jr : Fundamentals of Logic Design, Thomson Learning, 2004
[2] J.Bhaskar: A Verilog Primer, BSP, 2003.
[3] J.Bhaskar: A Verilog HDL Synthesis BSP, 2003

References:
[1] Nripendra N Biswas : Logic Design Theory, Prentice Hall of India,2001
[2] Parag K.Lala: Digital system Design using PLD, B S Publications, 2003
[3] Charles H Roth Jr. : Digital System Design using VHDL, Thomson learning, 2004
[4] Douglas L.Perry : VHDL programming by Example, Tata McGraw Hill, 2006

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ELECTRONIC DESIGN AUTOMATION			
Course Code:	**EC537**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exams Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exams Hours:**	**3**

UNIT I: Introduction
An overview of OS commands. System settings and configuration. Introduction to Unix/Linux commands. Writing Shell scripts. VLSI design automation tools. An overview of the features of CAD tools. Modelsim, Leonardo spectrum, ISE 8.1i, Quartus II, VLSI backend tools.

UNIT II: Synthesis and Simulation using HDLs
Basics of Verilog Language, Operators, Hierarchy, Procedures And Assignments, Timing Controls And Delay. Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, Other Verilog features. Verilog/VHDL And Logic Synthesis. Memory Synthesis, FSM Synthesis, Performance-Driven Synthesis. Simulation-Types of Simulation, Logic Systems Working of Logic Simulation, Cell Models, Delay Models State Timing Analysis, Formal Verification, Switch-Level Simulation Transistor-Level Simulation.

UNIT III: Tools for Circuit Design and Simulation
Circuit simulation using SPICE - circuit description. AC, DC and transient analysis. Advanced SPICE commands and analysis. Fundamentals Of Analog And Digital Simulation. Models for diodes, transistors and opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits**.** Mixed signal circuit modeling and analysis using VHDL –AMS.\

UNIT IV: Tools for PCB Design and Layout
An Overview of High Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB. Introduction to Orcad PCB Design Tools.

UNIT V: System Design
System design using systemC- SystemC models of computation. Classical hardware modeling in system C. Functional modeling. Parametrized modules and channels. Test benches. Tracing and debugging.

Text Books:
[1] J.Bhaskar: A Verilog Primer, BSP, 2003.
[2] J.Bhaskar: A Verilog HDL Synthesis BSP, 2003
[3] M.H.Rashid: Spice for Circuits and Electronics using Pspice (2/e), PHI.
[4] M.J.S.Smith, Application Specific Integrated Circuits, Pearson, 2002

References:
[1] ORCAD: Technical Reference Manual, Orcad, USA.
[2] SABER: Technical Reference Manual, Analogy Nic, USA.
[3] J. Bhaskar: A VHDL Synthesis Primer, BSP, 2003.
[4] Grdtker et al.: System Design with SystemC, Kluwer, 2004.
[5] P.J. Ashenden et al , The System Designer's Guide to VHDL-AMS, Elsevier, 2005

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ADVANCED DIGITAL SIGNAL PROCESSING			
Course Code:	**EC539**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Digital Filter Design

Amplitude and phase responses of FIR filters - Linear phase filters - Windowing techniques for design of Linear phase FIR filters - Rectangular, Hamming, Kaiser windows - frequency sampling techniques - IIR Filters - Magnitude response - Phase response - group delay - Design of Low Pass Butterworth filters (low pass) - Bilinear transformation - prewarping, impulse invariant transformation.

UNIT II: Discrete Random Signal Processing

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Auto covariance matrices. Parseval's Theorem, Wiener-Khintchine Relation- Power Spectral Density- Periodogram Spectral Factorization, Filtering random processes, Low Pass Filtering of White Noise, Parameter estimation: Bias and consistency.

UNIT III: Spectrum Estimation

Estimation of spectra from finite duration signals, Non-Parametric Methods-Correlation Method, Periodogram Estimator, Performance Analysis of Estimators -Unbiased, Consistent Estimators- Modified periodogram, Bartlett and Welch methods, Blackman –Tukey method. Parametric Methods - AR, MA, ARMA model based spectral estimation, Parameter Estimation -Yule-Walker equations, solutions using Durbin's algorithm

Unit IV: Adaptive Filters

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR), RLS adaptive filters-Exponentially weighted RLS-sliding window RLS.

UNIT V: Multirate Digital Signal Processing

Mathematical description of change of sampling rate - Interpolation and Decimation, Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter implementation for sampling rate conversion- direct form FIR structures, Polyphase filter structures, time-variant structures, Multistage implementation of multirate system. Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

Text Books:

[1] Monson H.Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc.,Singapore, 2002.
[2] John G.Proakis, Dimitris G.Manolakis, Digital Signal Processing Pearson Education, 2002.
[3] Rafael C. Gonzalez, Richard E.Woods, Digital Image Processing, Pearson Education, Inc., 2nd Edition, 2004.

References:

[1] John G.Proakis et.al., Algorithms for Statistical Signal Processing, Pearson Education, 2002.
[2] Dimitris G.Manolakis et.al., Statistical and adaptive signal Processing, McGraw Hill, Newyork,2000.

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DESIGN LAB I			
Course Code:	**EC585**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to Simulation Software Modelsim.
2. Realization of Gates using VHDL (AND, OR, NOT)
3. Realization of Universal Gates using VHDL (NAND,NOR, EX-OR, EX-NOR).
4. Realization of 2 to 4 Decoder using VHDL.
5. Realization of 3 to 8 Encoder using VHDL.
6. Realization of Combinational Design of Multiplexer using VHDL.
7. Realization of Combinational Design of Demultiplexer and Comparator using VHDL.
8. Realization of Functions of Half and Full Adder with different Modeling style using VHDL.
9. Realization of 32 bit ALU using VHDL.
10. Realization of Flip-flops using VHDL (SR,D, JK,T).
11. Realization of a 4-bit binary, BCD counters and any sequence counter with Synchronous Reset.
12. Realization of a 4-bit binary, BCD counters and any sequence counter with Asynchronous Reset.
13. Realization of VHDL code for 7- Segments Display.
14. Realization of VHDL codes to display messages on given LCD panel.
15. Realization of VHDL code to operate a given stepper motor.

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PROGRAMMING LAB			
Course Code:	**CS591**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. To find the sum of individual digits of a given number
2. To print the Fibonacci series for 1 to n value
3. To print a prime numbers up to 1 to n
4. To find the roots of the quadratic equation
5. To calculate the sum. Sum=1-x2/2!+ x4/4!- x6/6!+ x8/8!- x10/10!
6. Programs that use recursive function to find the factorial of a given integer.
7. Factorial of a number is nothing but the multiplication of numbers from a given number to 1
8. Program that use non recursive function to find the factorial of a given integer.
9. Factorial of a number is nothing but the multiplication of numbers from a given number to 1
10. To find the GCD of two given integers by using the recursive function
11. To find the GCD of two given integers by using the non recursive function
12. WAP to read a series of words from terminal using scanf function.
13. WAP to read a line of text containing a series of words from the terminal.
14. WAP for all type of sorting.
15. WAP. to illustrate the comparison of structure variables
16. WAP to print the address of variable along with its value.
17. WAP to illustrate the use of pointers in arithmetic operation.
18. WAP to read data from keyboard, write it to a file called INPUT, again read the same data from the INPUT file, and display it on the screen.

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EMBEDDED SYSTEM DESIGN			
Course Code:	**EC565**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to an embedded systems design

Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

Unit II: RTOS & its overview

Real Time Operating System: Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

Unit III: Microcontroller

Role of processor selection in Embedded System (Microprocessor V/s Micro-controller), 8051 Microcontroller: Architecture, basic assembly language programming concepts, Instruction set, Addressing Modes, Logical Operation, Arithmetic Operations, Subroutine, Interrupt handling, Timing subroutines, Serial data transmission, Serial data communication

Unit IV: Embedded system development

Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

Unit V: Networks for Embedded Systems

The I^2C Bus, The CAN bus, SHARC link Ports, Ethernet, Myrinet, Internet, Introduction to Bluetooth: Specification, Core Protocol, Cable replacement protocol. IEEE 1149.1 (JTAG) Testability: Boundary Scan Architecture

Text Books:

[1] Raj Kamal, Embedded Systems,TMH.
[2] K.J. Ayala, "The 8051 Microcontroller", Penram International.
[3] J. B. Peatman, "Design with PIC Microcontrollers", Prentice Hall

References

[1] David E. Simon, "An Embedded Software Primer," Pearson Education
[2] John Catsoulis ,"Designing Embedded Hardware," O'reilly
[3] Frank Vahid, Tony Givargis ,"Embedded System Design," John Wiley & Sons, Inc
[4] Karim Yaghmour, "Building Embedded Linux Systems", O'reilly
[5] Michael Barr ,"Programming Embedded Systems," O'reilly

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ADVANCED COMPUTER NETWORKS			
Course Code:	**EC541**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Principles of Computer Communications
Introduction to data communications and networks, protocol architecture, networking protocols, reference models, TCP/IP and OSI model, standards organizations, data transmission signal propagation, bandwidth of a signal and a medium; data transmission rate and bandwidth, modes of data transmission, guided media and wireless transmission, multiplexing; types of multiplexing; FDM vs. TDM, switching.

Unit II: Data Link and Network Layer Issues
Design issues in data link and network layers, framing, error control, flow control, sliding window protocols, Medium Access Control Sub layer (MACS), Multiple access Ethernet, Wireless LAN, factors affecting routing algorithms, routing algorithm.

Unit III: Advanced Internetworking and Mobility
Internetworking, addressing, routing and routing algorithms, congestion control algorithms, IPv4, ICMP, ARP, IPv6 and ICMPv6 extensions and functionality, mobile IP, service integration and quality of service (QoS) in IP networks.

Unit IV: Advanced Transport Issues and Signaling
Transport services, element of transport protocols, TCP and UDP, RTP, performance issues, congestion control and QoS, techniques to improve QoS, integrated services, signaling for multi-constrained services and applications.

Unit V: Self Organizing Networks
Introduction to Adhoc, sensor and mesh networks, routing in these networks, socket programming, SMTP, HTTP, Remote login, DNS, FTP.

Text Books:
[1] S. Tanenbaum, Computer Networks, 4th edition, Prentice Hall, 2008.
[2] W. Stallings," Data and Computer Communications, 8th edition, Prentice Hall, 2007.
[3] Forouzan,",Data Communications and Networking," 4th edition, McGraw Hill, 2007.

Reference:
[1] B.A. Forouzan," TCP/IP Protocol Suite", TMH, 3rd edition, 2006.
[3] H. Soliman, :Mobile IPv6 - Mobility in a Wireless Internet, Addison-Wesley, 2004.

PRINCIPLES OF ARTIFICIAL INTELLIGENCE			
Course Code:	**CS565**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to Artificial Intelligence
Basic concept of artificial intelligence (AI), history of AI, AI and consciousness, weak and strong AI, physical symbol system hypothesis, comparison of computer and human skills, practical systems based on AI, development of logic, components of AI, mind body problem, Chinese room experiment, artificial life, parallel and distributed AI.

UNIT II: Problem Solving through AI
Defining problem as state space search, analyzing the problem, representing the problems from AI viewpoint, production system, developing production rules, characteristics of production system, algorithm for problem solving using AI technique.

UNIT III: Search Techniques
Use of search in AI problem solution, blind search techniques, heuristic search techniques, concept of heuristic knowledge, designing of the heuristic function, types of heuristic search techniques: generate and test, best first search, problem reduction using AND – OR graph, local search technique, branch and bound search, memory bounded search technique, local beam search, properties of heuristic search techniques, overestimation and underestimation of heuristic function, hill climbing search, simulated annealing search, constraint satisfaction, means ends analysis.

UNIT IV: Introduction to Knowledge
Basic concept of knowledge, types of knowledge: declarative knowledge, procedural knowledge, inheritable knowledge, inferential knowledge, relational knowledge, heuristic knowledge, commonsense knowledge, explicit knowledge, tacit knowledge, uncertain knowledge, knowledge representation, knowledge storage, knowledge acquisition.

UNIT V: Introduction to Logic
Introduction, propositional calculus, syntax of propositional calculus, semantics of propositional calculus, well formed formula, properties of statements, inferencing of propositional logic, predicate logic, syntax of predicate logic, semantics of predicate logic, representation of facts First Order Predicate Logic (FOPL), inferencing in predicate logic, concept of resolution, resolution algorithm, skolemization, Types of resolution, unit resolution, binary resolution.

Game Playing
Theory of game playing, formulation of problem from viewpoint of game playing, minimax search procedure, ply of a search process, secondary effect, horizon effect, credit assignment problem, alpha – beta pruning, some example game playing theories: chess program, checker's program, card game, deep blue.

Reference books:
[1] Ela Kumar: Artificial Intelligence, IK international pub., New Delhi, 2008.
[2] Elanie Reich: Artificial Intelligence, TMH publishing house, 2008.
[3] Artificial intelligence, Peterson, TataMcGraw Hill, 2008.
[4] Russel and Norvig: Artificial intelligence, Pearson Printice Hall Publication, 2006.
[5] Winston: Artificial Intelligence, , PHI publication, 2006.

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WIRELESS NETWORKS			
Course Code:	**EC533**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: fundamentals of cellular networks
Cellular concepts, SIR calculation, capacity enhancement techniques, channel allocation schemes, handover, path loss modeling, multipath, channel measurements, simulation of radio channels.

Unit II: Multiple access Techniques
TDMA, FDMA, spread spectrum multiple access-SDMA, packet radio- protocols, CSMA protocols, reservation protocols.

Unit III: Wireless LAN
Evolution of WLAN, IEEE802.11 Physical layer, MAC layer, IEEE 802.11(a,b,e,f,g,h,i) Wireless routing protocols, Mobile IP, IPv4, IPv6, wireless TCP, protocols for 3G and 4G networks, IMT 2000, UMTS, CDMA2000, All-IP based cellular networks, wireless ATM, HYPER LAN, HYPER LAN2, WMAN,

Unit IV: WPAN and Geo-location Systems
IEEE 802.15 WPAN, Home RF, Bluetooth, interface between Bluetooth and IEEE 802.11, wireless geo-location technologies, geo-location standards, Satellite communication-satellite parameters and configurations, capacity allocation, Bluetooth, radio specifications, baseband specifications, iEEE802.15.

Unit-V: current issues in wireless networks
Issues in wireless networks: securities issues, authentication in mobile networks, privacy issues, power management, energy awareness computing, mobile IP VoIP applications

Text Books:
[1] William Stallings: Wireless Communications and Networks, PHI.
[2] Kaveh Pahlavan, Prashant Krishnamurthy: Principles of Wireless Networks, Pearson Education, 2002.

References:
[1] Theodore S. Rappaport: Wireless Communication, Principles and Practice, PHI.

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COMPUTER SYSTEM ARCHITECTURE			
Course Code:	**CS536**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I REGISTER TRANSFER AND MICROOPERATION

Register transfer language, bus and memory transfers, bus architecture, bus arbitration, arithmetic logic, shift microoperation, arithmetic logic shift unit.

UNIT II PROCESSOR DESIGN

Processor organization: general register organization, stack organization, addressing mode, instruction format, data transfer & manipulations, program control, reduced instruction set computer.

UNIT III INPUT-OUTPUT ORGANIZATION

I/O interface, synchronous and asynchronous data transfer, strobe, handshaking schemes, modes of transfer, interrupts & interrupt handling, direct memory access, input-output processor.

UNIT IV MEMORY ORGANIZATION

Memory hierarchy, main memory (RAM and ROM Chips), organization of 2d and $2^{1/2}$ d, auxiliary memory, cache memory, virtual memory, memory management hardware.

UNIT V INTRODUCTION TO PARALLELISM

Pipelining, Arithmetic pipeline, Instruction Pipeline, Flynn's classification of computer, Feng classification, Parallel Architecture, RISC & CISC, Interconnection Network Architecture

Reference Books:

1. Patterson, Computer Organisation and Design, Elsevier Pub. 2009
2. William Stalling, " Computer Organization", PHI
3. Vravice,Hamacher & Zaky, "Computer Organization", TMH
4. Mano," Computer System Architecture", PHI
5. John P Hays, " Computer Organization", McGraw Hill
6. Tannenbaum," Structured Computer Organization', PHI
7. P Pal chaudhry, ' Computer Organization & Design', PHI
8. Kai Hawng, Computer Architecture, TMH

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DATA MINING			
Course Code:	**CS 543**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to Data Mining and data ware house: Motivation and importance, What is Data Mining, Relational Databases, Data Warehouses, Transactional Databases, Advanced Database Systems and Advanced Database Applications, Data Mining Functionalities, Interestingness of a pattern Classification of Data Mining Systems, Major issues in Data Mining.
Data Warehouse: Multi-Dimensional Data Model, Data Warehouse Architecture, Data Warehouse Implementation, Development of Data Cube Technology, Data Ware housing to Data Mining

UNIT II: Data preprocessing, language, architectures, concept description
Why Preprocessing, Cleaning, Integration, Transformation, Reduction, Discretization, Concept Hierarchy Generation, Data Mining Primitives, Query Language, Graphical User Interfaces, Architectures, Concept Description, Data Generalization, Characterizations, Class Comparisons, Descriptive Statistical Measures.
Data Mining Primitives: What defines Data Mining Task? A Data Mining query language Designing graphical User Interfaces Based on a Data Mining, Query, language, Architectures of Data Mining Systems

UNIT III: Concept Description, Characterization and comparison
What is Concept Description? Data Generalization and summarization-based Characterization, Analytical Characterization: Analysis of Attribute Relevance, Mining Class Comparisons, Discriminating between different Classes, Mining Descriptive Statistical Measures in large Databases

UNIT IV: Mining Association rule in large Databases
Association Rule Mining, Mining Single -Dimensional Boolean Association Rules from Transactional Databases, Mining Multilevel Association Rules from Transaction Databases, Mining Multidimensional Association Rules from Relational Databases and Data Warehouses, From Association Mining to Correlation Analysis, Constraint-Based Association Mining

UNIT V: Classification and Clustering:
Concepts and Issues regarding Classification and Prediction, Classification by Decision Tree Induction, Bayesian Classification, Classification by Back propagation, Classification Based on Concepts from Association Rule Mining, Other Classification Methods like k-Nearest Neighbor Classifiers, Case-Based Reasoning, Generic Algorithms, Rough Set Approach, Fuzzy Set Approaches, Prediction, Classifier Accuracy.
Cluster Analysis: What is Cluster Analysis? Types of Data in Cluster Analysis, A categorization of Major Clustering methods.

Text Books:
[1] Jiawei Han and Micheline Kamber: Data Mining Concepts and Techniques, Morgan Kaufman Publications

Reference Books :
[1] Adriaan: Introduction to Data Mining, Addison Wesley Publication
[2] A.K.Pujari: Data Mining Techniques, University Press

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ADVANCED DIGTAL COMMUNCIATION SYSTEM			
Course Code:	**EC531**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Pulse Modulation Analog Signals:- Sampling of Signal, Sampling Theorem for Low Pass and Band Pass Signals, Aliasing, Pulse Amplitude Modulation (PAM), Time Division Multiplexing (TDM), Channel Bandwidth for PAM-TDM Signal, Types of Sampling, Instantaneous, Natural and Flat Top (Mathematical and Spectral Analysis), Aperture Effect, Introduction to Pulse Position and Pulse Duration Modulation.

Unit II: Pulse Code Modulation Digital Signal:- Quantization, Quantization Error, Pulse Code Modulation (PCM), Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding NRZ, RZ, Biphase, Duo Binary Etc ,Differential PCM (DPCM), Delta Modulation (DM), and Adaptive Delta Modulation (ADM), Slope Overload Error ,Granular Noise ,Comparison of various system in terms of Bandwidth and Signal-to-Noise Ratio.

Unit III: Digital Modulation Techniques :- Analysis, Generation and Detection (Block Diagram), Spectrum and Bandwidth of Amplitude Shift Keying (ASK), Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Offset and Non-offset Quadrature Phase Shift Keying (QPSK), M-ary PSK, Binary Frequency Shift Keying (BFSK), M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation (QAM), Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

Unit IV: Concept of Probability, Relative Frequency and Probability Conditional Probability and Independent Events, Random Variables, Discrete Random Variables, Cumulative Distribution Function(CDF), Probability Density Function(PDF),Statistical Averages (Means),Chebyshev's Inequality, Central Limit Theorem.

Unit V: Spread Spectrum Modulation: Pseudo random noise sequences, notion of spread spectrum, direct sequence, frequency hopping, processing gain. Convolution codes and Golay codes.

Text Books:
[1] B. Sklar, Digital Communication, Pearson Education.
[2] Tomasi: Advanced Electronics Communication Systems, 6th Edition, PHI

References:
[1] Taub & Schilling, Principles of Communication system, TMH.
[2] Lathi B.P., Modern Analog and Digital Communication systems, Oxford Uni. Press.
[3] Haykin Simon, Digital Communication, Wiley Publication.
[4] Proakis, Digital communication, McGraw Hill
[5] Schaum's Outline series, Analog and Digital Communication.
[6] Singh and Sapre: Communication System, TMH
[7] Couch: Digital and Analog Communication, Pearson Education
[8] David Smith: Digital Transmission Systems, Springer- Macmillan India Ltd

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VLSI TECHNOLOGY			
Course Code:	**EC536**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II: Lithography and Relative Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III: Deposition, Diffusion, Ion Implantation and Metallization
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV: Process Simulation and VLSI Process Integration
Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V: Assembly Techniques and packaging of VLSI Devices
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

Text Books:
[1] S.M.Sze: VLSI Technology, Mc.Graw Hill Second Edition. 2002.
[2] Richard Jaegar, Introduction to Microelectronics Fabrication, Addison-Wesley, 2006.
[2] Douglas A. Pucknell and Kamran Eshraghian: Basic VLSI Design, Prentice Hall India, 2003.

References:
[1] Amar Mukherjee: Introduction to NMOS and CMOS VLSI System design, Prentice Hall India, 2000.
[2] Wayne Wolf : Modern VLSI Design, Prentice Hall India,1998.
[3] Plummer, Deal and Graffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Prentice Hall, 2000

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ADVANCED ANALOG VLSI DESIGN			
Course Code:	**EC538**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I- Introduction
Basic building blocks in Analog ICs, Translinear networks, Video and RF/IF Amplifiers, IC negative feedback wide band amplifiers, Voltage Sources and References, IC Voltage Regulator, Characteristics and Parameters of Voltage, Protection circuitry for Voltage Regulator, Switched Mode Regulator, IC Voltage Op Amps, Transconductance Op Amps, Audio Power and Norton's Amplifier, Analog Multipliers, Voltage Controlled Oscillator, Self Tuned Filter, Phase Locked Loop, Current Mode ICs.

UNIT II – CMOS Analog Circuit Design
Submicron, Deep Submicron and Ultra-Deep Submicron CMOS Technology, BiCMOS Technology, Latchup and ESD, MOS Capacitor Model, Large Signal Model Dependence, Small Signal Models, Noise, Passive Component Models, Component Matching, Computer Models and Extraction of the Simple Large Signal Model, MOS Switch, Current Sinks and Sources.

UNIT III – High Speed Operational Amplifiers & Comparators Design
Two-stage Op Amp Design, Simulation and Measurement of Op Amps, Buffered Op Amps, High Speed Op Amps, Differential-In, Differential-Out Op Amps, Low Noise and Low Power Op Amps, Low Voltage Op Amps, Open-Loop Comparators, Improved Open-Loop Comparators and Latches, High speed comparators

UNIT IV – Design of ADCs & DACs
Characterization of DACs and Current Scaling DACs, Voltage, Charge Scaling and Serial DACs, Improved Resolution, Characterization of ADCs and Sample and Hold Circuits, Moderate Speed Nyquist ADCs, High Speed Nyquist ADCs, Oversampling ADCs.

UNIT V – Advance Topics
Analysis and optimized design of integrated analog systems and building blocks, Specific topics include operational and wide-band amplifiers, gain-bandwidth and power considerations, analysis of noise in integrated circuits, low noise design, feedback, precision passive elements, analog switches, comparators, CMOS voltage references, non-idealities such as matching and supply/IO/substrate coupling.

Text Books:
[1] Allen and Holberg, CMOS Analog Circuit Design, Oxford University Press
[2] Hurst and Meyer, Analysis and Design of Analog Integrated Circuits, Wiley
[3] Behzad Razavi, Design of Analog CMOS ICs, 2000. John Wiley
[4] Jaeger and Blalock, Microelectronics Circuit Design, McGraw Hill

References:
[1] Agarwal & Lang, Foundations of Analog and Digital Electronic Circuits, (The Morgan Kaufmann Series in Computer Architecture and Design)
[2] Behzad Razavi, Introduction to Microelectronics, 2006. John Wiley

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DESIGN LAB II			
Course Code:	**EC560**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to Cadence Virtuoso tool and Full Custom IC Design cycle.
2. Realization of an Inverter.
3. Realization of Differential Amplifier.
4. Realization of Common Source Amplifier.
5. Realization of Common Drain Amplifier.
6 .Realization of Operational Amplifier.
7. Realization of R-2R DAC.
8. Realization of SAR based ADC.

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VLSI FOR WIRELESS COMMUNICATIONS			
Course Code:	**EC408/EC566**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Standards, Communication Systems, Overview of Modulation Scheme, QPSK, BPSK, MSK, Classical Channel, Wireless Channel Description, Path Environment, Path Loss, Friss Equation, Time Varying Channel Models, Envelope Fading, Frequency Selective Fading, Fast Fading.

Unit II: Receiver Architectures
Introduction, Receiver Front: Motivations, Heterodyne and other Architecture, Filter Design: Band Selection Filter, Image Rejection Filter, Channel Filter, Nonidealities and Design Parameters: Nonlinearity, Noise, Derivation of NF, IIP_3 of receiver Front end.

Unit III: Low Noise Amplifier (LNA)
Introduction, Matching Networks, Wideband LNA Design, DC bias, Gain and Frequency Response, Noise Figure, Narrowband LNA, Impedance Matching, Interpretation of Power Matching, Quality Factor, Core Amplifier, Noise Figure, Power Dissipation, Noise Contribution from other sources.

Unit IV: Active Mixers
Unbalanced Mixers, Single Balanced Mixers, Qualitative Description of Gilbert Mixer, Conversion Gain, Distortion analysis of Gilbert Mixer, Comparison of Sample and Hold Circuit and Sampling Mixer.

Unit V: Passive Mixers
Switching Mixers, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single Ended Sampling Mixer, Distortion in single ended sampling mixer, Intrinsic and Extrinsic noise.

Text Books:
[1] Bosco Leung, "VLSI for Wireless Communication", PHI.

References:
[1] Emad N Farag, M.I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems", Kluwer Publication.
[2] David Tsee, Pramod Viswanath," Fundamentals of Wireless Communication", Cambridge Univ Press.

2-Years M.Tech. (ICT) for Engineering Graduates
Specialization: VLSI Design

QUALITY OF SERVICES IN NETWORKS			
Course Code:	**EC406/EC542**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: IP Quality Of Service
Level of QoS, IP QoS history, performance measures, QoS functions, layer 2 QoS technologies, multiprotocol label switching, end-to-end QoS.

Unit II: QOS Architectures
Intserv architecture; RSVP, reservation style, service types, RSVP media support, RSVP scalability, along with their case studies. Diffserv architecture; network boundary traffic conditioners, PHB, resource allocation policy, packet classification.

Unit III: Network Boundary Traffic Conditioners and Resource Allocation
Packet classification, packet marking, need of traffic rate management, traffic policing, traffic shaping along with their case studies. Scheduling of QoS support, sequence number computation based WFQ, flow based WFQ, flow based distributed DWFQ, class based WFQ, priority queuing, schedule mechanisms for voice traffic, MWRR, MDRR along with their case studies.

Unit IV: Congestion Avoidance
TCP slow start and congestion avoidance, TCP traffic behavior in a trial drop scenario, REDproactive queue management for congestion avoidance, WRED, flow WRED, ECN, SPD along with their case studies.

Unit V: QOS in MPLS-Based Networks
MPLS, MPLS with ATM, MPLS QoS, MPLS VPN, MPLS VPN QoS along with their case studies. traffic engineering; MPLS traffic engineering, the layer 2 overlay model, RRR, TE trunk definition, TE tunnel attributes, link resource attributes, distribution of link resource information, path selection policy, TE tunnel setup, link admission control, TE path maintenance, TE RSVP, IGP routing protocols, TE approaches along with their case studies.

Text Books:
[1] Srinivas Vegesna, “IP Quality of Service,” CISCO PRESS, 2001.
[2] Santiago alvarez, “Qos for IP/MPLS Networks,” Cisco Press, Pearson Education, 2006.

References:
1. IETF website: www.ietf.org

2-Years M.Tech. (ICT) for Engineering Graduates
Specialization: VLSI Design

MULTIMEDIA TECHNIQUES			
Course Code:	**CS553/CS653**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit-I: Introduction
Introduction to Multimedia, Multimedia Information, Multimedia Objects, Multimedia in business and work. Convergence of Computer, Communication and Entertainment products.

Stages of Multimedia Projects
Multimedia hardware, Memory & storage devices, Communication devices, Multimedia software's, presentation tools, tools for object generations, video, sound, image capturing, authoring tools, card and page based authoring tools.

Unit-II: Multimedia Building Blocks
Text, Sound MIDI, Digital Audio, audio file formats, MIDI under windows environment Audio & Video Capture.

Unit-III: Data Compression
Huffman Coding, Shannon Fano Algorithm, Huffman Algorithms, Adaptive Coding, Arithmetic Coding Higher Order Modeling. Finite Context Modeling, Dictionary based Compression, Sliding Window Compression, LZ77, LZW compression, Compression, Compression ratio loss less & lossy compression.

Unit-IV: Speech Compression & Synthesis
Digital Audio concepts, Sampling Variables, Loss less compression of sound, loss compression & silence compression.

Unit-V: Images
Multiple monitors, bitmaps, Vector drawing, lossy graphic compression, image file formatting animations Images standards, JPEG Compression, Zig Zag Coding, Multimedia Database .Content based retrieval for text and images, **Video:** Video representation, Colors, Video Compression, MPEG standards, MHEG Standard Video Streaming on net, Video Conferencing, Multimedia Broadcast Services, Indexing and retrieval of Video Database, recent development in Multimedia.

Reference:
[1] Tay Vaughan: Multimedia, Making IT Work, Osborne McGraw Hill.
[2] Buford: Multimedia Systems, Addison Wesley.
[3] Agrawal & Tiwari: Multimedia Systems, Excel.
[4]Mark Nelson: Data Compression Book, BPB.
[5] David Hillman: Multimedia technology and Applications, Galgotia Publications.
[6] Rosch: Multimedia Bible, Sams Publishing.
[7] Sleinreitz: Multimedia System, Addison Wesley.
[8] James E Skuman: Multimedia in Action, Vikas.

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SOFT COMPUTING			
Course Code:	**CS551/CS651**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fuzzy Logic
Introduction to fuzzy logic, classical and fuzzy sets, overview of fuzzy sets, membership function, fuzzy rule generation, operations on fuzzy sets: compliment, intersection, union, combinations on operations, aggregation operation.

UNIT II: Fuzzy Arithmetic
Fuzzy numbers, linguistic variables, arithmetic operations on intervals & numbers, uncertainty based information, information and uncertainty, no specificity of fuzzy and crisp sets, fuzziness of fuzzy sets.

UNIT III: Neural Network
Overview of biological neurons, computational neuron, mathematical model of neurons, ANN architecture, single layer and multilayer architectures, activation function, threshold value, self learning and forced learning algorithms, feed forward and feedback architectures.

UNIT IV: Learning Fundamentals
Learning paradigms, supervised and unsupervised learning, reinforced learning, ANN training, algorithms perceptions, training rules, delta, back propagation algorithm, multilayer perception model, Hopfield networks, associative memories, applications of artificial neural networks,

UNIT V: Genetic Algorithms
History of genetic algorithm, terminology of genetic algorithm, biological background, creation of offspring, working principles of genetic algorithms, fitness function, reproduction: Roulette wheel selection, Boltzmann selection, cross over mutation, inversion, deletion, and duplication, generation cycle.
Concept of Uncertainty
Presence of uncertainty in real world problems, handling uncertain knowledge, degree of belief, degree of disbelief, uncertainty and rational decisions, decision theory, utility theory, concept of independent events, Bay's rule, using Bay's rule for combining events.

References:

[1] Peteus J. Braspenning: Artificial Neural Networks: An introduction to ANN Theory and Practice, PHI publication, 2005.
[2] Paul P. Wang: Fuzzy Logic: A spectrum of Theoretical and Practical issues, Pearson publication 2004.
[3] Lotfi Asker Zadeh, George J. Kilr, Bo Yuan Fuzzy: Sets, Fuzzy logic, and Fuzzy Systems: Selected Papers-, 2005.
[4] Foundations of Fuzzy logic and Soft Computing: 12th International Fuzzy conference proceeding, 2005.
[5] Particia Melin: Neural Networks Theory, Oxford University press, 2003
[6] Oscar Castillo: Neural Networks Theory and Application, Wiley Eastern publication 2003.

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WIRELESS SYSTEM DESIGN			
Course Code:	**EC534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
RF system design procedures, methodology, link budget, propagation models, tower-top amplifiers, RF design guidelines, traffic projections, cell site design,

Unit II:
Network design- traffic forecasts, node dimensioning, interface design, placement of network nodes, topology

Unit III:
Antenna systems,-base station antenna, cross pole antenna, dual band antenna, intelligent antenna, diversity techniques-derivation of selection diversity and maximal ratio combining improvement, polarization diversity, frequency diversity, time diversity, RAKE receiver

Unit IV:
UMTS system design-design principles, coverage analysis, capacity analysis, radio access networks, overloading UMTS over GSM, CDMA system design-design methodology, deployment guidelines, traffic estimation, radio elements, fixed network d4sign requirements, traffic models, link budget, case studies-CDAM2000 1xRTT, EVDO, CDMA2000 1xRTT with EVDO overlay

Unit V:
Communication sites-types, installation, towers, stealth, in-building and tunnel systems, inter, modulation, collocation, Study of various network simulators, GloMoSim, ns-2, Opnet, designing and evaluating performance of transport and routing protocols of mobile and wireless networks.

Text Books:
[1] Clint Smith, P.E. Daniel Collins: 3G Wireless Networks" Tata McGraw-Hill, 2nd Edition
[2]Theodore S. Rappaport: Wireless Communication, Principles and Practice" Pearson

References:
IEEE Journals and proceedings

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OPEN SOURCE SOFTWARE SYSTEM			
Course Code:	**CS404/CS534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Open Source Software (OSS)
History, philosophy, ethics, licensing, Pernes' principle, open source software methodology, open source vs. closed source, open source software vs. free software, open source software vs. source available, Windows and Linux, open source standards, open source development environment, OSS in e-government, OSS management, OSS management tools: taskjuggler, dotProject.net, licenses, open source content management system, project management via open source and open standard, copyright, patent, social dynamic of collaboration and legal implication of software intellectual property.

UNIT II: Open Source Technology and Infrastructure
Operating system: Linux, Berkeley Software Distribution (BSD); protocols: low level protocols, high level protocols; common open source language: presentation language, system programming languages, scripting languages; database system: MYSQL, PostgreSQL, BerkeleyDB; web services: Apache; communication servers: send mail, jabber; application and messaging server: Open3.org, Enhydra.org, JBoss, Zope, Zend, Open Source Desktop and server Applications.

UNIT III: Open Source Standards
Standards, open standards, benefits of open standards, national considerations, standard setting organization and processes, open standard organization for internet networking and application/services, computer graphics and multimedia, office documents, open standards usage, Linux standard base, Linux standard base as an ISO standard, Linux standards base certification, patents in standards.

UNIT IV: Open Source Software Applications
Rapid web application development framework: Ruby on Rail (ROR), Model-View-Controller (MVC) model, Don't Repeat Yourself (DRY) principle, convention over configuration principle, open source applications - business applications: Enterprise Resource Planning (ERP), Customer Relationship Management (CRM); educational applications: educational suites, learning support, language,; groupware: Content Management Systems (CSM), Wiki software; programming language support: bug trackers, code generators, configuration software.

UNIT V: Open Source in the Enterprise
Modern era of open source, rebranding open source, character of the community, open source community development, open source and enterprise applications, risks and benefits of using open source in the enterprise, developing an enterprise application strategy, cost, licensing and resources of OSS.

References:

[1] O'Reilly Media, Dan Woods: Open Source for the Enterprise: Managing Risks, Reaping Rewards,, 2005.
[2] James Lee, Brent Ware: Open Source Web Development with LAMP, Pearson Education, 2008.
[3] Paul Kavanagh: Open Source Software: Implementation and Management, Digital Press, 2004.
[4] Steven Weber: The Success of Open Source, Harvard University Press, 2004.

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DESIGN OF SEMICONDUCTOR MEMORIES			
Course Code:	**EC568**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: RAM Technologies
Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs, DRAMs Cell Theory

UNIT II: Non Volatile Memories
Masked Read-Only Memories, High Density ROMs, PROMs, CMOS PROMs, EEPROMs, Floating-Gate EPROM Cell, Electrically Erasable PROMs, EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories, Advanced Flash Memory Architecture.

UNIT III: Memory Testing
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.

UNIT IV: Reliability and Radiation Effects
General Reliability Issues, RAM Failure Modes and Mechanics, Nonvolatile Memory Reliability, Reliability Modeling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, RAM Fault Modeling, Electrical Testing, Psuedo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling.

UNIT V: Packaging Technologies
Radiation Effects, Single Event Phenomenon, Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimeter, Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories, GaAs FRAMs, Analog Memories, Magnetoresistive Random Access Memories

Text Books:
[1] Ashok K. Sharma: Semiconductor Memories Technology, Testing and Reliability, Prentice-Hall of India Private Limited, New Delhi, 1997.
[2] Tegze P. Haraszti: CMOS Memory Circuits, Kluwer Academic publishers, 2001.

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PRINCIPLES OF MEMS DESIGN			
Course Code:	**EC570**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II: Mechanics for MEMS Design
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III: Electrostatic Design
Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV: Circuit and System Issues
Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Capacitive Accelerometer, Piezoelectric pressure sensor, Modeling of MEMS systems, CAD for MEMS.

UNIT V: Introduction to Optical and RF MEMS
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

Text Books:
[1] Stephen Santuria: Microsystems Design, Kluwer publishers, 2000.
[2] Nadim Maluf: An introduction to Micro electro mechanical system design, Artech House, 2000.

References:
[1] Mohamed Gad-el-Hak: The MEMS Handbook, CRC press Baco Raton,2000.
[2] Tai Ran Hsu: MEMS & Micro systems Design and Manufacture Tata McGraw Hill, New Delhi, 2002.

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SOLID STATE ELECTRONICS DEVICES			
Course Code:	**EC572**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fundamental Models
Physical models-bohr model, quantum mechanics, atomic structure, energy bands & charge carriers in semi conductors, carrier concentration, drift of carriers in electric and magnetic fields, diffusion of carriers. Continuity equation. Semi-conductor materials. Introduction to solid state electronics.

UNIT II: Diodes
Fabrication of P-N junctions, equilibrium conditions, forward and reverse biased junctions, steady state conditions, reverse bias breakdown, transient and a.c. condition, Recovery time, deviation from simple theory, metal semi-conductor junction, heterojunction. P-N junction linearly graded and step junction diodes, tunnel diode, photo diode, light emitting diodes and lasers.

UNIT III: BJTs
BJT amplification & switching: Fundamental of BJT operation, minority carier distribution & terminal currents, generalized biasing, switching, frequency limitation of transistors, ebber Molls model, Gummel Poon Model of BJTs. Heterojuction bipolar transistor.

UNIT IV: FETs
FET-metal semi-conductor (MESFETs), FET-Metal insulator semiconductor (MOSFET). Power MOSFETs, MODFETs, High Electron Mobility Transistors.

UNIT V: Integrated circuits
Monolithic device elements, charge transfers devices, very large scale integration, testing of VLSI chips, Stuck at faults and Fault diagnosis.

Text Book:
[1] Ben G Streetman, Solid State Electronic Devices PHI

References:
[1] S M Sze: Physics of semiconductor Devices, Wiley Pub.
[2] Kittel C: Introduction to Solid State Physics, Wiley Pub.

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INTEGRATED CIRCUIT PHYSICAL DESIGN			
Course Code:	**EC574**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: The Well
Substrate, Parasitic Diode, N-well as a Resistor, N-well patterning and layout, Design Rules, Resistance calculation, N-well Resistor, N-well/Substrate Diode, Carrier Concentrations, Fermi Energy Level, Depletion Layer Capacitance, Storage or Diffusion Capacitance, RC Delay through the N-well, Distributed RC Delay, Distributed RC Rise Time, Twin Well Processes.

Unit II: The Metal Layers
Bonding Pad and layout, Metal-to-Substrate capacitance, Passivation, Design and Layout of Metal Layers, Metal1 and Via1, Parasitic Associated with Metal Layers, Intrinsic Propagation Delay, Current-Carrying Limitations, Design Rules for Metal Layers, Contact Resistance, Crosstalk and Ground Bounce , Crosstalk, Ground Bounce, DC Problems, AC Problems.

Unit III: The Active and Poly Layers
Layout Using Active and Poly Layers, P- and N-Select Layers, Poly Layer, Self-Aligned Gate, Poly Wire, Silicide Block, Connecting Wires to Poly and Active, Connecting P-Substrate to Ground, N-Well Resistor layout, NMOS and PMOS Device layout, Standard Cell Frame, Design Rules, Electrostatic Discharge (ESD) Protection, Diodes layout.

Unit IV: Resistors, Capacitors, MOSFETs
Resistors, Temperature Coefficient, Voltage Coefficient, Unit Elements, Guard Rings, Interdigitated Layout, Common- Centroid Layout, Dummy Elements, Poly-Poly Capacitor layout, Parasitic, MOSFETs: Lateral Diffusion, Oxide Encroachment, Source/Drain Depletion Capacitance, Source/Drain Parasitic Resistance, Long-Length MOSFETs layout, Large-Width MOSFETs layout, MOSFET Capacitances.

Unit V: MOSFET Operation
Accumulation, Depletion, Strong Inversion, Threshold Voltage, Characteristics of MOSFETs, MOSFET Operation: Triode and Saturation, Cgs Calculation, Long-Channel MOSFET Models, Model Parameters Related to the Drain Current, Modeling of the Source and Drain Implants Short-Channel MOSFETs Hot Carriers, Lightly Doped Drain, MOSFET Scaling, Short-Channel Effects, Oxide Breakdown, Drain-Induced Barrier Lowering, Gate-Induced Drain Leakage.

Text Books:
[1] R. Jacob Baker: CMOS Circuit Design, Layout, and Simulation, Second Edition.
[2] Christopher Saint, Judy Saint: IC Layout Basics: A Practical Guide

References:
[1] Dan Clein: CMOS IC Layout : Concepts, Methodologies, and Tools,.
[2] Alan Hastings, Roy Alan Hastings: The Art of Analog Layout

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CMOS RF CIRCUIT DESIGN			
Course Code:	**EC576**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF design and Wireless Technology
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

UNIT II: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

UNIT III: RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT V: RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text Book:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University press 1998.

References:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce CMOS Circuit Design, layout and Simulation PHI, 1998
[3] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996

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CMOS VLSI DESIGN			
Course Code:	**EC578**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor theory
nMOS / pMOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT II: CMOS Process Technology
Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT III: Basics of Digital CMOS Design
Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques.

UNIT IV: CMOS Analog Design
Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

UNIT V: Dynamic CMOS and clocking
Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking-clock generation, clock distribution, clocked storage elements.

Text Books:
[1] Neil Weste and K. Eshragian: Principles of CMOS VLSI Design: A System Perspective, 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
[2] Wayne, Wolf: Modern VLSI design: System on Silicon, Pearson Education, 2nd Edition

References:
[1] Douglas A Pucknell & Kamran Eshragian: Basic VLSI Design, PHI, 3rd Edition
[2] Sung Mo Kang & Yosuf Lederabic Law: CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 3rd Edition

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VLSI DESIGN TECHNIQUES			
Course Code:	**EC580**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor Theory and Process Technology
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II: Inverters and Logic Gates
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III: Circuit Characterization and Performance Estimation
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing ,Scaling.

UNIT IV: VLSI System Components Circuits and System Level Physical Design
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V: Verilog Hardware Description Language
Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modelling, data flow modeling, behavioral modeling, task & functions, Test Bench.

Text Books:
[1] Neil H.E. Weste and Kamran Eshraghian: Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
[2] John P.Uyemura: Introduction to VLSI Circuits and Systems, John Wiley & Sons, Inc., 2002.
[3] Samir Palnitkar: Verilog HDL, Pearson Education, 2nd Edition, 2004.

References:
[1] Eugene D.Fabricius: Introduction to VLSI Design McGraw Hill International Editions, 1990.
[2] J.Bhasker, B.S.Publications: A Verilog HDL Primer, 2nd Edition, 2001.
[3] Pucknell: Basic VLSI Design, Prentice Hall of India Publication, 1995.
[4] Wayne Wolf: Modern VLSI Design System on chip, Pearson Education, 2002

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ADVANCED RF ENGINEERING			
Course Code:	**EC544**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF Electronics
Introduction to RF Design and Wireless Technology: Design and Applications,

UNIT II: Complexity and Choice of Technology
Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion

UNIT III: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direct conversion and two-step transmitters. RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation Overview of RF Filter design, Active RF components & modeling,

UNIT V: RF Circuits Design
Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text books:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce: CMOS Circuit Design, layout and Simulation, PHI, 1998.

References:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University Press, 1998.
[2] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996
[3] David M. Pozar: Microwave Engineering, John Wiley & Sons, 2nd Edition, 2003.

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PROBABILITY AND STOCHASTIC PRICESSES			
Course Code:	**EC548**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
Probability models, Algebra of events, probability axioms, conditional probability, Baye's rules, Bernoulli traits. **Discrete Random Variables**: Discrete random variables, probability mass functions, discrete distribution functions-Bernoulli, Binomial, geometric, Poisson, hyper geometric & uniform distributions, probability generating function.

Unit II:
Continuous Random variable: Exponential distribution, memory less property, application to reliability, hypo exponential, Erlang, Gamma, hyper exponential & Normal distributions ,order statistics, distribution of sums.

Unit III:
Stochastic Process, Classification, Discrete and continuous time markov chain, Poisson process, renewal process, littles's formula, Erlang Loss Model, M/M/1 Queue, M/M/m Queue Multidimensional Queue.

Unit IV:
Solution Techniques: Steady-State Solutions of Markov Chains, Solution for a Birth Death Process, Matrix-Geometric Method: Quasi-Birth-Death Process, Heisenberg Matrix: Non-Markovian Queues, Transient analysis, stochastic Petri nets, Numerical Solution: Direct Methods, Numerical Solution: Iterative Methods, Comparison of Numerical Solution Methods, Performance Measures,

Unit V:
Queueing Networks. Definitions and Notation. Performance Measures. Product-Form Queueing Networks. Algorithms for Product-Form Networks, priority Networks.

Reference Books:
[1] Research Methodologies, R. Panneerselvam, Prentice Hall, 2007.
[2] Research in Education, Best John V. and James V Kahn, Wiley eastern, 2005.
[3] Elements of Educational Research, Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra, PHI publication, 2003.
[4] Methodology of Research Education, K. Setia, IEEE publication, 2004.
[5] Research methodology, Methods and Techniques, Kothari, C.R., 2000.

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ADVANCED MICROWAVE COMMUNICATION			
Course Code:	**EC550**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Microwave and Millimeter Wave Devices
Overview of microwave and millimeter wave vacuum tube devices, limitations of microwave vacuum tubes, gyratron vacuum tube devices. Advances in microwave and millimeter wave solid state devices, Gunn devices, oscillator using, Gunn diode, and injection locked oscillators, IMPATT devices, and microwave and mm wave performance of IMPATT. Other solid state devices like Tunnel diode, BARITT and TRAPAT. Microwave and mm wave circuits.

UNIT II: Microwave and MM Wave Circuits
Review of scattering matrix concept in the light of vector network analyzer, impedance matching network, couplers, power dividers, resonators and filters, Detectors, mixers, attenuators, phase shifters, amplifier and oscillator, Ferrite based circuits.

UNIT III: Antennas
Hertzian dipole, loop antenna, helical antenna, frequency independent antenna: Du0Hamel principle, log spiral and log periodic dipole antenna array. Babinet principle, waveguide slot antenna, microstrip antenna, horn antenna, parabolic reflector. Antenna arrays and phased array antenna.

UNIT IV: Satellite Communication
Orbital parameters, satellite trajectory, period, geostationary satellites, non-geostationary constellations. Communication satellites – Space craft subsystems, payload – repeater, antenna, attitude and control systems, telemetry, tracking and command, power sub system and thermal control. Earth stations antenna and feed systems, satellite tracking system, amplifiers, fixed and mobile satellite service earth stations. Terrestrial: line of sight transmission, relay towers and distance considerations. Communication link design: Frequency bands used, antenna parameters, transmission equations, noise considerations, link design, propagation characteristics of fixed and mobile satellite links, channel modeling, very small aperture terminals (VSAT), VSAT design issues.

UNIT V: Microwave and MM Wave Propagation.
Overview of basic radio wave propagation mechanisms, Friis transmission formula, plane earth propagation model, troposcatter systems, ionosphere propagation, duct propagation, microwave radio link and calculation of link budget. Effect on radio wave propagation due to rain, fog, snow, ice, atmospheric gases, Earth's magnetic field.

Text Books:
[1] David M Pozar: Microwave Engineering, John Wiley & Sons
[2] R E Collin, Antenna & Radio wave Propagation, McGraw Hill Book Co.

References:
[1] M Richharia: Satellite Communication Systems,2nd Edition, Macmillan Press Ltd.
[2] Ferdo Ivanek: Terrestrial Digital Microwave Communications, Artech House
[3] E. Hund: Microwave Communications, IEEE Press
[4] Jordan & Balman: Electromagnetic waves & Radiating System
[5] R E Collin: Microwave Engineering, McGraw Hill Co.

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IMAGE PROCESSING AND BIOMETRICS			
Course Code:	**EC418/EC556**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Image Processing and Image Enhancement
Introduction, An image model, sampling & quantization, Basic relationships between Pixels, imaging geometry, Properties of 2 – D Fourier transform, FFT algorithm and other separable image transforms, Components of an image processing System., Digital Image Fundamentals- elements of visual perception, image sensing and acquisition, Basic relationships between pixels
Fundamentals of spatial filtering, smoothing spatial filters (linear and non-linear).

Unit II: Pattern Recognition
Fundamentals of Pattern Recognition, Recognition Measurement, Errors, and Statistics, Recognition measurement and testing, Identification System Errors and Performance Testing, Computer Security, Bayesian decision theory, Multilayer neural networks, Unsupervised Learning and Clustering.

Unit III: Biometrics
Introduction to Biometrics, Fingerprints: Ridges, Furrows, Types of Fingerprints, Image and Signal Processing, Biometric Signal Processing, Other Biometric Modalities, Comparing Biometrics, Passwords, and Tokens, Multimodal Biometrics, Biometric Resources and Standards, Large Scale Biometrics and Systems Case Studies.

Unit IV: Analysis in Biometrics
Large-Scale Biometric Identification: Challenges and Solutions, Issues Involving the Human Biometric Sensor Interface, Fundamentals of Biometric-Based Training System Design, Biometric Systems and Applications, Force Field Feature Extraction for Fingerprint Biometrics, Behavioral Biometrics for Online Computer User Monitoring.

Unit V: Synthesis in Biometrics:
Introduction to Synthesis in Biometrics, Local B-Spline Multiresolution with Example in Iris Synthesis and Volumetric Rendering, image smoothing filters (Butterworth and Guassian low pass filters), image sharpening filters (Butterworth and Guassian high pass filters), selective filtering, Computational Geometry and Image Processing in Biometrics: On the Path to Convergence, **,** A Statistical Model for Biometric Verification.

Text Books:
[1] Practical Algorithms for Image Analysis: Description, Examples, and Code, Seul, O'Gorman, Sammon, 2000.
[2] S. Annadurai and R. Shanmugalakshmi: Fundamentals of Digital Image Processing, Pearson Education.
[3] R. C. Gonzalez and R. E. Woods: Digital Image Processing, 3rd Edition, Pearson Education.
[4] A. K. Jain: Fundamentals of Digital Image Processing, PHI Learning.
References:
[1] M. Sonka, V. Hlavac and R. Boyle: Digital Image Processing and Computer Vision: Cengage Learning.
[2] B. Chanda and D. D. Majumder: Digital Image Processing and Analysis, PHI Learning.
[3] S. Jayaraman, S. Esakkirajan and T. Veerakumar: Digital Image Processing, TMH.

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ADVANCED COMMUNCIATION NETWORKS			
Course Code:	**EC402/EC532**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Digital switching systems-analysis, hierarchy, evolution, SPC, call processing, communication and control- level 1,2,& 3 control, interface control, network control processor, central processor, control architecture, multiplexed highways, switching fabric-space division switching, time division switching, STS, TST, TTT, switching system software-architecture, OS, database management

Unit II: MPLS-label stack and label distribution, traffic engineering, design of switching systems, and routers, switching networks-crossbar switches, multistage switches, shared memory switches, optical networks, DWDM techniques, IP over optical core switches

Unit III: Congestion control: integrated services, differentiated services, congestion control, congestion control in packet switching, frame relay congestion control, flow control at link level, TCP congestion control

Unit IV: Voice over IP: basic IP telephone system, digital voice sampling, compression techniques, protocol for VoIP, session initiation protocol

Unit V: Internetworking-connection mode network service, x.75 internetworking, network through ISDN, internetworking SNA, and x.25, x.300 internetworking standards, personal computer networking, data transmission in PTN, Data network standards, voice-data integration, fast packet switches

Text books:

[1] Syed R. Ali, " Digital Switching Systems, System Reliability and analysis, Tata McGraw-Hill
[2] William Stallings, " High Speed Networks and Internet" 2nd ed. Perason edu, 2005
[3] Bellamy John, " Digital Telephony" Wiley 3rd Ed, 2000
[4] Viswanathan, T, "Telecommunications Switching Systems and Networks, " PH

References:

[1] Andrew S. Tanenbaum: Computer networks, PHI.
[2] W. Stallings: Data and computer communications, MC, Milan.
[3] Alberto Leon-Gercia, India Widjaja: Communication networks, fundamental concepts and key architecture, TATA McGraw Hill.
[4] Bertsekas D. and Gallager R.: Data Networks, PHI.
[5] Keshav S: An Engineering Approach to computer Networking, Addison Weslay.

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LOW POWER VLSI DESIGN			
Course Code:	**EC633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

UNIT II: Device & Technology Impact on Low Power
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III: Power estimation
Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT IV: Low Power Design
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT V: Low power Architecture & Systems
Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text Books:
[1] Gary K. Yeap: Practical Low Power Digital VLSI Design, KAP, 2002
[2] Rabaey and Pedram: Low power design methodologies, Kluwer Academic, 1997

References :
[1] Kaushik Roy, Sharat Prasad: Low-Power CMOS VLSI Circuit Design, Wiley, 2000
[2] J. B. Kulo and J.H Lou: Low voltage CMOS VLSI Circuits, Wiley 1999.
[3] A.P. Chandrasekaran and R.W. Broadersen: Low power digital CMOS design, Kluwer, 1995.
[4] Abdelatif Belaouar, Mohamed.I. Elmasry, "Low power digital VLSI design, Kluwer, 1995.

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DESIGN LAB III			
Course Code:	**EC683**	**Credits:**	**3**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to simulation software ANSYS using GUI.
2. Introduction to simulation software ANSYS using Command lines.
3. Performing a Harmonic Response Analysis using ANSYS.
4. Realization of a Force Sensor using ANSYS.
5. Multiphysics Analysis of a Thermal Actuator using ANSYS.
6. Piezoelectric Analysis using ANSYS.
7. Introduction to MEMS Design using ANSYS.
8. Electromechanical Analysis of an Optical Brag Reflector using ANSYS.

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RESEARCH TECHNIQUES IN ICT			
Course Code:	**CS633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I : Introduction to Research Techniques
Meaning of research, objectives of research, motivation in research, types of research-Introduction to experimental test bed, algorithmic research, simulation research, mathematical modeling approach, characteristics and prerequisites of research, significance of research, research process, Sources of research problem, criteria of identifying the problem, necessity of defining the problem, errors in selecting research problem, technique involved in defining the problem, Report and paper writing

Unit II: Data Analysis and Statistical Techniques
Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminant analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis.

Unit III: Random Numbers and Variates
Properties of random numbers, generation, tests for random numbers, random-variate generation
Inverse Transform technique, direct transformation, convolution method, acceptance-rejection Technique, Probability distributions functions, Moments, moment generating functions, joint distributions, marginal and conditional distributions, functions of two dimensional random variables Poisson process-Markovian queues, single and multi server models, Little's formula, steady state analysis

Unit IV: Algorithmic Research
Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments,

Unit V: Simulation and Soft Computing Techniques
Introduction to soft computing, Artificial neural network, Genetic algorithm, Fuzzy logic and their applications, Tools of soft computing, Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, verification of simulation models, calibration and validation of models, Output analysis, introduction to MATLAB, NS2, ANSYS, Cadence

Text Books:
[1] R. Panneerselvam: Research Methodologies, PHI
[2] Jerry Banks, John S. Carson, Barry.L. Nelson David. M. Nicol: Discrete-Event System Simulation, Prentice-Hall India
[3] Donald Gross, Carl M. Harris: Fundamentals of Queueing Theory, 2nd Ed. John Wiley and Sons, New York,

References:
[1] Best John V. and James V Kahn: Research in Education, Wiley eastern, 2005.
[2] Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra: Elements of Educational Research, PHI publication, 2003.
[3] K. Setia: Methodology of Research Education, IEEE publication, 2004.
[4] Kothari, C.R.: Research methodology, Methods and Techniques, 2000.

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VLSI ASIC DESIGN			
Course Code:	**EC665**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I : Introduction to ASICs, CMOS Logic and ASIC Library Design
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II: Programmable ASICs, Programmable ASIC Logic Cells and ASICs I/O Cells.
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III: Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV: Logic Synthesis, simulation and Testing
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation- boundary scan test - fault simulation - automatic test pattern generation.

UNIT V: ASIC Construction, Floor Planning, Placement and Routing
System partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC.

Text Books:
[1] M.J.S .Smith, Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
[2] Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.

References:
[1] Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
[2] R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House, 2000.

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MICRO AND SMART SYSTEM TECHNOLOGY			
Course Code:	**EC667**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT 1: Introduction to Micro and Smart Systems
Smart-material systems, Evolution of smart materials, structures and systems, Components of a smart system, Application areas, Commercial products, Microsystems, Feynman's vision, Micromachined transducers, Evolution of micro-manufacturing, Applications.

UNIT II: Micro and Smart Devices and Systems: Principles and Materials:
Microsensors, silicon capacitive accelerometer, resonant accelerometer, piezo-resistive pressure sensor, capacitive pressure sensor, inertial sensor, sensor for munitions, microresonator, tunable rf filters, actuators, , microvalve/micropumps, microactuator, microgripper, detectors, flow sensor, accelerometer, gyros sensor, enhanced jet engine, chemical sensor, biosensors, DNA chips, micro thruster, CNT.

UNIT III: Micromanufacturing and Material Processing
Materials: types, mechanical properties, electronics properties and optical properties. Processing of other materials: ceramics, polymers and metals, silicon wafer processing, lithography, nanolithography, micro contact printing lithography, thin-film deposition, etching (wet and dry), TMAH etching, LIGA, laser ECE, wafer-bonding, and metallization, Silicon micromachining: surface, bulk, moulding, bonding based process flows, Thick-film processing, Smart material processing, Emerging trends.

UNIT IV: Modeling, Design and Simulations
Scaling issues, Elastic deformation and stress analysis of beams and plates, Residual stresses and stress gradients, Thermal loading, Heat transfer issues, Basic fluids issues, Electrostatics. Coupled electromechanics. Electromagnetic actuation, Capillary electro-phoresis. Piezoresistive modeling, Piezoelectric modeling. Magnetostrictive actuators,finite element method overview.

UNIT V: Advanced Topic
Micro and smart system based switches for RF and Microwave applications, inductors and capacitors, RF filters, phase shifters, transmission lines and components, antenna, integration and packaging.

Text Books:
[1] MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill.
[2] RF MEMS and their applications, V.Varadan, K. J. Vinoy, K.A. Jose, Wiley.

References:
[1] Microsystems Design, S. D. Senturia, Kluwer Academic Publishers, 2001.
[2] Analysis and Design Principles of MEMS Devices, Minhang Bao, Elsevier
[3] Design and Development Methodologies, Smart Material Systems and MEMS: V. Varadan, K. J. Vinoy, S. Gopalakrishnan, Wiley.
[4]MEMS- Nitaigour Premchand Mahalik, TMH 2007

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ADVANCES IN VLSI DESIGN			
Course Code:	**EC669**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.MESFET and MODFET operations, quantitative description of MESFETS.MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

UNIT II: Short channel effects and challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

UNIT III: Beyond CMOS
Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing.

UNIT IV : Super buffers, Bi-CMOS and Steering Logic
Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

UNIT V: Special circuit layouts & technology mapping and System Design
Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out. CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

Text Books:
[1] Kevin F Brrnnan Introduction to semi conductor device, Cambridge Publications
[2] Eugene D Fabricius Introduction to VLSI design, McGraw-Hill International Publications

References:
[1] D.A Pucknell Basic VLSI design, PHI Publication
[2] Wayne Wolf, Modern VLSI Design Pearson Education, Second Edition, 2002

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MODERN OPTIMIZATION TECHNIQUES			
Course Code:	**EC671**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Artificial Neural Networks (ANN)
Objectives-History-Biological inspiration, Neuron model, Single input neuron, Multi-input neuron, Network architecture, Single layer of neurons, Multi-layers of Neurons.

UNIT II: Perceptron and Learning
Perceptron architecture, Stingle-neuron perceptron, Multi-neuron perceptron- Perceptron Learning Rule, Constructing learning rules, Training multiple neuron perceptrons. Associative Learning: Simple associative network, Unsupervised Hebbrule- Hebb rule with decay, Instar rule, Kohonen rule. Widro-Hoff Learning: Adaline Network, Single Adaline, Mean square Error, LMS algorithm, Analysis of Convergence.

UNIT III: Neural Network Roles in VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Time Series and Forecasting.

UNIT IV: Genetic Algorithms and its Mathematical Foundations
Introduction, robustness of traditional optimization and search methods, goals of optimization, difference between genetic algorithms and traditional methods, a simple genetic algorithm, hand simulation, Grist for the search mill, similarity templates, learning the lingo. Foundation theorem, schema processing, the two armed and k-armed bandit problem, schemata processing, building block hypothesis, minimal deceptive problem (MDP), extended schema analysis, MDP results, similarity templates as hyper planes.

UNIT V: Advanced Topics
Data structures, reproduction, crossover and mutation, a time to reproduce and a time to cross, main program and results, mapping objective functions to fitness form, fitness scaling, codings, a multiparameter mapped fixed point coding, discretization, constraints.

Text Books:
[1] Neural Network Design, PWS publishing company, 1995.
[2] Introduction to Artificial Neural Systems, Jaico Pub.House, Bombay, 1994.
[3] Neural Computing : Theory and practice, Van Nastrand Reinhold, 1989.

References
[1] Haykin S., Neural Networks-A Comprehensive Foundations, Prentice-Hall International, New Jersey, 1999.
[2] Freeman J.A., D.M. Skapura, Neural Networks: Algorithms, Applications and Programming Techniques, Addison-Wesley, Reading, Mass, (1992).
[3] Golden R.M., Mathematical Methods for Neural Network Analysis and Design, MIT Press, Cambridge, MA, 1996.

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VLSI-RELIABILTY ENGINEERING			
Course Code:	**EC673**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Probability Plotting and Load- Strength Interference
Statistical distribution , statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II: Reliability Prediction, Modeling and Design
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III: Electronics and Software System Reliability
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV: Reliability Testing and Analysis
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V Manufacture and Reliability Management
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

Text Books:
[1] Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
[2] David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, AT & T Reliability Manual, 5th Edition, 1998.

Reference:
[1] Gregg K. Hobbs, Accelerated Reliability Engineering - HALT and HASS, John Wiley & Sons, New York, 2000.

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SENSOR NETWORKS			
Course Code:	**EC647**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Sensor Network Operations
Overview of mission-oriented sensor networks, trends in sensor development, mission oriented sensor networks, dynamic systems perspective, Dense sensor networks, robust sensor positioning in wireless ad hoc sensor networks, trigonometric k clustering (TKC) for censored distance estimation, sensing coverage and breach paths in surveillance wireless sensor networks.

UNIT II: Lower Layer Issues-MAC, Scheduling, and Transmission
Medium access control for sensor networks, comprehensive performance study of IEEE 802.15.4, providing energy efficiency for wireless sensor networks, link adaptation techniques.

UNIT III: Network Routing
Load balanced query protocols for wireless sensor networks, energy efficient and MAC aware routing for data aggregation in sensor networks, ESS low energy security solution for large-scale sensor networks based on tree ripple zone routing scheme.

UNIT IV: Sensor Network Applications
Evader centric program, Pursuer centric program, hybrid pursuer evader program, efficient version of hybrid program, Implementation and simulation results

UNIT V: Embedded Soft Sensing for Anomaly Detection
Mobile robot simulation setup, software anomalies in mobile robotic networks, soft sensor, software anomaly detection architecture, anomaly detection mechanisms, test bed for software anomaly detection in mobile robot application, multisensor network-based framework; Basic model of distributed multi sensor surveillance system, super resolution imaging, optical flow computation, super resolution image reconstruction, experimental results.

Text Books:
[1] Sensor Network Operations, Shashi Phoha, Thomas F. La Porta , Chrisher Griffin, Wiley-IEEE Press March 2006.
[2] Wireless sensor networks, Jr. Edger H. Callaway, CRC Press.

References:
[1] Wireless Sensor Networks, I. F. Akyildiz and M. C. Vuran, John Wiley and Sons Publ. Company
[2] Wireless Sensor Networks: An Information Processing Approach, Feng Zho, Morgan Kaufmann

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MIXED SIGNAL VLSI DESIGN			
Course Code:	**EC519/EC675**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Signals, Filters, and Tools
Sinusoidal Signals, Pendulum Analogy, Amplitude in the x-y Plane, In-Phase and Quadrature Signals, Complex (z-) Plane, Comb Filters, Digital Comb Filter, Digital Differentiator, Intuitive Discussion of the z-Plane, Comb Filters with Multiple Delay Elements, Digital Integrator, Delaying Integrator, Exponential Fourier Series, Fourier Transform, Dirac Delta Function .

Unit II: Sampling and Aliasing
Sampling, Impulse Sampling, Time Domain Description of Reconstruction, Decimation, Sample-and-Hold, S/H Spectral Response, Reconstruction Filter, Circuit Concerns for Implementing the S/H, Track-and-Hold (T/H), Interpolation, Zero Padding, Hold Register, Linear Interpolation, K-Path Sampling, Switched-Capacitor Circuits, Non-Overlapping Clock Generation, Circuits Implementing the S/H, Finite Op-Amp Gain-Bandwidth, Auto zeroing,

Unit III: Analog Filters
Integrator Building Blocks, Lowpass Filters, Active-RC Integrators, Effects of Finite Op-Amp Gain Bandwidth Product, Active-RC SNR, MOSFET-C Integrators, gm-C Integrators, Common-Mode Feedback Considerations, High-Frequency Transconductor, Discrete-Time Integrators, Frequency Response of an Ideal Discrete-Time Filter, Filtering Topologies, Bilinear Transfer Function, Active-RC Implementation, Transconductor-C Implementation.

Unit IV: Digital Filters
Models for DACs and ADCs, Ideal DAC, Modeling of Ideal DAC, Ideal ADC, Number Representation, Increasing Word Size, Adding Numbers and Overflow, Two's Complement Sinc-Shaped Digital Filters, Counter, Aliasing, Accumulate-and-Dump, Lowpass Sinc Filters, Averaging without Decimation, Cascading Sinc Filters, Finite and Infinite Impulse Response Filters, Bandpass and Highpass Sinc Filters, Frequency Sampling Filters.

Unit V: Data Converter SNR
Quantization Noise, Quantization Noise Spectrum, Bennett's Criteria, RMS Quantization Noise Voltage, Quantization Noise as a Random Variable, Quantization Noise Voltage Spectral Density, Power Spectral Density, SNR, Effective Number of Bits, Coherent Sampling, SNDR, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter.

Text Books:
[1] Jacob Baker, CMOS Mixed Signal Circuit Design, TMH

References:
[1] Yannis Tsividis ,"Mixed Analog-Digital VLSI Device and Technology", Wiley
[2] Roubik Gregorian ,"Introduction to CMOS Opamps and Comparators",TM

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DSP INTEGRATED CIRCUITS			
Course Code:	**EC521/EC677**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: DSP Integrated Circuits and VLSI Circuit Technologies
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

Unit II: Digital Signal Processing
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

Unit III: Digital Filters and Finite Word length Effects
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

Unit IV: DSP Architectures and Synthesis of DSP Architectures
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Unit V: Arithmetic Units and Integrated Circuit Design
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

Text Books:
[1] Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
[2] A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.

References:
[1] Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
[2] Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

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ADVANCED DIGITAL VLSI DESIGN			
Course Code:	**EC679**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Basic principle of MOSFETs, Introduction to large signal MOS models (long channel) for digital design. The MOS Inverters: Static and Dynamic characteristics: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, transition time, Propagation Delay, Power Consumption.

UNIT II: MOS Circuit Layout & Simulation
Layout design rules, MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation, Circuit Compaction; Circuit extraction and post-layout simulation.

UNIT III: Combinational MOS Logic Design
Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits, DSL, DCVSL, Transmission gate logic. Dynamic MOS design: Dynamic logic families and performances. Memory Design: ROM & RAM cells design

UNIT IV: Sequential MOS Logic Design
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Adders, Multiplier Circuits.

UNIT V: Interconnects & IO Buffers and BiCMOS Logic Circuits
Interconnect delays, Cross Talks. Introduction to low power design, Input and Output Interface circuits. BiCMOS Logic Circuits: Introduction, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits.

Text Books:
[1] Kang & Leblebigi CMOS Digital IC Circuit Analysis & Design- McGraw Hill, 2003
[2] J.M. Rabey, Digital Integrated Circuits Design, Pearson Education, Second Edition, 2003
[3] Weste and Eshraghian, Principles of CMOS VLSI design Addison-Wesley, 2002

Reference:
[1] W Wolf Modern VLSI Design.
[2] David A. Hodges, Horace G. Jackson, Resve Saleh, Analysis & Design of Digital Integrated Circuits, 3rd Edi Mc Graw Hill, 2003.

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TEST AND VERIFICATION OF VLSI CIRCUITS			
Course Code:	**EC681**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Basic Concepts, Functional Modeling: Truth table and primitive cubes, Binary decision diagrams, Basic RTL constructs, Timing Modelling, Structural Modeling: External Representations Structural Properties, Internal representations, Wired Logic and bidirectionality.

UNIT II: Logic Simulation
Types of simulations, The unknown logic values, Complied simulation, Event driven simulation Delay Models for gates, Element Evaluation, Hazard Detection, Tristate Logic, MOS Logic, other delay models: Rise and Fall Delays, Inertial Delays, Ambiguous Delays, Oscillation Control.

UNIT III: Fault Modeling and Simulation
Logical Fault Models, Fault Detection and Redundancy: Combinational Circuits, Sequential Circuits, Fault Equivalence and Fault location: Combinational Circuits, Sequential Circuits, Fault Dominance, Single stuck Fault model, Multiple stuck at Fault model, General Fault Simulation Techniques: Serial Fault, Parallel Fault, Deductive Fault, Concurrent Fault, Fault Simulation for Combinational Circuits.

UNIT IV: Testing for Faults
Basic Issues, ATG for SSFs in Combinational Circuits: Fault Oriented ATG, Common Concepts, Algorithms, Selection Criteria, Fault Independent ATG, Random Test Generation, Combined Deterministic/Random Test Generation, ATG for single stuck at faults in sequential Circuits, Bridging Fault model, Detection of feedback and non feedback Bridging Faults.

UNIT V: Design for Testability
Testability: Tradeoffs, Controllability and Observability, Ad Hoc Design for Testability Techniques: Test points, Initialization, Monostable multivibarators, Oscillators and Clocks, Controllability and Observability by means of scan registers, Generic scan based designs.

Text Books:
[1] Digital Systems Testing & Testable Design, Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman.
[2] An Introduction to Logic Circuit Testing, Parag K Lala

REFERENCE BOOKS
[1] VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon), Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen.

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EM INTERFERENCE AND CAPABILITIES IN SYSTEM DESIGN			
Course Code:	**EC661**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Basic EMC concepts at IC level
Introduction , Definition of EMC, EMI, EMS and EME, Sources of electromagnetic interference, Electromagnetism versus integrated circuit design, Electrical length, Near field versus far field, Radiation of a conductor , Basic EMC antenna concepts, Radiated, induced and conducted disturbances, Practical example, Intra-chip versus externally-coupled EMC, EMC in automotive applications.

UNIT II: EMC of Integrated Circuits and Distortion
Relationship between EMI resisting design and distortion , Linear distortion, Nonlinear distortion (rectification) , Weak and strong nonlinear distortion, diode connected NMOS transistor , NMOS source follower, NMOS current mirror, Capacitor decoupling the mirror node, Low-pass *R-C* filter in the mirror node , EMI resisting (4-transistor) current mirror , EMI resisting (Wilson totem pole) current mirror , Comparison of EMI susceptibility of current mirrors , EMI susceptibility in ESD protections.

UNIT III: EMI Resisting Analog output circuits
Categorization of analog output structures, Common-drain output circuits, Common-source output circuits, Comparing the electromagnetic susceptibility, Large EMI amplitudes, EMI resisting DC current regulator , EMI issues in a classic DC current regulator, EMI issues: small signal analysis large signal analysis, Decoupling capacitor *Cd* , DC current regulator with a high immunity to EMI Measurements.

UNIT IV: EMI Resisting Analog input circuits
Electromagnetic immunity of CMOS operational amplifiers, Asymmetric slew rate, Strong nonlinear behaviour of the input differential pair, Weak nonlinear behaviour of the input differential pair, EMI induced offset in a classic differential pair , Classic differential pair using source degeneration, Cross-coupled differential pair, Differential pair with low-pass *R-C* filter, Improved cross-coupled differential pair, Source-buffered differential pair, Comparison, EMI induced offset measurement setups, Measurements.

UNIT V: Advance Topics
CMOS bandgap voltage references with a high immunity to EMI, EMI injection in a bandgap reference, Small signal analysis, Large signal analysis, EMI resisting bandgap reference , Small signal analysis , Large signal analysis, EMI resisting bandgap reference, Small signal analysis, Large signal analysis, Startup circuit and biasing, Measurements.

Text Books:
[1] EMC of Analog Integrated Circuits, Jean-Michel Redoute, Michiel Steyaert

References:
[1] Electromagnetic compatibility of integrated circuits: techniques for low emissions and susceptibility, Sonia Ben Dhia, Mohamed Ramdani, Étienne Sicard.
[2] Electromagnetic Compatibility Engineering , Henry Ott.

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ALGORITHM FOR VLSI DESIGN AUTOMATION			
Course Code:	**EC685**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction

Architectural Design , Logic Design, Physical Design , Full-custom Layout**,** Gate-array Layout, Standard-cell Layout Macro-cell Layout, Programmable Logic Arrays, FPGA layout**,** Difficulties in Physical Design, Problem Subdivision, Computational Complexity of Layout Subproblems, Solution Quality, Nets and Netlists, Connectivity Information, Weighted Nets, Grids, Trees, and Distances.

UNIT II: Circuit Partitioning and Floorplanning

Cost Function and Constraints: Bounded Size Partitions, Minimize External Wiring, Approaches to Partitioning Problem: Kernighan-Lin Algorithm, Variations of Kernighan-Lin Algorithm, Fiduccia Mattheyses Heuristic, Simulated Annealing, Floorplanning Model, Approaches to Floorplanning, Cluster Growth ,Simulated Annealing ,Analytical Technique , Dual Graph Technique.

UNIT III: Placement

Complexity of Placement , Problem Definition , Cost Functions and Constraints: Estimation of Wirelength, Minimize Total Wirelength , Minimize Maximum Cut , Minimize Maximum Density, Maximize Performance, Other Constraints, Approaches to Placement: Partition-Based Methods, Limitation of the Min-cut Heuristic, Simulated Annealing , Numerical Techniques.

UNIT IV: Routing

Problem Definition, Cost Functions and Constraints: Placement Constraints , Number of Routing Layers Geometrical Constraints, Maze Routing Algorithms: Lee Algorithm, Limitations of Lee Algorithm for Large Circuits ,Connecting Multi-point Nets ,Finding More Desirable Paths, Further Speed Improvements, Line Search Algorithms, Other Issues: Multi Layer Routing , Ordering of Nets , Rip-up and Rerouting, Power and Ground Routing.

UNIT V: Advanced Topics

Cost Functions and Constraints , Routing Regions: Routing Regions Definition, Routing Regions Representation, Sequential global Routing: The Steiner Bee Problem, Global Routing by Maze Running, Integer Programming ,Global Routing by Simulated Annealing : The First Stage , The Second stage, Hierarchical Global Routing.

Text Books:

[1] VLSI physical design automation: theory and practice, By Sadiq M. Sait, Habib Youssef.

[2] Algorithm for VLSI physical design automation by Naveed A. Sherwani.

References:

[1] Essential Electronic Design Automation (EDA), Mark D Birnbaum.

[2] Physical Design Automation for VLSI systems, Bryan D Ackland.

[3] Practical Problems in VLSI Physical Design Automation, Sung Ku Lim.

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SMART ANTENNA SYSTEMS			
Course Code:	**EC643**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Basic Concepts of Radiation
Radiation mechanism: Basic sources of Radiation- Current distribution on antennas, Basic antenna parameters.

UNIT II- Analysis and Synthesis of Antennas
Vector potential, Antenna theorems and definitions, dipole, loop, reflector, slot antennas. Types of linear arrays, current distribution in linear arrays, Antenna array synthesis techniques.

UNIT III Smart Antennas
Spatial processing for wireless systems: Introduction, Vector channel impulse response & the spatial signature. Spatial processing receivers, fixed beam forming Networks, switched beam systems, Adaptive antenna systems, Wide band smart antennas, Digital radio receiver & software radio for smart antennas.

UNIT IV- Smart Antenna Techniques for CDMA
Non-coherent & coherent CDMA spatial processors, spatial processing rake receiver, Multi-user spatial processing, dynamic resectoring, down link beam forming for CDMA, MIMO.

UNIT V: Microstrip Antenna
Radiation Mechanism and Excitation techniques : Microstrip dipole; Patch ,Rectangular patch, Circular patch, and Ring antenna – radiation analysis from cavity model; input impedance of rectangular and circular patch antenna; Microstrip array and feed network; Application of microstrip array antenna.

Text Books:
[1] Balanis A., Antenna Theory Analysis and Design, John Wiley and Sons, New York, 1982.
[2] Joseph C. Liberti, Theodore S. Rappaport – Smart Antennas for Wireless Communications: IS95 and third generation CDMA Applications, Prentice Hall, Communications Engineering and Emerging Technologies Series.

References:
[3] I.J. Bahl and P. Bhartia, Microstrip Antennas,Artech House,Inc.,1980
[4] W.L.Stutzman and G.A.Thiele,Antenna Theory and Design, 2nd edition,John Wiley& Sons Inc.,1998.