ICIAICT 2012 **TRACK V (VLSI DESIGN)** **Session: VLSI-I**

Venue: I- 205 **Date: 30/03/12** **Time: 2:30pm- 04:00pm**

S.No	Paper ID	Name of the Authors/Title of the Papers
1	VLSI 135	**HARSHI TOMAR TANYA SHARMA SANDEEP KUMAR SANDEEP SHARMA**
		A SIMULATION BASED APPROACH TOWARDS THE TEMPERATURE MONITORING FOR THE E-JACKET
2	VLSI 136	**RAVINDAR KUMAR GURJIT KAUR DEEPAK KEDIA**
		REDUCTION TECHINQUE OF POWER DISSIIPATION OF 6T SRAM CELL USING SLEEP TRANSISTOR IN CADENCE VIRTUOSO TOOL
3	VLSI 137	**MANGEY RAM NAGAR NAVAID Z. RIZVI RAAZIYAH SHAMIM**
		HIGH SPEED POWER EFFICIENT WALLACE TREE ADDERS
4	VLSI 109	**SHIPRA UPADHYAY R. A. MISHRA and R.K. NAGARIA**
		COMPARATIVE PERFORMANCE OF IRREVERSIBLE ADIABATIC LOGIC CIRCUITS FOR LOW POWER VLSI DESIGN
5	VLSI 110	**NEERAJ YADAV SANJEEV AGRAWAL JAYESH RAWAT CHANDAN KUMAR JHA**
		LOW-VOLTAGE CURRENT MIRROR BASED ON DIFFERENT TECHNIQUES
6	VLSI 111	**ANIL KUMAR CHAUDHARY SANJAY KUMAR SINGH NISHANT TRIPATHI S. C. AGRAWAL**
		RELIABILITY COMPARSION OF INVERTERS IN HYBRID ELECTRICAL VEHICLES UNDER DIFFERENT SWITCHING PATTERN
7	VLSI 133	**PRABHASH SINGH MD. TAUHEED KHA DEEPIKA YADAV SANJAY SINGH YADAV MOHIT KUMAR SINGH**
		EFFECT OF WIDTH VARIATION OF COUPLED INDUCTIVE VLSI INTERCONNECT LINE ON TRANSITION TIME AND CROSSTALK NOISE

S.No.	Paper ID	Name of the Authors/Title of the Papers
8	VLSI 112	**GARIMA KULSHRESHTHA, RICHA BANSAL**
		DESIGN & CHARACTERIZATION OF LOW POWER SRC CMOS- BUFFER
9	VLSI 118	**VINAY KUMAR YADAV, ASHWANI KUMAR RANA**
		IMPACT OF GATE LENGTH ON NANO SCALE DG-MOSFET PERFORMANCE PARAMETERS- TCAD SIMULATION
10	VLSI 120	**PRADEEP SINGLA NAVEEN KUMAR MALIK**
		REVERSIBLE PROGRAMMABLE LOGIC ARRAY (RPLA) USING FEYNMAN & MUX GATES FOR LOW POWER INDUSTRIAL APPLICATIONS
11	VLSI 121	**SUNIL KUMAR SINGH, R. K. SINGH, M. P. S. BHATIA**
		CAD FOR AUTOMATIC LOGIC DENSITY UTILIZATION OF SYMMETRICAL FPGA ARCHITECTURE THROUGH HYBRID LUTS/PLAS
12	VLSI 126	**KIRAT PAL SINGH DILIP KUMAR**
		EFFICIENT HARDWARE DESIGN AND IMPLEMENTATION OF ENCRYPTED MIPS PROCESSOR
13	VLSI 127	**ALE IMRAN**
		DESIGN & PERFORMANCE ANALYSIS OF BULK CMOS DUAL-X CCII IN DEEP SUBMICRON NODE
14	VLSI 105	**ANIE JAIN, SHYAM BABU, SHYAM AKASHE**
		EFFECTS OF DUAL VTH ON LEAKAGE POWER CONSUMPTION IN A CONVENTIONAL CMOS 6T-SRAM BIT-CELL AT 45NM TECHNOLOGIES
15	VLSI 102	**RITIKA SAXENA, GARIMA SHARMA, SHOBHIT SAXENA, AVNEESH MITTAL, ALOK BHATNAGAR, T.K. SAXENA**
		DESIGN AND DEVELOPMENT OF LOW COST SPEED CONTROLLER FOR BLDC MOTOR OF SOLECKSHAW USING 89C51 MICROCONTROLLER
16	VLSI 103	**VIJAY SHARMA AVNEESH MITTAL, SANJEEV BAJAJ, T.K. SAXENA**
		UPGRADATION OF LARGE SIZE OEDOMETER AND PERMEABILITY EQUIPMENT TO MAKE IT FULLY COMPUTER CONTROLLED UNATTENDED SYSTEM