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Experience Summary Most recent experiences in Memory Design, SOC design, Analog ASIC. Thorough experiences in CMOS library design, digital systems, communications, DSP products, board design.

Education Ph.D. (Computer Engineering) 1992, University of Nebraska-Lincoln, NE.
Thesis – Accurate Computation of chip reject ratio based on fault latency

M.Tech. (EE with Communication emphasis) 1975, IIT Kanpur, India

B.Tech. (EE) 1973,IIT Kanpur, India

Employers Tata consultancy Services, Bombay (assignments with Burroughs – Detroit, Hewlett Packard Cupertino, Texas Instruments – Dallas), Cadence Design Systems Noida, HCL Technologies, Neomagic Noida.

Experience

07/04-03/09 **Virage Logic, Noida**

Worked and managed all aspects of memory design. Have a very good handle on physical design using Laker and Virtuoso. Recently completed assignments are described below.

NEC CODS – NEC service project to fine tune NEC's memory compiler system for development of 55nm memories. Required updating Skill routines to generate instance lvs netlist and characterization netlist from cadence schematic database.

Implementation of ULP techniques in existing 65 nm compilers, to make the memory competitive with respect to power consumption. Incorporated dual voltage rail for periphery and array, source biasing in the array, and selective high Vt implant in logic. Development of autochar setup for accurate power measurement based on tiledC approach.

Management responsibilities
Design migration across foundries and technology nodes- Single and Dual port high density SRAMs, register files and ROMs on 130, 90, 65 nm and half nodes. Work content includes feasibility study, bitcell analysis, modifications to meet design margins, minarray development, layout migration and development, compiler characterization and compiler engineering effort requiring placement file enhancements, and functional verification, qa.

In line R&D work for off the shelf memory products – (a) Implementing architectural changes in moving from side decode to center decode and one bank to multibank design. (b) Establishing tradeoffs in bit-line and word-line tracking. (c) Implementing low leakage techniques in advanced technology nodes, (d) resolving silicon debug issues.
Layout development, measure statement development for design margins, compiler engineering and characterization.

Work in progress – development of optimization techniques to improve the performance of scaled designs (65nm to 45nm).

09/02-06/04 **Neomagic, Noida**

Design Manager for IP hardening for ARM9 based applications processor for multi-media

application. RTL to GDS implementation for Neomagic's MiMagic6 multimedia chip.

Evaluate and re-architect vendor provided platform libraries for high performance and low leakage, to meet end product specs.

02/02-08/02 **HCL Technologies Ltd. Gurgaon**

Working as a Senior Consultant with HCL Technologies, my job was to provide design services to HCL clients. Following are the projects handled by me:

Analog ASIC for optoelectronic applications, proposal development, design and relationship management with foundry.

Flow engineering for DSP product development in Matlab and implementation on Motorola 58K DSP development board.

ASIC Physical Design Services provided to HCL clients (Calix, Chorum Electronics)

06/93-01/02 **Cadence Design Systems (India**)

Signal Processing WorkSystem (DSP oriented design environment)

Track Market Requirements Document to provide new features and enhancements in SPW's Library as detailed below. Complete ownership of content planning, feasibility, development, release management and continual support.

Matrix Library – LU Decomposition, QR Decomposition, Eigenvalue, Eigenvector, Singular value decomposition, Pseusoinverse, Overdetermined Solve, Underdetermined Solve, Toeplitz matrix system

Responsibility - Enhanced the simulation capability of the SPW to process Matrix samples as compared to scalars, for rapid design space exploration. This method provided a mechanism to implement advanced DSP algorithms required in adaptive signal processing, speech coding algorithms, spectral estimation and multi-rate systems. Development of demo systems to showcase the novel Matrix Library features

Encoder/Decoder library – Block and Convolution error correcting codes.

Responsibility – Develop simulation models of various error correcting coding-decoding schemes to capture the effect of non-linearity and non-additive and non-Gaussian noise sources to effectively evaluate the performance of coded communication systems. Enhanced the library to include Turbo codes.

Communications Toolkit – Source Encoders/Decoder, Baseband Modulation, Formatting and Line Coding, RF Modulation, Demodulation, Filtering, Error Control Coding, Synchronization

Responsibility – Given the fixed-point and parametric simulation models of blocks in the communication library, develop behavioral VHDL generators (a C++ class library). Use *Visual Architect* (*A Cadence behavioral synthesis tool)* to develop optimized synthesizable RTL descriptions. Characterize the RTL library for timing and area. Bundled as *Communications Toolkit* with *HDS (Hardware development system for SPW)*, enabling seamless implementation of various communications domain products as ASICs.

DSP Generators – FIR, IIR Filters, Interpolation and Decimation filters, DFT, DCT Rake Receiver.

Responsibility – Develop C++ class library to generate behavioral VHDL for application specific DSP modules. Behavioral VHDL code is synthesized by *Visual Architect*. User has the ability to specify the implementation architecture and topology of the DSP modules. Cordic algorithm is used for mathematical implementation of the DSP.

Polymorphic Communications Library – Basic communications library blocks, technology specific blocks (CDMA, OFDM, WLAN)

Responsibility – Re-architect the communications library in terms of basic communications system blocks, technology oriented blocks, and application specific libraries. Provide polymorphic (C++ based) capability to change block type between floating point and fixed point, data type to real or complex, and data container type to be scalar, vector and matrix. Developed reference systems based on the library to provide Verification Environment for Wireless Standards.

BONes : (Tool for modeling behavior of communication network) Provided support for developing new network modules such as traffic generators, LAN segments, interconnects etc. Develop TCP/IP verification environment.

Spectrum Services: Managed the development of front end model generators for Application specific embedded memories (RAMs, and ROMs). Kawasaki Steel Company was the Spectrum Services Client for this work.

Physical Systems Group (Allegro Product): Developed methodology for EMI measurement of high speed PCBs based on EM simulation Allegro is the PCB layout and analysis tool.

01/88-12/92 **University of Nebraska-Lincoln**

PhD Student (Research in VLSI Test)
Teaching Assistant: Instructor with full teaching responsibilities for various courses in EE/Comp.Sci.
Research Assistant for analyzing electromagnetic fields surrounding high Tc superconductors and electromagnetic scattering from rough surfaces.

08/75-12/87 **Tata Consultancy Services, Bombay**
Field Engineering('75-'83): TCS as a distributor of Burroughs Machines in India sold B6700, B6800, B6900 (Large systems) B4700/4800 (Medium systems), B1700 (Small systems) to various organizations in India. As a field engineer for Burroughs systems, provided Site planning and development, Installation, Maintenance and User Support of Burroughs Mainframe computers at various sites in India (1975-1982)

Board Design('82-'83): Acquired board design experience while working as field engineer by design and fabrication of TTL based interface boards required for Data Products printers to be used with Burroughs computers.

CMOS Library('84-85): As a TCS consultant working at Hewlett Packard, Cupertino, developed CMOS1.6 micron Standard Cells and I/O library.

ASIC Design('85-'86): As a TCS consultant working at H.P. Santa Clara, designed a hard disk controller interface chip, interfacing SCSI bus and hard disk drive electronics. Another assignment in ASIC design required design migration of DMA board to Standard Cell based CMOS IC for HP's bobcat line of workstation.

EDA Software('87): As a TCS consultant worked at Texas Instruments, Dallas, for the development of EDIF Reader/Writer software

Skills

CAD Tools Experience:
HSIM, HSPICE – used extensively
Proficient in writing Hardware descriptions in Verilog and VHDL for simulation and synthesis.
Expert user of Laker (Industry standard IC layout tool) for 65nm, 45nm designs, Cadence Virtuoso Layout Editor
Synopsis DC, Primetime used extensively (synthesis, timing closure)

Signal Processing WorkSystem (SPW), Matlab for DSP based system design and algorithm development.

Programming/OS: C,C++, MFC, Visual C++ (Windows programming). Scripting in Perl Tcl/Tk, shell

Graphics: Expertise in mechanical, architectural drawing with AutoCAD. Visio for general purpose drawing

Packages: MS Project, Excel, Word (office tools). Mathematica with programming.

Publications

[1] D.V.Das, S.C.Seth, P.T.Wagner, J.C.Anderson, and V.D.Agrwal. AN experimental Study on Reject Ratio Prediction for VLSI circuits. Proceedings of IEEE International Test Conference 1990, Washington, DC, Sept. 10-14, 1990, pp. 712-720

[2] D.V.Das, S.C.Seth and V.D.Agrawal. Estimating the Quality of Manufactured Digital Sequential Circuits. Proceedings of IEEE International Test Conference 1991, Nashville, TN, Oct 26-30, 1991, pp. 210-217

[3] D.V.Das, S.C.Seth and V.D.Agrawal. An Accurate Method for estimation of required fault coverage. 14th Annual IEEE Workshop on Design for Testability, Vail Colorado, April 16-19, 1991

[4] D.V.Das. S.C.Seth and V.D.Agrawal. Accurate computation of Chip Reject Ratio based on Fault Latency, IEEE Transaction on VLSI Systems, 1992, pp, 537-545.

[5] D.V.Das, Signal Integrity analysis for ICs and MCMs, Conference Proceedings, The Electronic Design Automation and Test Conference and Exhibition, Oct 26-Nov 5, 1994, Taiwan, Korea and China, pp. 76-86.

[6] D.V.Das, EM Simulation, The 8th International Conference on VLSI Design, 1995, New Delhi, India, Jan. 4-7, 1995, pp. 264-267.

[7] D.V.Das, Rajesh Kumar, M.Lauria, Modeling Application Specific Memories, IEEE International Workshop on Memory Technology, Design and Testing, Aug. 7-8, 1995 San Jose CA.

[8] D.V.Das, Application of Matrix Library in SPW, Cadence Technical Conference 2002.