M. TECH. ICT

(Specialization in VLSI Design)

Course Structure and Detailed Syllabus

SCHOOL OF INFORMATION AND COMMUNICATION TECHNOLOGY

GAUTAM BUDDHA UNIVERSITY

GREATER NOIDA – 210308

(INDIA)

SEMESTER I

Sr. No.	Subject Code	Courses	L-T-P	Credits
		THEORY		
1	EC535	Digital IC Design	3-1-0	4
2	CS523	Advanced Computer Architecture	3-1-0	4
3	EC531	Advanced Digital Communication System	3-1-0	4
4	CS527	Research Techniques in ICT	3-0-0	3
5	SS101	Human Values & Buddhist Ethics	2-0-0	2
		PRACTICALS		
6	EC585	Design IC Design Lab	0-0-3	2
7	EC581	Digital Communication Lab	0-0-3	2
8	GP531	General Proficiency	---	1
		Total	**17-3-6**	**22**
		Total Contact Hours	26	

SEMESTER II

Sr. No	Subject Code	Courses	L-T-P	Credits
		THEORY		
1	MA402	Modeling and Simulation	3-1-0	4
2	EC536	IC- Technology	3-0-0	3
3	EC538	Analog IC Design	3-0-0	3
4	EC578	CMOS VLSI Design	3-0-0	3
5		Elective-I	3-0-0	3
		PRACTICALS		
7	EC580	Design Lab I	0-0-3	2
8	EC592	Major Project	0-0-10	5
9	GP532	General Proficiency	---	1
		Total	**15-1-13**	**24**
		Total Contact Hours	29	

Elective-I

S. No	Subject Code	Courses
1	EC574	Integrated Circuit Physical Design
2	EC568	Design of Semiconductor Memories
3	EC576	CMOS RF Circuit Design

SEMESTER – III

Sr. No	Subject Code	Courses	L-T-P	Credits
		THEORY		
1	EC633	Low Power VLSI Design	3-0-0	3
2	EC675	Mixed Signal VLSI Design	3-0-0	3
3		Elective- II	3-0-0	3
4		Elective- III	3-0-0	3
		PRACTICALS		
5	EC683	Design Lab II	0-0-3	2
6	EC691	Dissertation Phase-I	0-0-14	7
7	GP631	General Proficiency	---	1
		Total	**12-0-17**	**22**
		Total Contact Hours		**29**

Elective-II & III

Sr.No	Subject Code	Courses
1	EC665	VLSI ASIC Design
2	EC667	RF MEMS Design and Technology
3	EC673	VLSI-Reliability Engineering
4	EC677	DSP Integrated Circuits
5	EC679	Test and Verification of VLSI Circuits
6	EC669	Algorithm for VLSI Design Automation

SEMESTER – IV

Sr. No	Subject Code	Courses	L-T-P	Credits
1	EC690	Dissertation Phase-II	---	21
2	GP632	General Proficiency	---	1
		Total	**---**	**22**

Grand Total Credits = 90

SEMESTER I

DIGITAL IC DESIGN			
Course Code:	**EC535**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45+15**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Digital number systems and information representation; arithmetic operations, decimal and alphanumeric codes, Binary logic, Boolean algebra (identities, functions and manipulation), standard forms, simplification, Logic gates, switch-level and logic CMOS implementation, integrated circuits.

UNIT II: Combinational Logic Design
Components of Combinational Design, Multiplexer and Decoder, Multiplexer Based Design of Combinational Circuits, Implementation of Full Adder using Multiplexer and Decoder, Types of PLD, Combinational Logic Examples, PROM - Fixed AND Array and Programmable OR Array Implementation of Functions using PROM, PLA, PAL, Comparison of PROM, PLA and PAL Implementation of a Function using PAL, Types of PAL Outputs, Device Examples

UNIT III: Sequential Logic Design
Introduction to Sequential Circuits, R-S Latch and Clocked R-S Latch, D Flip Flop, J-K Flip Flop, Master Slave Operation, Edge Triggered Operation, Clocking of Flip-flops, Setup and Hold Times, Moore Circuit, Mealy Circuit Clocking Rules, Sequential Circuits – Design Rules, Sequential Circuit Design Basics, Design of a 4-bit Full Adder using D Flip-flop, Pattern Identifier, State Graph , Transition Table, Implementation of Pattern Identifier, MUX Based Realization, ROM Realization, PAL Implementation

UNIT IV: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
PLD families, ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array, I/O Block, Programmable interconnect, Xilinx – 3000 series and 4000 series FPGAs, Altera CPLDs, Altera FLEX 10K series PLDs, Designing a synchronous sequential circuit using PLA/PAL, Realization of finite state machine using PLD

UNIT V: System Design using HDL
HDL operators , Arrays, concurrent and sequential statements , packages, Data flow, Behavioral – structural modeling, compilation and simulation of HDL code, Test bench, Realization of combinational and sequential circuits using HDL, Registers, counters, sequential machine, serial adder , Multiplier-Divider, System Design examples.

Text Books:
[1] Charles H.Roth Jr : Fundamentals of Logic Design, Thomson Learning, 2004
[2] J.Bhaskar: A Verilog Primer, BSP, 2003.
[3] J.Bhaskar: A Verilog HDL Synthesis BSP, 2003

References:
[1] Nripendra N Biswas : Logic Design Theory, Prentice Hall of India,2001
[2] Parag K.Lala: Digital system Design using PLD, B S Publications, 2003
[3] Charles H Roth Jr. : Digital System Design using VHDL, Thomson learning, 2004
[4] Douglas L.Perry : VHDL programming by Example, Tata McGraw Hill, 2006

ADVANCED COMPUTER ARCHITECTURE			
Course Code:	CS523	**Credits:**	**4**
No. of Lectures (Hrs/Week):	3+1	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	45+15	**End Sem Exam Hours:**	**3**

UNIT I
Introduction to parallel processing: parallelism in uniprocessor system, basic uniprocessor architecture, parallel processing mechanism, balancing of sub system bandwidth, multiprogramming and time sharing, parallel computer structures, pipeline computers, array computers, multiprocessor systems, dataflow computer concept, architectural classification scheme: multiplicity of instruction-data streams, serial versus parallel processing, parallelism versus pipelining, parallel processing applications, productive modeling simulation, engineering design and automation.

UNIT II
Principles of pipelining and vector processing: pipelining- an overlapped parallelism, principles of linear pipelining, clock period, efficiency, throughput, classification of pipeline processors, general pipeline and reservation tables.

UNIT III
Principles of designing pipeline processors: effect of branching, data buffering and bussing structures, internal forwarding and register tagging, hazard detection and resolution, job sequencing and collision prevention, reservation and latency analysis, collision free scheduling, state diagram, greedy cycle, pipeline schedule optimization, pipeline throughput, pipeline efficiency.

UNIT IV
Structure and algorithm for array processors: SIMD array processor, SIMD computer organization, inter – PE communication, SIMD interconnection network, static versus dynamic networks, cube interconnection network, shuffle-exchange omega networks, parallel algorithms and SIMD matrix multiplication.

UNIT V
Multiprocessor architecture and scheduling: functional structure, loosely coupled and tightly coupled multiprocessor, deterministic scheduling strategy, deterministic scheduling model, control flow versus data flow computer, data flow graphs and languages.

References Books:
[1]Kai Hwang, "Advanced Computer Architecture", Tata McGrawHill Edition
[2]Kai Hwang and Faye A. Briggs, "Computer Architecture and Parallel Processing", McGraw-Hill International Edition
[3] Richard Y. Kain, "Advanced Computer Architecture: a Systems Design", Prentice Hall.
[4] James M. Feldman, Charles T. Retter, "Computer architecture: a designer's Text Based on a generic RISC", McGraw-Hill
[5]Jurij Silc, Borut Robic, Theo Ungerer, "Processor Architecture: From Dataflow to Superscalar and Beyond", Springer.
[6] Hennessy and Patterson, "Computer Architecture: A Quantitative Approach", Elsevier.
[7] Dezso and Sima, "Advanced Computer Architecture", Pearson.
[8] Quinn, "Parallel Computing: Theory & Practice", TMH.
[9] Quinn, "Parallel Programming in C with MPI and Open MP", TMH.

ADVANCED DIGITAL COMMUNICATION SYSTEM			
Course Code:	EC531	**Credits:**	4
No. of Lectures (Hrs/Week):	3+1	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45+15	**End Sem Exam Hours:**	3

UNIT I
Pulse Modulation Analog Signals:- Sampling of Signal, Sampling Theorem for Low Pass and Band Pass Signals, Aliasing, Pulse Amplitude Modulation (PAM), Time Division Multiplexing, Channel Bandwidth for PAM-TDM Signal, Types of Sampling, Instantaneous, Natural and Flat Top (Mathematical and Spectral Analysis), Aperture Effect, Introduction to Pulse Position and Pulse Duration Modulation.

UNIT II
Pulse Code Modulation Digital Signal:- Quantization, Quantization Error, Pulse Code Modulation (PCM), Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding NRZ, RZ, Biphase, Duo Binary Etc ,Differential PCM (DPCM), Delta Modulation (DM), and Adaptive Delta Modulation (ADM), Slope Overload Error ,Granular Noise ,Comparison of various system in terms of Bandwidth and SNR.

UNIT III
Digital Modulation Techniques :- Analysis, Generation and Detection (Block Diagram),
Spectrum and Bandwidth of Amplitude Shift Keying (ASK), Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Offset and Non-offset Quadrature Phase Shift Keying (QPSK), M-ary PSK, Binary Frequency Shift Keying (BFSK), M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation (QAM), Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

UNIT IV
Concept of Probability, Relative Frequency and Probability Conditional Probability and
Independent Events, Random Variables, Discrete Random Variables, Cumulative Distribution Function(CDF), Probability Density Function(PDF),Statistical Averages (Means),Chebyshev"s Inequality,Central Limit Theorem.

UNIT V
Spread Spectrum Modulation: Pseudo random noise sequences, notion of spread spectrum, direct sequence, frequency hopping, processing gain. Convolution codes and Golay codes.

Text Books:
[1] B. Sklar, Digital Communication, Pearson Education.
[2] Tomasi: Advanced Electronics Communication Systems, 6th Edition, PHI

References:
[1] Taub & Schilling, Principles of Communication system, TMH.
[2] Lathi B.P., Modern Analog and Digital Communication systems, Oxford Uni. Press.
[3] Haykin Simon, Digital Communication, Wiley Publication.
[4] Proakis, Digital communication, McGraw Hill
[5] Schaum"s Outline series, Analog and Digital Communication.
[6] Singh and Sapre: Communication System, TMH
[7] Couch: Digital and Analog Communication, Pearson Education
[8] David Smith: Digital Transmission Systems, Springer- Macmillan India Ltd.

RESEARCH TECHNIQUES IN ICT			
Course Code:	CS527	Credits:	3
No. of Lectures (Hrs/Week):	3	Mid Sem Exam Hours:	2
Total No. of Lectures:	45	End Sem Exam Hours:	3

Unit I : Introduction to Research Techniques
Meaning of research, objectives of research, motivation in research, types of research-Introduction to experimental test bed, algorithmic research, simulation research, mathematical modeling approach, characteristics and prerequisites of research, significance of research, research process, Sources of research problem, criteria of identifying the problem, necessity of defining the problem, errors in selecting research problem, technique involved in defining the problem, Report and paper writing

Unit II: Data Analysis and Statistical Techniques
Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminant analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis.

Unit III: Random Numbers and Variates
Properties of random numbers, generation, tests for random numbers, random-variate generation
Inverse Transform technique, direct transformation, convolution method, acceptance-rejection Technique, Probability distributions functions, Moments, moment generating functions, joint distributions, marginal and conditional distributions, functions of two dimensional random variables Poisson process-Markovian queues, single and multi server models, Little's formula, steady state analysis

Unit IV: Algorithmic Research
Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments,

Unit V: Simulation and Soft Computing Techniques
Introduction to soft computing, Artificial neural network, Genetic algorithm, Fuzzy logic and their applications, Tools of soft computing, Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, verification of simulation models, calibration and validation of models, Output analysis, introduction to MATLAB, NS2, ANSYS, Cadence

Text Books:
[1] R. Panneerselvam: Research Methodologies, PHI
[2] Jerry Banks, John S. Carson, Barry.L. Nelson David. M. Nicol: Discrete-Event System
    Simulation, Prentice-Hall India
[3] Donald Gross, Carl M. Harris: Fundamentals of Queueing Theory, 2nd Ed. John Wiley and
    Sons, New York,
References:
[1] Best John V. and James V Kahn: Research in Education, Wiley eastern, 2005.
[2] Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra: Elements of Educational Research, PHI, 2003.
[3] K. Setia: Methodology of Research Education, IEEE publication, 2004.
[4] Kothari, C.R.: Research methodology, Methods and Techniques, 2000.

DIGITAL IC DESIGN LAB			
Course Code:	**EC585**	**Credits:**	**2**
No. of Labs (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions	**15**		

List of Experiments

1. Introduction to Simulation Software Modelsim.
2. Realization of Gates using VHDL (AND, OR, NOT)
3. Realization of Universal Gates using VHDL (NAND,NOR, EX-OR, EX-NOR).
4. Realization of 2 to 4 Decoder using VHDL.
5. Realization of 3 to 8 Encoder using VHDL.
6. Realization of Combinational Design of Multiplexer using VHDL.
7. Realization of Combinational Design of Demultiplexer and Comparator using VHDL.
8. Realization of Functions of Half and Full Adder with different Modeling style using VHDL.
9. Realization of 32 bit ALU using VHDL.
10. Realization of Flip-flops using VHDL (SR,D, JK,T).
11. Realization of a 4-bit binary, BCD counters and any sequence counter with Synchronous Reset.
12. Realization of a 4-bit binary, BCD counters and any sequence counter with Asynchronous Reset.
13. Realization of VHDL code for 7- Segments Display.
14. Realization of VHDL codes to display messages on given LCD panel.
15. Realization of VHDL code to operate a given stepper motor.

DIGITAL COMMUNICATION LAB			
Course Code:	**EC581**	**Credits:**	**2**
No. of Labs (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions	**15**		

List of Experiments

1. To verify the sampling theorem.

2. To study ASK (Amplitude Shift Keying) System.
   - Modulate a digital signal using amplitude shift keying.
   - Demodulate a amplitude shift keyed signal.

3. To study FSK (Frequency Shift Keying) System.
   - Modulate a digital signal using frequency shift keying.
   - Demodulate a frequency shift keyed signal.

4. To study BFSK (Binary Frequency Shift Keying) System.
   - Modulate a digital signal using Binary Frequency shift keying.
   - Demodulate a Binary Frequency Shift keyed signal.

5. To study PSK (Phase Shift Keying) System.
   - Modulate a digital signal using phase shift keying.
   - Demodulate a phase shift keyed signal.

6. To study BPSK (Binary Phase Shift Keying) System.
   - Modulate a digital signal using binary phase shift keying.
   - Demodulate a binary phase shift keyed signal.

7. To study QPSK (Quadrature Phase Shift Keying) System.
   - Modulate a digital signal using Quadrature phase shift keying.
   - Demodulate a Quadrature phase shift keyed signal.

8. To study DPSK (Differential Phase Shift Keying) System.
   - Modulate a digital signal using differential phase shift keying.
   - Demodulate a differential phase shift keyed signal.

9. To study Pulse Code Modulation System (PCM) System.
   - Generate, modulate and transmit a pulse coded signal.
   - Receive and demodulate a pulse coded signal.

10. To study TDM (Time Division Multiplexing) System.
    - Generate and transmit a TDM signal.
    - Receive and de-multiplex a TDM signal.

11. To study M-ARY FSK modulation and demodulation.
12. To study and implement the cyclic redundancy check.
13. To study the circuit of PAM modulator and demodulator.
14. To study the circuit of PWM modulator and demodulator.
15. To study the circuit of PPM modulator and demodulator.

IC- TECHNOLOGY			
Course Code:	EC536	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

SEMESTER II

UNIT I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II: Lithography and Relative Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III: Deposition, Diffusion, Ion Implantation and Metallization
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV: Process Simulation and VLSI Process Integration
Ion implantation, Diffusion and oxidation, Epitaxy, Lithography, Etching and Deposition, NMOS IC Technology, CMOS IC Technology, Memory IC technology, Bipolar IC Technology, IC Fabrication.

UNIT V: Assembly Techniques and packaging of VLSI Devices
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

Text Books:
[1] S.M.Sze: VLSI Technology, Mc.Graw.Hill Second Edition. 2002.
[2] Douglas A. Pucknell and Kamran Eshraghian: Basic VLSI Design, Prentice Hall India, 2003.

References:
[1] Amar Mukherjee: Introduction to NMOS and CMOS VLSI System design, Prentice Hall, 2000.
[2] Wayne Wolf : Modern VLSI Design, Prentice Hall India,1998.

ANALOG IC DESIGN			
Course Code:	EC538	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

UNIT I: Basics in Analog ICs

Analog IC system, Op-Amps, phasors and impedance, Power supply, Transfer functions, filters, bode plots, Integrated circuits, Power speed and efficiency, MOS: as a switch, I/V characteristic, second order effects, device models, amplification, Amplifier: biasing, distortion, two port model, transfer function, frequency response, Noise in circuits, noise in amplifiers, noise bandwidth, small signal modeling for FETs: CS & CE amplifier.

UNIT II: Single Stage and Multistage IC Amplifier

Single transistor amplifier: Amplifier classification: CE & CS, CC & CD, CB & CG, BJT & FET amplifier, Ideal and Non Ideal operational amplifier, influence of body effect on amplifier performance, **Multistage amplifier:** AC coupled, direct coupled, differential amplifier, two stage operational amplifier, BiCMOS amplifier, Class A, Class B, Class AB amplifier,

UNIT III: Current Mirrors and Frequency response

Current Mirrors: MOS transistor, BJT, Buffered, Widlar, Wilson, Cascode, as reference current generation, as bandgap reference, as active load in amplifier. Gilbert Analog amplifier,

Frequency response: LF and HF response, transistor model at high frequency, limitation of CE and CS amplifier at low frequency, miller multiplication, open circuit time constant method, frequency response of multistage amplifier, tuned amplifier, mixers.

UNIT IV: Feedback, Stability and Oscillators

Classical feedback system, general considerations, topologies, voltage amplifier, trans-resistance amplifier, current amplifiers, transconductance amplifiers, loop gain estimation, stability of feedback amplifier, Oscillators: Barkhausen criteria, frequency selective RC oscillators, LC & Crystal oscillators.

UNIT V: Analog ICs Special Circuits

Sample and Hold Circuits, Switch Capacitor circuits, Switched capacitor integrators, switched capacitor filter circuits, Data Converter Fundamentals & Architecture: Ideal D/A & A/D converter, Serial and Flash D/A converters and A/D converters, Medium and High Speed converters, Over-sampling converters, CMOS VCO, Ring oscillators, PLL, Gm-C Circuits, rectifiers, comparator.

Text Books:

[1] Behzad Razavi, Design of Analog CMOS Integrated Circuits, Mcgraw Hill, 2002.
[2] Richard C. Jaeger and T. N. Blalock, Microelectronic Circuit Design, 4th Edition, McGraw-Hill, 2010.
[3] Carusone, Johns and Martin, Analog Integrated Circuit Design, 2nd Edition, John Wiley, 2012

References:

[1] Yannis Tsividis and Colin McAdrew, Operation and Modeling of the MOS Transistor, 3rd Edition, Oxford University Press, 2011.
[2] Gray, Hurst, Lewis & Meyer, Analysis & Design of Analog Integrated Circuits, 4th Edition, John Wiley, 2012.

CMOS VLSI DESIGN			
Course Code:	**EC538**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

[3] Allen and Holberg, CMOS Analog Circuit Design, 2nd Edition, Oxford University Press, 2002.

[4] Agarwal and Lang, Foundations of Analog Digital Electronic Circuits, Morgan Kaufmann, 2005.

UNIT I: MOS Transistor theory
NMOS / PMOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT II: CMOS Design Rules
Lambda Based Design rules, scaling factor, p well / n well / twin well CMOS process, Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, MOS circuits scaling.

UNIT III: Basics of Digital CMOS Design
Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques.

UNIT V: Dynamic CMOS and clocking
Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking-clock generation, clock distribution, clocked storage elements.

UNIT IV: VLSI System Components Circuits and System Level Physical Design
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers, Physical design Delay modeling, cross talk, floor planning, power distribution, Clock distribution.

Text Books:
[1] Neil H.E. Weste and Kamran Eshraghian: Principles of CMOS VLSI Design, Pearson Education
    ASIA, 2nd edition, 2000.
[2] John P.Uyemura: Introduction to VLSI Circuits and Systems, John Wiley & Sons, 2002.

References:
[1] Eugene D.Fabricius: Introduction to VLSI Design McGraw Hill International Editions, 1990
[2] Pucknell: Basic VLSI Design, Prentice Hall of India Publication, 1995.
[3] Wayne Wolf: Modern VLSI Design System on chip, Pearson Education, 2002

DESIGN LAB I			
Course Code:	**EC580**	**Credits:**	**2**
No. of Labs (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions	**15**		

1. Introduction to Linux OS

2. Introduction to Virtuoso tool and Full Custom IC Design cycle.

3. Realization of an Inverter – I

4. Realization of an Inverter – II

5. Realization of an Inverter – III

6. Realization of an Inverter – IV

7. Realization of Differential Amplifier.

8. Realization of Common Source Amplifier.

9. Realization of Common Drain Amplifier.

10. Realization of Operational Amplifier – I.

11. Realization of Operational Amplifier – II.

12. Realization of Basic DAC Circuit.

13. Realization of R-2R DAC.

14. Realization of Basic ADC Circuit.

15. Realization of SAR based ADC.

INTEGRATED CIRCUIT PHYSICAL DESIGN			
Course Code:	**EC574**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

ELECTIVE I

Unit I: The Well
Substrate, Parasitic Diode, N-well as a Resistor, N-well patterning and layout, Design Rules, Resistance calculation, N-well Resistor, N-well/Substrate Diode, Carrier Concentrations, Fermi Energy Level, Depletion Layer Capacitance, Storage or Diffusion Capacitance, RC Delay through the N-well, Distributed RC Delay, Distributed RC Rise Time, Twin Well Processes.

Unit II: The Metal Layers
Bonding Pad and layout, Metal-to-Substrate capacitance, Passivation, Design and Layout of Metal Layers, Metal1 and Via1, Parasitic Associated with Metal Layers, Intrinsic Propagation Delay, Current-Carrying Limitations, Design Rules for Metal Layers, Contact Resistance, Crosstalk and Ground Bounce , Crosstalk, Ground Bounce, DC Problems, AC Problems.

Unit III: The Active and Poly Layers
Layout Using Active and Poly Layers, P- and N-Select Layers, Poly Layer, Self-Aligned Gate, Poly Wire, Silicide Block, Connecting Wires to Poly and Active, Connecting P-Substrate to Ground, N-Well Resistor layout, NMOS and PMOS Device layout, Standard Cell Frame, Design Rules, Electrostatic Discharge (ESD) Protection, Diodes layout.

Unit IV: Resistors, Capacitors, MOSFETs
Resistors, Temperature Coefficient, Voltage Coefficient, Unit Elements, Guard Rings, Interdigitated Layout, Common- Centroid Layout, Dummy Elements, Poly-Poly Capacitor layout, Parasitic, MOSFETs: Lateral Diffusion, Oxide Encroachment, Source/Drain Depletion Capacitance, Source/Drain Parasitic Resistance, Long-Length MOSFETs layout, Large-Width MOSFETs layout, MOSFET Capacitances.

Unit V: MOSFET Operation
Accumulation, Depletion, Strong Inversion, Threshold Voltage, Characteristics of MOSFETs, MOSFET Operation: Triode and Saturation, Cgs Calculation, Long-Channel MOSFET Models, Model Parameters Related to the Drain Current, Modeling of the Source and Drain Implants Short-Channel MOSFETs Hot Carriers, Lightly Doped Drain, MOSFET Scaling, Short-Channel Effects, Oxide Breakdown, Drain-Induced Barrier Lowering, Gate-Induced Drain Leakage.

Text Books:
[1] R. Jacob Baker: CMOS Circuit Design, Layout, and Simulation, Second Edition.
[2] Christopher Saint, Judy Saint: IC Layout Basics: A Practical Guide

References:
[1] Dan Clein: CMOS IC Layout : Concepts, Methodologies, and Tools,.
[2] Alan Hastings, Roy Alan Hastings: The Art of Analog Layout

DESIGN OF SEMICONDUCTOR MEMORIES			
Course Code:	EC568	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

UNIT I: RAM Technologies
Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs, DRAMs Cell Theory

UNIT II: Non Volatile Memories
Masked Read-Only Memories, High Density ROMs, PROMs, CMOS PROMs, EEPROMs, Floating-Gate EPROM Cell, Electrically Erasable PROMs, EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories, Advanced Flash Memory Architecture.

UNIT III: Memory Testing
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, ASIC Memory Testing.

UNIT IV: Reliability and Radiation Effects
General Reliability Issues, RAM Failure Modes and Mechanics, Nonvolatile Memory Reliability, Reliability Modeling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, RAM Fault Modeling, Electrical Testing, Psuedo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling.

UNIT V: Packaging Technologies
Radiation Effects, Single Event Phenomenon, Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimeter, Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories, GaAs FRAMs, Analog Memories, Magnetoresistive RAM.

Text Books:
[1] Ashok K. Sharma: Semiconductor Memories Technology, Testing and Reliability, Prentice-
    Hall of India Private Limited, New Delhi, 1997.
[2] Tegze P. Haraszti: CMOS Memory Circuits, Kluwer Academic publishers, 2001.

CMOS RF CIRCUIT DESIGN			
Course Code:	EC576	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

UNIT I: Introduction to RF design and Wireless Technology
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

UNIT II: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

UNIT III: RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT V: RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks, Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Mixers- working and implementation. Oscillators- Basic topologies, VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text Book:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University press 1998.

References:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce CMOS Circuit Design, layout and Simulation PHI, 1998
[3] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996

LOW POWER VLSI DESIGN			
Course Code:	EC633	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

SEMESTER- III

UNIT I: Introduction
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

UNIT II: Device & Technology Impact on Low Power
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III: Low Power Design
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT IV: Low power Architecture & Systems
Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT V: Power Optimization Techniques
Design time power optimization, circuit level power optimization, various architectural level methods for optimization, estimation and optimization of interconnects parasitic and delays, Low power clocking and system optimization, Standby low power optimization, Run Time voltage optimization and estimation.

Text Books:
[1] Gary K. Yeap: Practical Low Power Digital VLSI Design, KAP, 2002
[2] Rabaey and Pedram: Low power design methodologies, Kluwer Academic, 1997
[3] Jan Rabaey, Low Power Design Essentials, Springer, 2009

References :
[1] Kaushik Roy, Sharat Prasad: Low-Power CMOS VLSI Circuit Design, Wiley, 2000
[2] J. B. Kulo and J.H Lou: Low Voltage CMOS VLSI Circuits, Wiley 1999.
[3] A.P. Chandrasekaran and R.W. Broadersen: Low power digital CMOS design, Kluwer, 1995.
[4] Abdelatif Belaouar, Mohamed.I. Elmasry, "Low power digital VLSI design, Kluwer, 1995

MIXED SIGNAL VLSI DESIGN			
Course Code:	**EC675**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit 1: Signals, Filters, and Tools
Sinusoidal Signals, Pendulum Analogy, Amplitude in the x-y Plane, In-Phase and Quadrature Signals, Complex (z-) Plane, Comb Filters, Digital Comb Filter, Digital Differentiator, Intuitive Discussion of the z-Plane, Comb Filters with Multiple Delay Elements, Digital Integrator, Delaying Integrator, Exponential Fourier Series, Fourier Transform, Dirac Delta Function .

Unit 2: Sampling and Aliasing
Sampling, Impulse Sampling, Time Domain Description of Reconstruction, Decimation, Sample-and-Hold, S/H Spectral Response, Reconstruction Filter, Circuit Concerns for Implementing the S/H, Track-and-Hold (T/H), Interpolation, Zero Padding, Hold Register, Linear Interpolation, K-Path Sampling, Switched-Capacitor Circuits, Non-Overlapping Clock Generation, Circuits Implementing the S/H, Finite Op-Amp Gain-Bandwidth, Auto zeroing,

Unit 3: Analog Filters
Integrator Building Blocks, Lowpass Filters, Active-RC Integrators, Effects of Finite Op-Amp Gain Bandwidth Product, Active-RC SNR, MOSFET-C Integrators, gm-C Integrators, Common-Mode Feedback Considerations, High-Frequency Transconductor, Discrete-Time Integrators, Frequency Response of an Ideal Discrete-Time Filter, Filtering Topologies, Bilinear Transfer Function, Active-RC Implementation, Transconductor-C Implementation.

Unit 4 Digital Filters
Models for DACs and ADCs, Ideal DAC, Modeling of Ideal DAC, Ideal ADC, Number Representation, Increasing Word Size, Adding Numbers and Overflow, Two's Complement Sinc-Shaped Digital Filters, Counter, Aliasing, Accumulate-and-Dump, Lowpass Sinc Filters, Averaging without Decimation, Cascading Sinc Filters, Finite and Infinite Impulse Response Filters, Bandpass and Highpass Sinc Filters, Frequency Sampling Filters.

Unit 5: Data Converter SNR
Quantization Noise, Quantization Noise Spectrum, Bennett's Criteria, RMS Quantization Noise Voltage, Quantization Noise as a Random Variable, Quantization Noise Voltage Spectral Density, Power Spectral Density, SNR, Effective Number of Bits, Coherent Sampling, SNDR, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter.

Text Books:
[1] Jacob Baker, CMOS Mixed Signal Circuit Design.
[2] Tony Chan, David Johns and Ken Martin Analog Integrated Circuit Design, 2nd edition, 2009.

References:
[1] Yannis Tsividis: Mixed Analog-Digital VLSI Device and Technology.
[2] Roubik Gregorian: Introduction to CMOS OpAmps and Comparators,.
[3] Razavi: Piley, Principle of Data Conversion System Design, Wiley, 1994.
[4] Allen Holberg: CMOS Circuit Design, Oxford, 2010.
[5] Baker, Li, Boyce: CMOS Circuit Design, Layout, Simulation, Wiley, 1997.
[6] Gregorian, Themes: Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
[7] Oppenheim: Time Discrete Signal Processing, Oldenbourg.
[8] Norsworthy, Schreier, Themes: Delta Sigma Data Converter, IEEE Press, 1997.
[9] Schreir, Themes: Understanding Delta Sigma Data Converter, IEEE Press, 2005.

DESIGN LAB II			
Course Code:	**EC683**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**03**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**15**		

List of Experiments

1. Introduction to simulation software ANSYS using GUI.
2. Introduction to simulation software ANSYS using Command lines.
3. Simulation and Realization of Capacitive Acceleration Sensor using ANSYS.
4. Modal and harmonic analysis of Silicon Beam Actuator using ANSYS
5. Multiplysics Analysis of a Thermal Actuator using ANSYS.
6. Simulation and Realization of Axisymmetric model of a piezoresistive pressure sensor.
7. Electromechanical Simulation and Modeling of RF MEMS Capacitance using ANSYS.
8. Introduction to VHDL AMS/ Verilog A and Cadence Mixed Signal Simulation Environment.
9. Reduced Order Modeling of RF MEM Capacitance.
10. Realization of Mixed Signal Design of R-2R DAC using Cadence.
11. Realization of Mixed Signal Design of SAR based ADC using Cadence.
12. Realization of Mixed Signal Design of 32b Ripple-Carry Adder.
13. Realization of Mixed Signal Design of Pipelined 32b Adder using Cadence.

VLSI ASIC DESIGN			
Course Code:	EC665	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

ELECTIVE III AND IV

UNIT I : Introduction to ASICs, CMOS Logic and ASIC Library Design
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II: Programmable ASICs, Programmable ASIC Logic Cells and ASICs I/O Cells.
Anti fuse, static RAM, EPROM and EEPROM technology, PREP benchmarks, Actel ACT,Xilinx LCA, Altera FLEX , Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III: Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV: Logic Synthesis, simulation and Testing
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation- boundary scan test - fault simulation - automatic test pattern generation.

UNIT V: ASIC Construction, Floor Planning, Placement and Routing
System partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC.

Text Books:
[1] M.J.S .Smith, Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
[2] Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach,
   Prentice Hall PTR, 2003.

References:
[1] Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
[2] R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House, 2000.

RF MEMS DESIGN AND TECHNOLOGY			
Course Code:	**EC667**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to MEMS Technology
Introduction and Origin of MEMS, driving force for MEMS development, Application of MEMS, MEMS fabrication technologies: Conventional IC Vs MEMS fabrication processes, Micromachining Technology and Process, LIGA process, Wafer Bonding, MEMS Packaging

UNIT II: Mechanics for MEMS Design
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III: MEMS Sensor and Actuation Principles
Sensors, Classification and terminology of Sensors, evolution of Semiconductor sensors, sensor characterization basic concept of acoustic, mechanical, magnetic, thermal sensors and integrated sensors. Actuation of MEMS devices, electrostatic actuation, and parallel plate capacitor- cantilever beam based movement, comb-drive structures.

UNIT IV: Modeling and Realization of RF MEMS components
Typical features of RF and wireless system. The functionality, modeling and implementation issues of central RF MEMS components: Capacitors/ Inductors, Varactor, Switches, RF Power Attenuator, Power Amplifier, Impedance Matching Network, transmission lines, phase shifters, resonators, filters and oscillators, Antenna, different modeling styles in RF MEMS devices.

UNIT V: Packaging, Reliability and Integration of RF MEMS
Overview of packaging, possibilities for monolithic integration of RF MEMS with microelectronics, Reliability issues in RF MEMS, Case studies on more composite RF MEMS systems.

Text Books:
[1] Stephen Santuria: Microsystems Design, Kluwer publishers, 2000.
[2] N. Maluf: An introduction to Micro Electromechanical System Design, Artech House, 2000.
[3] V. Varadan, K. J. Vinoy, K. A. Jose, RF MEMS and their Applications, Wiley, 2003.

References:
[1] Mohamed Gad-el-Hak: The MEMS Handbook, CRC press Baco Raton,2000.
[2] Tai Ran Hsu: MEMS & Micro systems Design and Manufacture, TMH, Delhi, 2002.
[3] V. Varadan, K. J. Vinoy, S. Gopalakrishnan Design and Development Methodologies, Smart Material Systems and MEMS, Wiley.
[4] A.L. Hartzell, M.G.da Silva, H.R.Shea, MEMS Reliability, Springer, 2011.
[5] R.R. Tummala, Fundamentals of Microsystems Packaging, Mcgraw Hill.
[6] H.J. De L. Santos, RF MEMS Circuit Design for Wireless Communications, Artech House.

VLSI-RELIABILTY ENGINEERING			
Course Code:	EC673	**Credits:**	3
No. of Lectures (Hrs/Week):	3	**Mid Sem Exam Hours:**	2
Total No. of Lectures:	45	**End Sem Exam Hours:**	3

UNIT I: Probability Plotting and Load- Strength Interference

Statistical distribution , statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II: Reliability Prediction, Modeling and Design

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III: Electronics and Software System Reliability

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV: Reliability Testing and Analysis

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V Manufacture and Reliability Management

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

Text Books:
[1] Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability
    Engineering, Fourth edition, John Wiley & Sons, 2002
[2] David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New
    York, AT & T Reliability Manual, 5th Edition, 1998.

Reference:
[1] Gregg K. Hobbs, Accelerated Reliability Engineering - HALT and HASS, John Wiley &
    Sons, New York, 2000.

DSP INTEGRATED CIRCUITS			
Course Code:	**EC677**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: DSP Integrated Circuits and VLSI Circuit Technologies
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic.

UNIT II: Digital Signal Processing
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III: Digital Filters and Finite Word length Effects
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP Architectures and Synthesis of DSP Architectures
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. DSP algorithms hardware mapping, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V Arithmetic Units and Integrated Circuit Design
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

Text Books:
[1] Lars Wanhammer, DSP Integrated Circuits, 1999 Academic press, New York
[2] A.V.Oppenheim et.al, Discrete-time Signal Processing, Pearson Education, 2000.

References:
[1] Emmanuel C. Ifeachor, Barrie W. Jervis, Digital signal processing – A practical approach, Second Edition, Pearson Education, Asia.
[2] Keshab K.Parhi, VLSI Digital Signal Processing Systems design and Implementation, John Wiley & Sons, 1999.

TEST AND VERIFICATION OF VLSI CIRCUITS			
Course Code:	**EC679**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Basic Concepts, Functional Modeling: Truth table and primitive cubes, Binary decision diagrams, Basic RTL constructs, Timing Modelling, Structural Modeling: External Representations Structural Properties, Internal representations, Wired Logic and bidirectionality.

UNIT II: Logic Simulation
Types of simulations, The unknown logic values, Complied simulation, Event driven simulation Delay Models for gates, Element Evaluation, Hazard Detection, Tristate Logic, MOS Logic, other delay models: Rise and Fall Delays, Inertial Delays, Ambiguous Delays, Oscillation Control.

UNIT III: Fault Modeling and Simulation
Logical Fault Models, Fault Detection and Redundancy: Combinational Circuits, Sequential Circuits, Fault Equivalence and Fault location: Combinational Circuits, Sequential Circuits, Fault Dominance, Single stuck Fault model, Multiple stuck at Fault model, General Fault Simulation Techniques: Serial Fault, Parallel Fault, Deductive Fault, Concurrent Fault, Fault Simulation for Combinational Circuits.

UNIT IV: Testing for Faults
Basic Issues, ATG for SSFs in Combinational Circuits: Fault Oriented ATG, Common Concepts, Algorithms, Selection Criteria, Fault Independent ATG, Random Test Generation, Combined Deterministic/Random Test Generation, ATG for single stuck at faults in sequential Circuits, Bridging Fault model, Detection of feedback and non feedback Bridging Faults.

UNIT V: Design for Testability
Testability: Tradeoffs, Controllability and Observability, Ad Hoc Design for Testability Techniques: Test points, Initialization, Monostable multivibarators, Oscillators and Clocks, Controllability and Observability by means of scan registers, Generic scan based designs.

Text Books:
[1] Digital Systems Testing & Testable Design, Miron Abramovici, Melvin A. Breuer, Arthur D.
    Friedman.
[2] An Introduction to Logic Circuit Testing, Parag K Lala

References:
[1] VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon), Laung-
    Terng Wang, Cheng-Wen Wu, Xiaoqing Wen.

ALGORITHM FOR VLSI DESIGN AUTOMATION			
Course Code:	**EC669**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction

Architectural Design , Logic Design, Physical Design , Full-custom Layout**,** Gate-array Layout, Standard-cell Layout Macro-cell Layout, Programmable Logic Arrays, FPGA layout**,** Difficulties in Physical Design, Problem Subdivision, Computational Complexity of Layout Subproblems, Solution Quality, Nets and Netlists, Connectivity Information, Weighted Nets, Grids, Trees, and Distances.

UNIT II: Circuit Partitioning and Floorplanning

Cost Function and Constraints: Bounded Size Partitions, Minimize External Wiring, Approaches to Partitioning Problem: Kernighan-Lin Algorithm, Variations of Kernighan-Lin Algorithm, Fiduccia Mattheyses Heuristic, Simulated Annealing, Floorplanning Model, Approaches to Floorplanning, Cluster Growth ,Simulated Annealing ,Analytical Technique , Dual Graph Technique.

UNIT III: Placement

Complexity of Placement , Problem Definition , Cost Functions and Constraints: Estimation of Wirelength, Minimize Total Wirelength , Minimize Maximum Cut , Minimize Maximum Density, Maximize Performance, Other Constraints, Approaches to Placement: Partition-Based Methods, Limitation of the Min-cut Heuristic, Simulated Annealing , Numerical Techniques.

UNIT IV: Routing

Problem Definition, Cost Functions and Constraints: Placement Constraints , Number of Routing Layers Geometrical Constraints, Maze Routing Algorithms: Lee Algorithm, Limitations of Lee Algorithm for Large Circuits ,Connecting Multi-point Nets ,Finding More Desirable Paths, Further Speed Improvements, Line Search Algorithms, Other Issues: Multi Layer Routing , Ordering of Nets , Rip-up and Rerouting, Power and Ground Routing.

UNIT V: Advanced Topics

Cost Functions and Constraints , Routing Regions:Routing Regions Definition, Routing Regions Representation, Sequential global Routing: The Steiner Bee Problem, Global Routing by Maze Running, Integer Programming ,Global Routing by Simulated Annealing : The First Stage , The Second stage, Hierarchical Global Routing.

Text Books:

[1] VLSI physical design automation: theory and practice, By Sadiq M. Sait, Habib Youssef.
[2] Algorithm for VLSI physical design automation by Naveed A. Sherwani.

References:

[1] Essential Electronic Design Automation (EDA), Mark D Birnbaum.
[2] Physical Design Automation for VLSI systems, Bryan D Ackland.
[3] Practical Problems in VLSI Physical Design Automation, Sung Ku Lim.