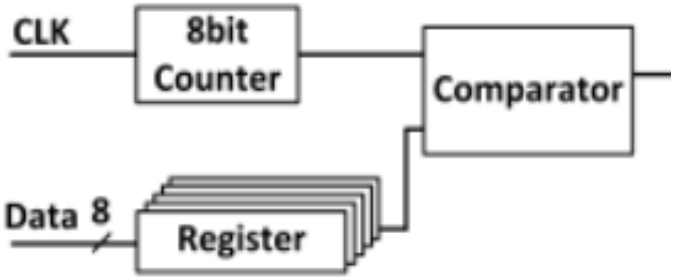
PULSE WIDTH MODULATION GENERATOR DESIGN

A Simple PWM Signal Generator Design in Verilog HDL



Introduction to PWM

- **PWM (Pulse Width Modulation):**
  - A technique used to control the power delivered to electrical devices.
  - The duty cycle (percentage of time signal is high) controls the average power.
  - Applications: Motor control, signal modulation, power supply regulation, etc.

VERILOG CODE:

Inputs:

- clk (Clock Signal)
- rst (Reset Signal)
- dutycycle (8-bit input for PWM duty cycle)

Output:

- out (PWM Output Signal)

Key Feature: The output out generates a square wave with a duty cycle controlled by the dutycycle input.

Registers:

- counter: An 8-bit register that counts clock cycles.

Behavior:

- The counter increments on every clock cycle.
- The PWM output is high when the counter is less than the duty cycle.

Always Block:

- Triggered by positive edge of clk or rst.
- If rst is active, reset counter to 0 and output out to 0.
- If rst is not active, increment the counter and check if the counter value is less than the dutycycle.

PWM Generation Logic:

- If the counter value is less than the dutycycle, set out to high (1).
- Otherwise, set out to low (0)

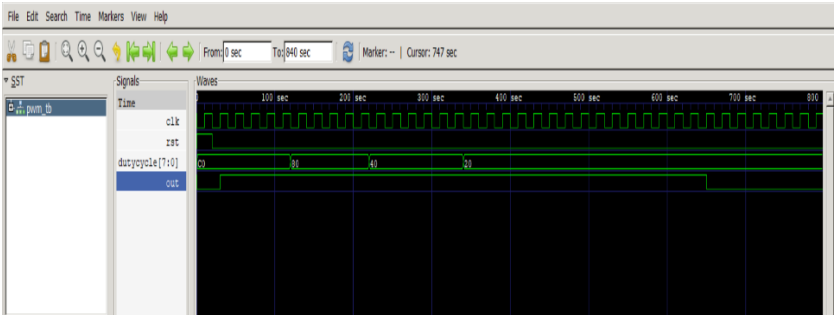
Working of the PWM Generator

Clock Driven:

- The clock signal (clk) drives the timing of the PWM signal.

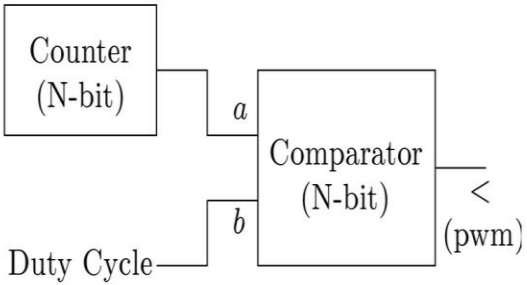
Duty Cycle Control:

- The dutycycle input adjusts the high time of the PWM signal.
- A dutycycle of 128 (50%) means the PWM signal is high for half the time and low for the other half.



Applications of PWM

- **Motor Control:**
  - Varying the duty cycle can control the speed of DC motors.
- **Signal Modulation:**
  - Used in communication systems and signal encoding.
- **Power Control:**
  - Efficient power delivery in power electronics.



Conclusion:

The PWM generator in Verilog is a simple yet powerful way to control the pulse width modulation signal based on an input duty cycle.