data_flow.v | tb2.v | Untitled 10

C:/Users/Pyami/verilog/verilog.srcs/sources_1/new/data_flow.v

```
1  module data_flow(a,b,and_out,or_out,nand_out,nor_out,notb_out,xor_out,xnor_out);
2   input a,b;
3   output and_out,or_out,nand_out,nor_out,notb_out,xor_out,xnor_out;
4   assign and_out=a&b;
5  assign or_out=a|b;
6   assign nand_out=~(a&b);
7   assign nor_out=~(a|b);
8   assign notb_out=~b;
9   assign xor_out=a^b;
10  assign xnor_out=~(a^b);
11  endmodule
12
```

logic gates.v × Untitled 1 ×

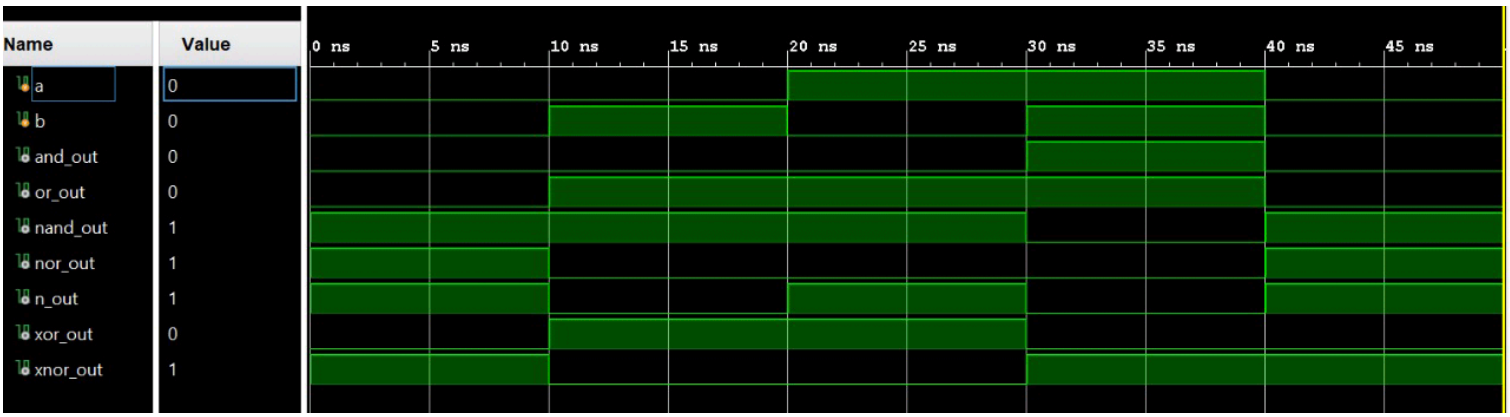
C:/Users/Pyami/verilog/verilog.srcs/sources_1/new/logic gates.v

```
1
2   module logic_gates (a,b,and_out,or_out,nand_out,nor_out,n_out,xor_out,xnor_out);
3   input a,b;
4   output and_out,or_out,nand_out,nor_out,n_out,xor_out,xnor_out;
5   and a1(and_out,a,b);
6   or a2(or_out,a,b);
7   nand a3(nand_out,a,b);
8   nor a4(nor_out,a,b);
9   not a5(n_out,b);
10  xor a6(xor_out,a,b);
11  xnor a7(xnor_out,a,b);
12  endmodule
13
```

data_flow.v × | tb2.v × | Untitled 10 ×

C:/Users/Pyami/verilog/verilog.srcs/sim_1/new/tb2.v

```
1  module tb2( );
2  reg a,b;
3  wire and_out,or_out,nand_out,nor_out,notb_out,xor_out,xnor_out;
4  data_flow uut(
5   .a(a),
6   .b(b),
7   .and_out(and_out),
8   .or_out(or_out),
9   .notb_out(notb_out),
10  .nand_out(nand_out),
11  .nor_out(nor_out),
12  .xor_out(xor_out),
13  .xnor_out(xnor_out)
14 );
15 initial
16 begin
17  a=0; b=0; #10
18  a=0; b=1; #10
19  a=1; b=0; #10
20  a=1; b=1; #10
21  a=0; b=0; #10
22  $finish;
23 end
24 endmodule
25
```


Name
Value
0 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns
40 ns
45 ns
a
0
b
0
and_out
0
or_out
0
nand_out
1
nor_out
1
n_out
1
xor_out
0
xnor_out
1